Test Results of the Tracking Detector Readout ASIC, SMX2, for the Compressed Baryonic Matter Experiment

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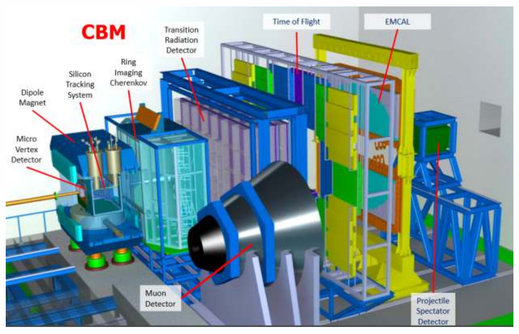
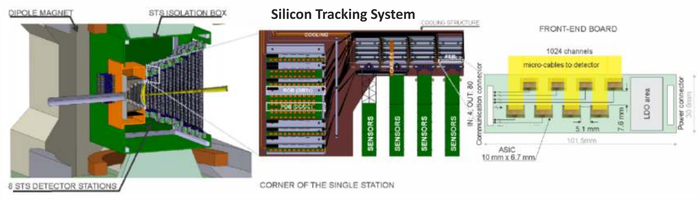
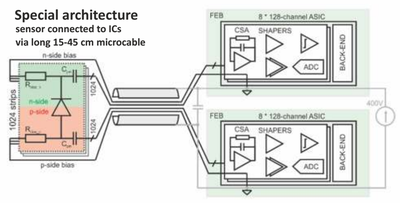
Overview of the target application: Compressed Baryonic Matter Experiment



Experiment aim: Creation of the highest baryon densities in nucleus-nucleus collisions, exploration of the properties of the super-dense nuclear matter.





Similar requirements of two detector systems

Detector system	STS	MUCH
Sensor type	Silicon microstrip, double-sided, AC-coupled, stereo-angle 7° on n-side, 280 - 320 µm thickness	GEM
Sensor lengths	2cm, 4cm, 6cm	
Microcable lengths	15 cm - 47 cm	
Expected capacitance	0-50 pF	1 - 50 pF
Hit rate	250 kHz average	Up to 2 MHz (in central pads)
Channel pitch	58 µm	~ 100 µm
Power consumption [mW/channel]	< 10	< 10
Dynamic range	0-15 fC 4 fC typical	1-100 fC
Time measurement accuracy	< 10 ns	
Signal polarity	positive, negative	negative
Operating temperature	~ -10 °C	~ 80 °C

NEED FOR A SINGLE PROTOTYPE READOUT ASIC

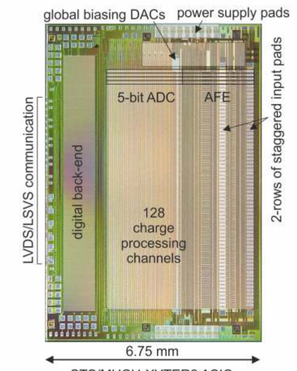
SMX2 Chip: microstrip Silicon & GEM sensors readout

STS-MUCH-XYTER2 developed & fabricated in Q3 2016

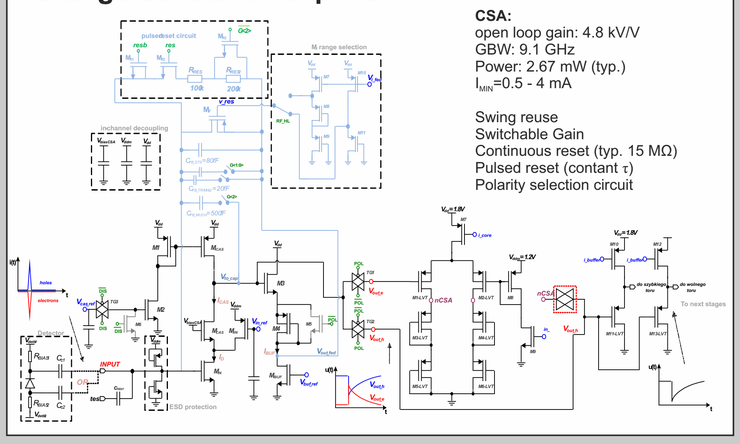
AFE (Analog Front-End)
- time and amplitude measurement
- digitization and derandomized readout
- 128 channels (+ 2 test channels with direct outputs)
- time (3.125 ns, 14-bit timestamp) & amplitude digitization (5-bit)
- gain switching & trimming:
  - 0-12 fC electrons & holes (STS Si microstrips)
  - 0 - 50 fC electrons (MUCH GEMs)
- 250 khit/s rate (pulsed reset)
- 80-280 ns shaping time (slow path)
- time-walk corrected offline
- continuous-time ADC + peak det.
- P=7.6 mW/channel (incl. logic)

Back-end:
- control via synthesized reg & AFE DICE cells
- 9.41 – 47 Mhit/s/ASIC data BW
- throttling, diagnostic features
- link loopback (multi-level)
- 64-bit e-fuse for traceability

- die size: 10 mm x 6.75 mm
- tab bonding, wire-bonding, pogo-probing, wafer-level probing
- Technology: UMC 180nm CMOS MM/RF



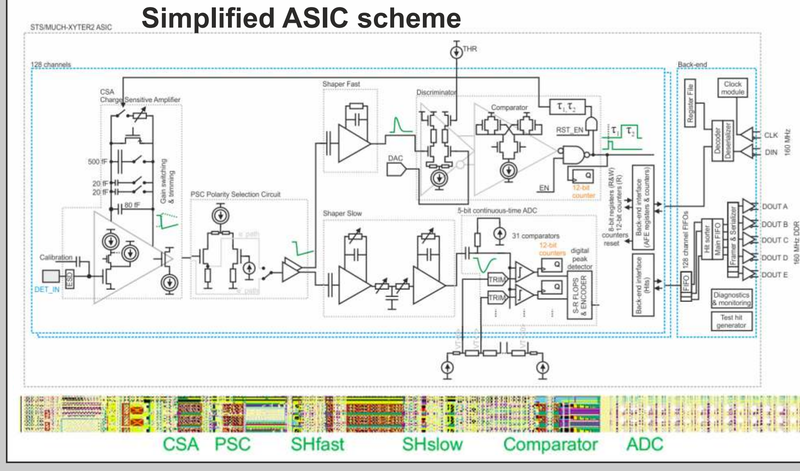
Charge-Sensitive Amplifier



CSA:
open loop gain: 4.8 kV/V
GBW: 9.1 GHz
Power: 2.67 mW (typ.)
I_{MIN}=0.5 - 4 mA

Swing reuse
Switchable Gain
Continuous reset (typ. 15 MΩ)
Pulsed reset (contant τ)
Polarity selection circuit

Simplified ASIC scheme



Charge-Sensitive Amplifier + Polarity Sel.

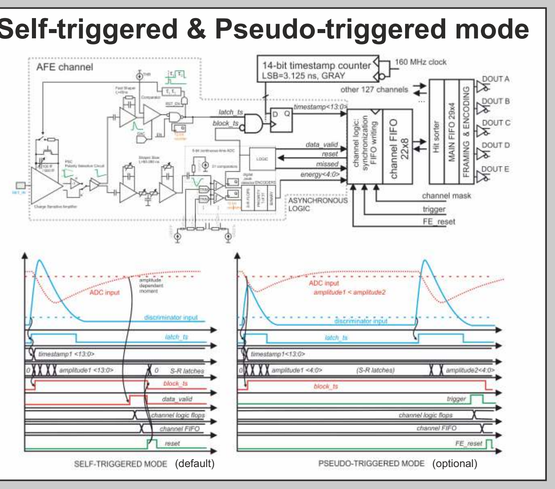
FAST PATH
CR-RC shaper + comparator + timestamp latch

SLOW PATH
CR-RC^3 (shaper) + ADC continuous-time with digital peak detector (no ADC clock)

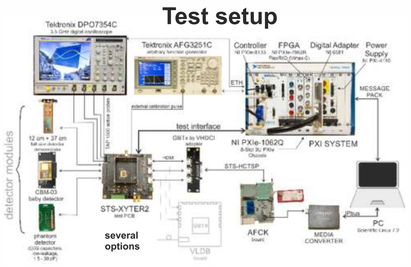
HIT DATA IS FORMED (27 bits)
- 7-bit channel number
- 5-bit amplitude (ADC value)
- 14-bit timestamp
- 1-bit event missed marker

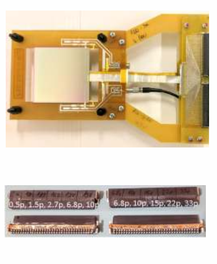
Self triggered operation requires:
- high data throughput of interface
- low rate of noise hits
- throttling options for effective flow control
- link monitoring features

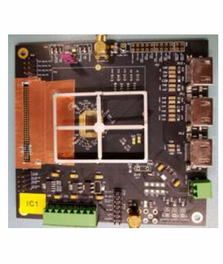
Self-triggered & Pseudo-triggered mode



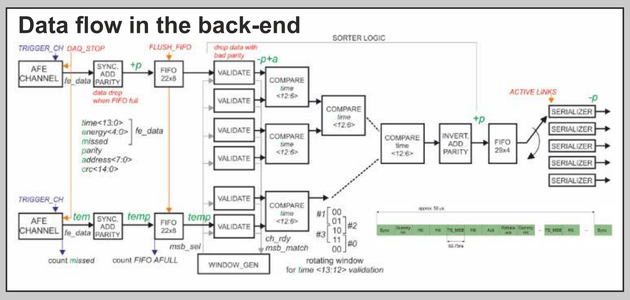
Test setup



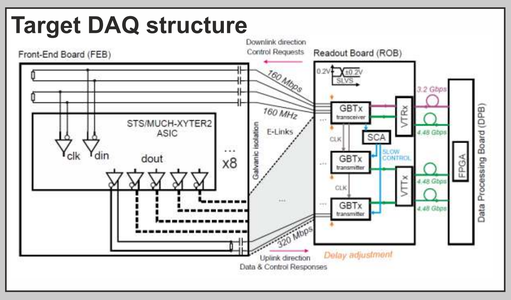




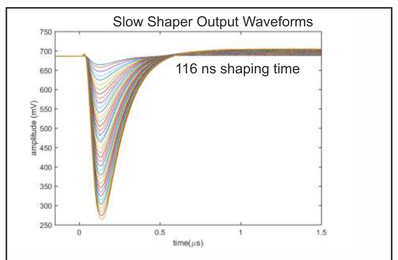
Data flow in the back-end

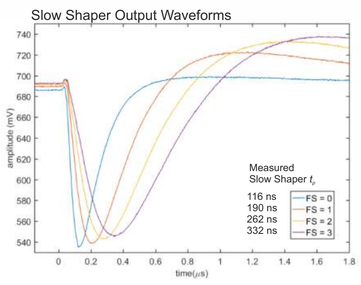


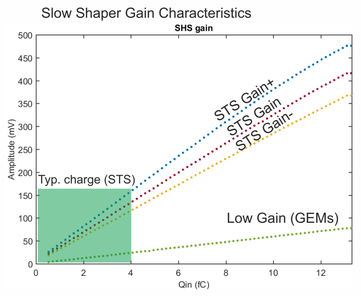
Target DAQ structure

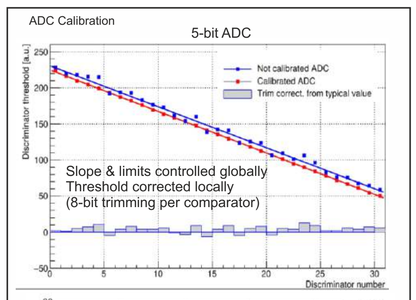


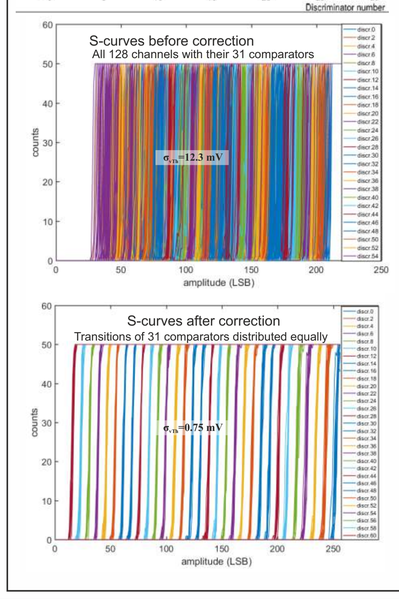
Amplitude measurements with 5-bit Continuous Time ADC (in every channel)

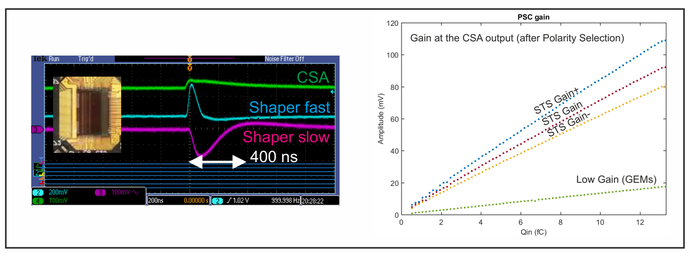


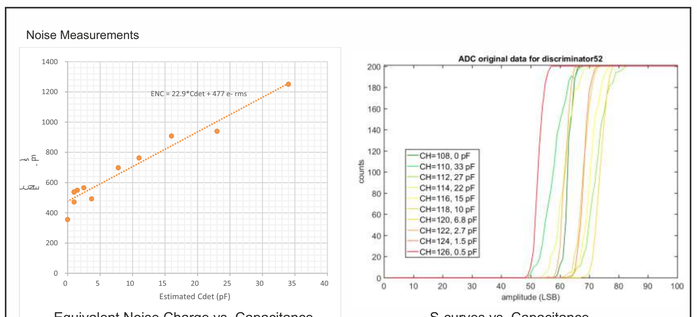


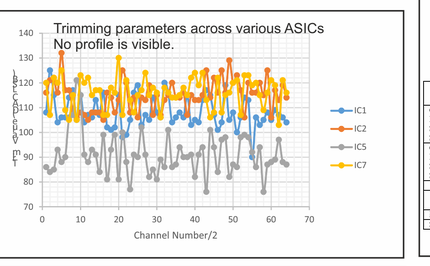










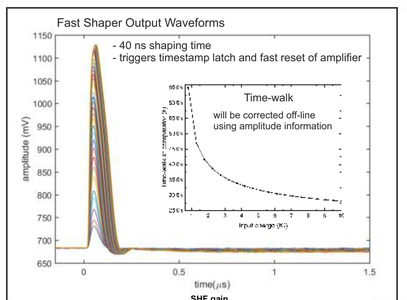


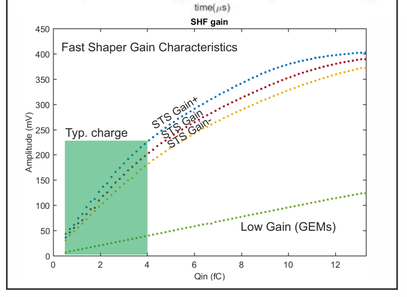
AFE gain parameters

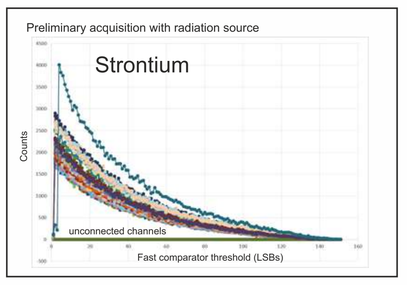
	-trim [mV/fC]	Nominal [mV/fC]	+trim [mV/fC]
Gain MUCH			
PSC	1.28	1.32	1.36
SHfast	9.30	9.35	9.72
SHslow	5.67	5.80	5.98
Gain STS			
PSC	5.99	6.90	8.16
SHfast	45.08	50.44	57.28
SHslow	27.97	32.06	37.97

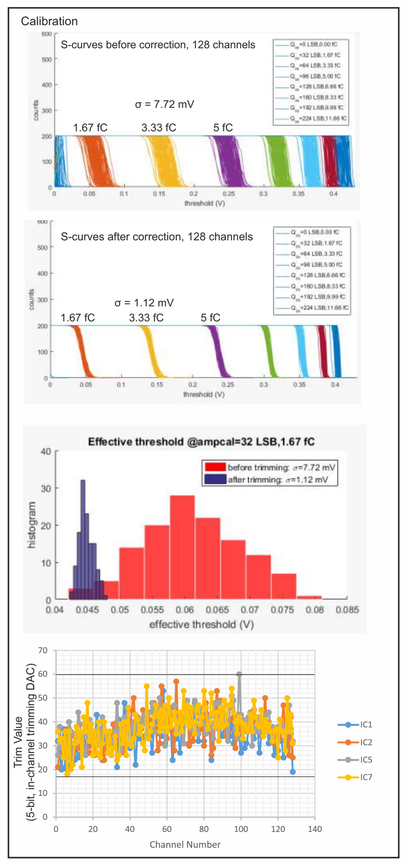
Shaping time setting	0	1	2	3
Measured t_p (ns)	116	190	262	332
Simulated t_p (ns)	90	150	220	280

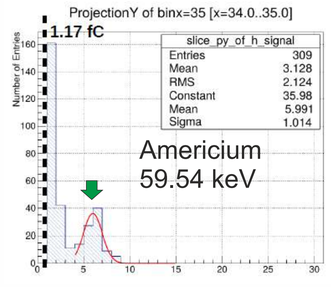
Time measurements with comparator & 3.125 ns resolution timestamping





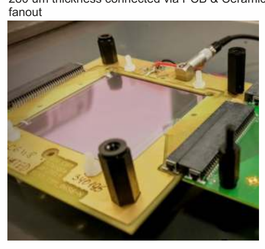




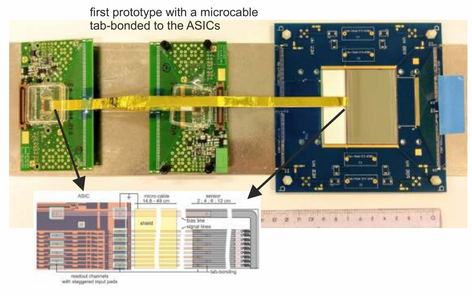


Preliminary acquisition with radiation source

6 cm long, double-sided Si sensor
280 um thickness connected via PCB & Ceramic fanout



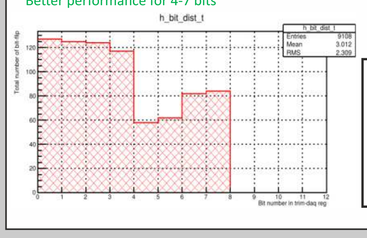
first prototype with a microcable tab-bonded to the ASICs



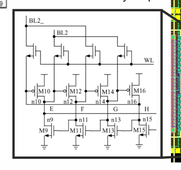
SEU Immunity

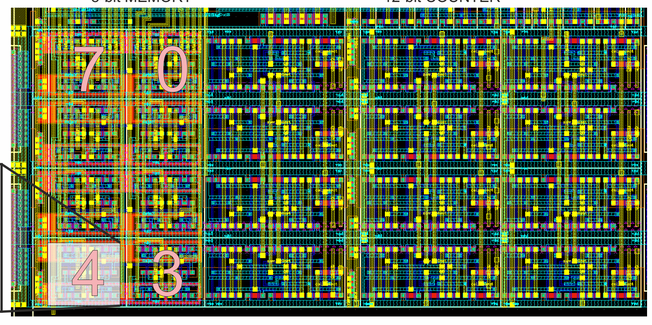
Beam test @ COSY, Juelich, Germany

Observations:
Synthesized registers using Triple-Modular Redundancy behave the best
Overall good performance of DICE cells
Better performance for 4-7 bits



DICE memory cells
store AFE configuration
>4kbits of memory/chip





Changes in the next ASIC revision SMX2.1 :

- enhanced resolution of ADC reference threshold (2000 e^- down to 200 e^-) => precise threshold setting above noise level
- internal biasing / power supply monitoring circuit => to enhance module self-check capabilities after assembly
- enhanced SEU immunity (DICE cells & counters in full-custom part) => increased and equalized cross-sections among all config. bits
- improve layout against latchup at very high doses => to mitigate observed latchups during beam tests
- minimize ESD protection diodes at the amplifiers input => to reduce the leakage-related effects: increased noise and operating point shift

Summary

- 128-channel, 58-µm pitch, amplitude & time digitizing ASIC designed for 10-50 pF capacitive sensors (Si microstrip & GEM)
- radiation-hardened and dedicated for CBM experiment conditions but can be reused in other applications
- simple and high-bandwidth protocol for deterministic-latency communication, synchronization and self-triggered or pseudo-triggered data acquisition
- promising test results, minor changes are required in the high-volume production version

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