Biasing Potentials Monitoring Circuit for Multichannel Radiation Imaging ASIC In-system Diagnostics

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Diamentowy Grant

Outline

Introduction :

- CBM Experiment, STS & MUCH detectors

Motivation

- Need for on-line monitoring & calibration
- Problems

Circuit Design:

- Internal monitoring circuit overview
- Simulations results
- Next steps

This work was funded by Ministry of Science and Higher Education Poland, from the scientific budget in years 2016-2018 – research project in the programme “Diamentowy Grant”.

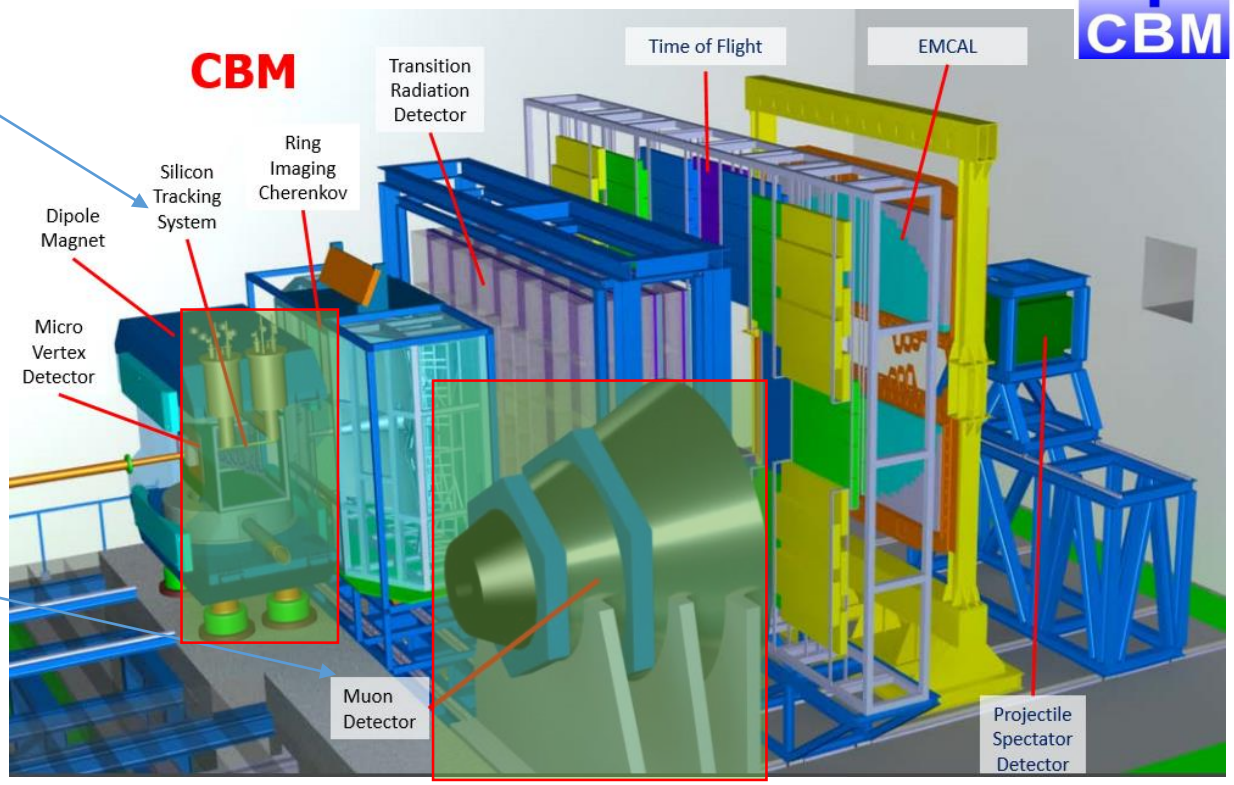
The CBM experiment at GSI

STS (*Silicon Tracking System*) detector

- tracking and momentum determination of the charged particles
- the interaction rate of 10 MHz
- 8 tracking stations in distances from 30 cm to 100 cm from the target
- 1T magnetic dipole field

MUCH (*Muon Chamber*)

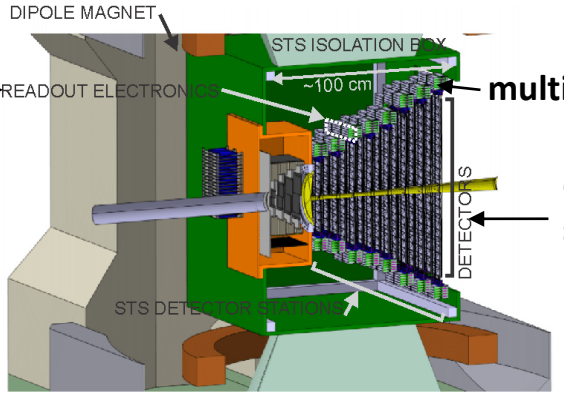
- Gas Electron Multiplier detector
- 18 gaseous chambers
- 6 hadron absorber layers



Experiment aim: Creation of the highest baryon densities in nucleus-nucleus collisions, exploration of the properties of the super-dense nuclear matter.

The CBM experiment at GSI:STS (*Silicon Tracking System*) detector

readout electronics (STS-XYTER2 chips) at the perimeter of the detector stations on FEB boards (8 chips/board) + data concentrators (GBTx-based ROB boards)

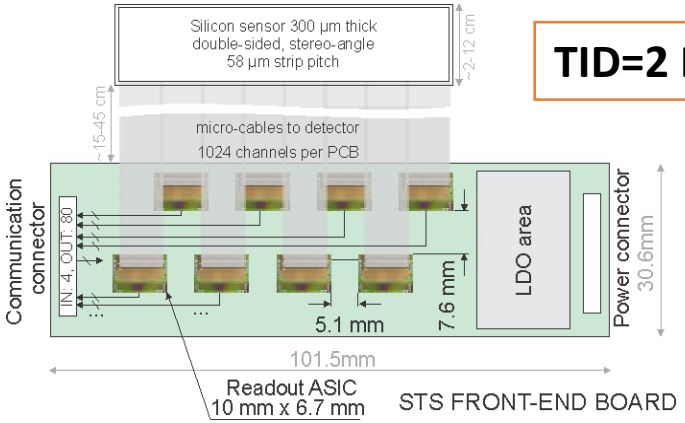


multi-line micro-cables -> sensors read out

double–sided, micro-strip sensors, 1024 CH/side, 7.5°stereo angle, 58 μm strip pitch

The STS/MUCH-XYTER2:

- developed at AGH University Cracow
- 10 mm × 6.75 mm
- 128 readout channels + two test channels
- **each channel**:
  - Charge Sensitive Amplifier (CSA),
  - Polarity Selection Circuit (PSC),
  - fast and a slow pulse shaping amplifiers (shapers),
  - timing discriminator
  - 5-bit continuous-time, flash analog-to-digital converter (ADC)
- **digital back-end**: communication via application-specific protocol STS-HCTSP, logic for register access, data read-out, and streaming + some diagnostic features.



TID=2 Mrad during lifetime

STS metrics:

>1 790 000 channels

>14 000 ASICs

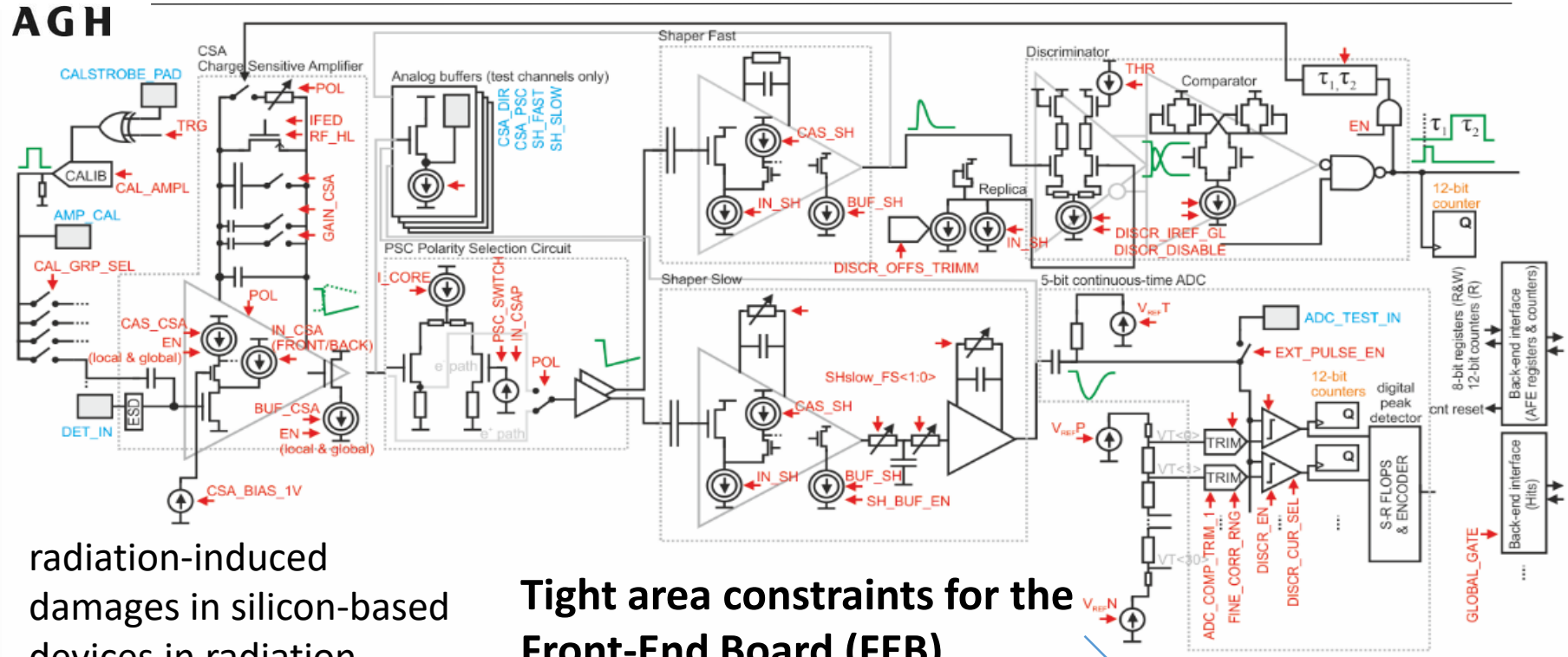
1752 FEBs

>20 reference voltages/ASIC

4420B of AFE configuration (16 global DACs + switches + in-channel ctrl)

multiple on-FEB power supply circuits

Need for monitoring of internal potentials

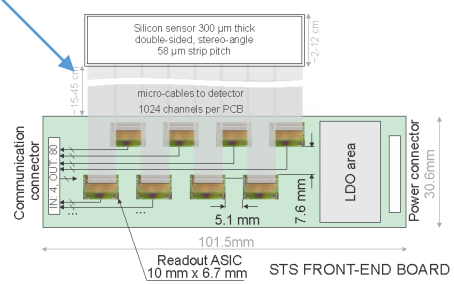


radiation-induced damages in silicon-based devices in radiation imaging integrated circuits -> **in-system tests** required

the root cause of the performance degradation

Tight area constraints for the Front-End Board (FEB)

- 101.5 mm × 30.6 mm FEB area,
- 8 10 mm × 6.75 mm ASICs,
- several low-noise application-specific low-dropout voltage regulators (LDO)
- power and communication interface connectors

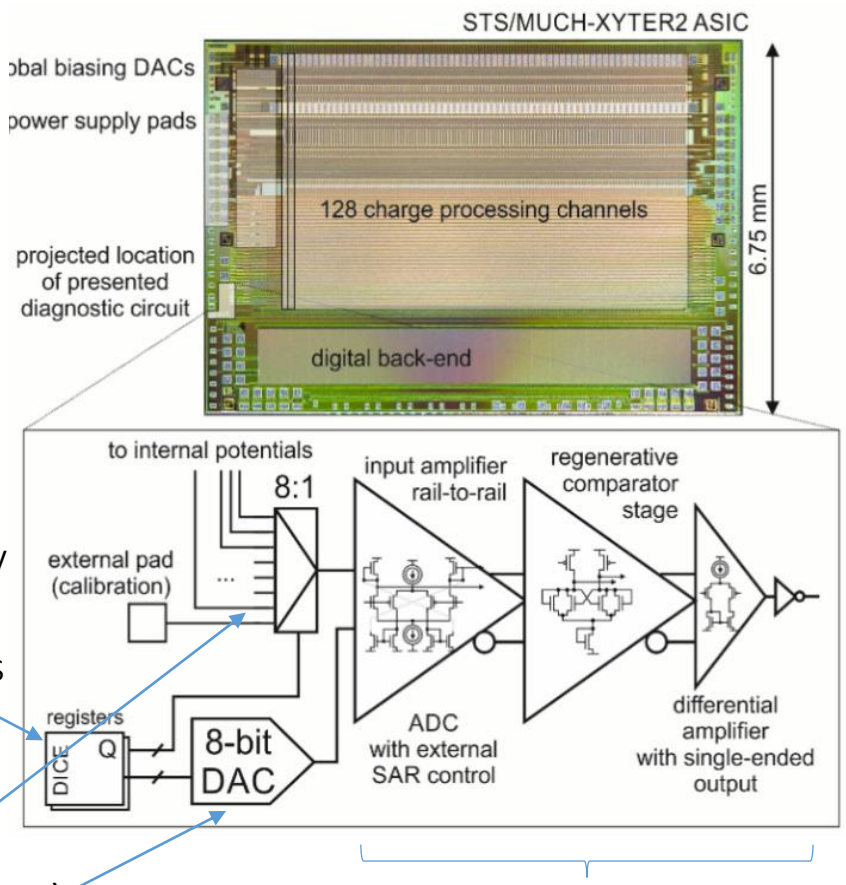


Internal bias monitoring circuit – overview

remote measurement of important voltages inside the circuit during the experiment lifetime (10 years) and correction of the circuit's settings to restore the optimum performance in the harsh, irradiated environment and power supply fluctuation conditions

1-bit successive approximation register (SAR) ADC with the reference digital-to-analog converter (DAC) controlled from the higher-level circuit in the CBM DAQ system

- radiation-hardened by design
- operability across the wide range of supply voltages and extended operating temperature range (-20–85 ºC)
- measurements of voltages close to supply rails
- circuit fully controlled by the register cells available within the ASICs address space

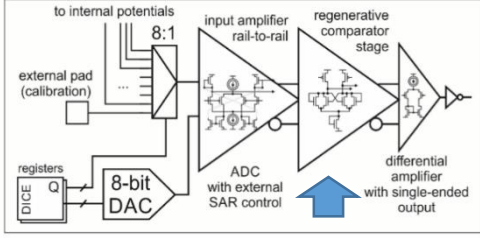


8:1 analog multiplexer

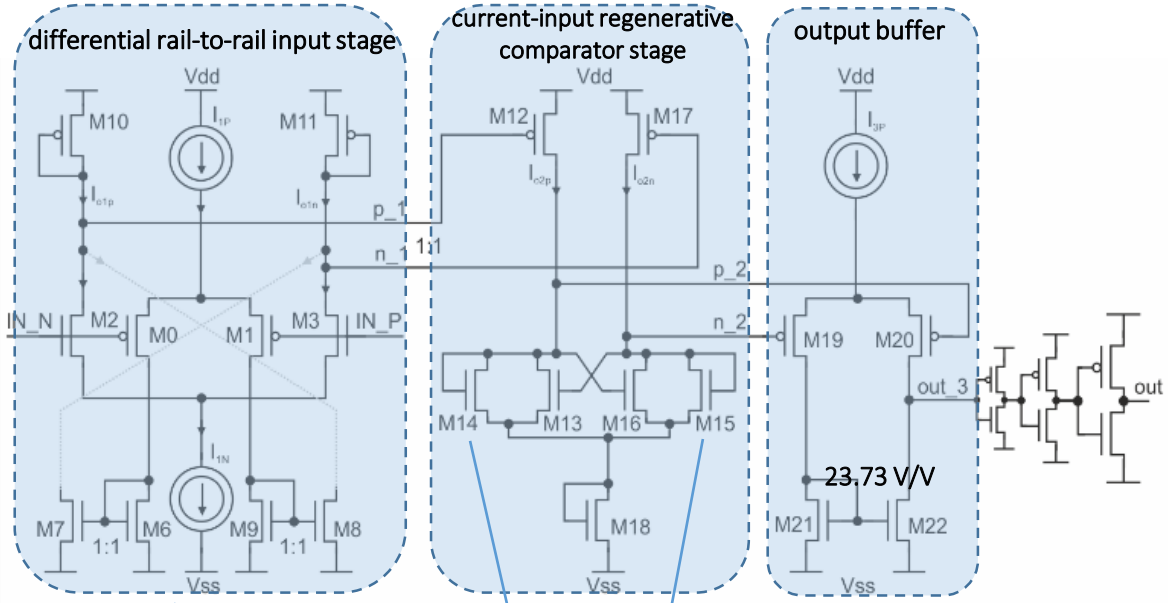
8-bit DAC (reference voltage)

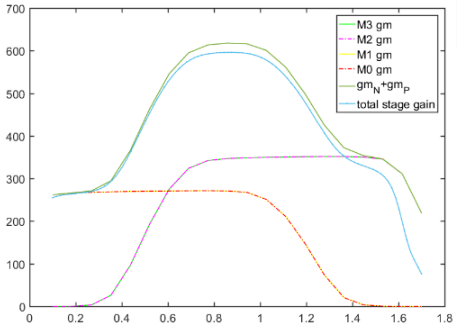
3 stage general purpose rail-to-rail comparator

Three-stage comparator



- rail-to-rail operation (input stage)
- nominal gain: **595.70 µA/V**
- gain vs. power supply voltage characteristics change due to power supply voltage fluctuations: **572 µA/V²** falling down to **270 µA/V** for 1.2 V
- gain temperature drift: **1 µA/V·K**

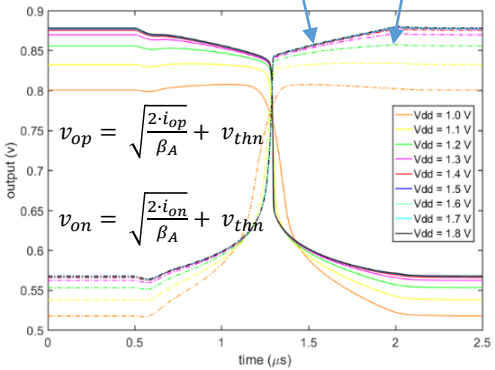




Param.	Nominal conditions (DC=0.9 V, T=27 °C, V_{dd}=1.8 V)			
	Nominal value	Monte Carlo mismatch	Monte Carlo process	Corners
Gain (µA/V)	595.70	µ=592.96 σ=4.37	µ=590.45 σ=13.91	µ=592.55 σ=13.57
BW (MHz)	12.85	12.82	11.90	12.80

hysteresis width:
~ **4.43 mV**
$(W/L)_{14,15}$=20/0.5
$(W/L)_{13,16}$=22/0.5

$$v_h \sim \frac{\frac{W_{14,15}}{L_{14,15}} - \frac{W_{13,16}}{L_{13,16}}}{\frac{W_{14,15}}{L_{14,15}} + \frac{W_{13,16}}{L_{13,16}}}$$

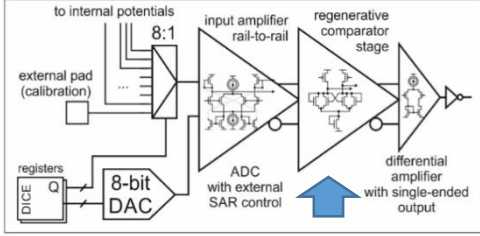


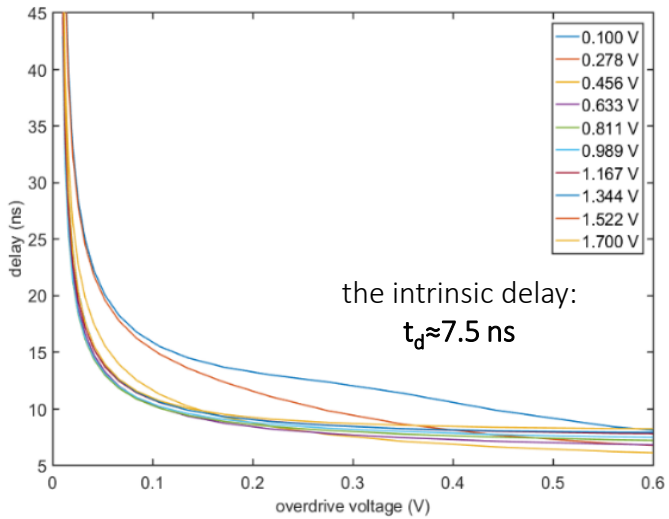
Additional gain + conversion of differential signals to the single-ended fast-edge signal

$$g_{m19,20} \cdot (r_{o20} || r_{o22})$$

Param.	Output amplifier			
	Nominal value	Monte Carlo mismatch	Monte Carlo process	Corners
Gain (V/V)	23.55	µ=22.94 σ=0.89	µ=23.29 σ=.36	µ=23.90 σ= 1.38
BW (MHz)	16.64	16.67	16.68	16.14

Three-stage comparator

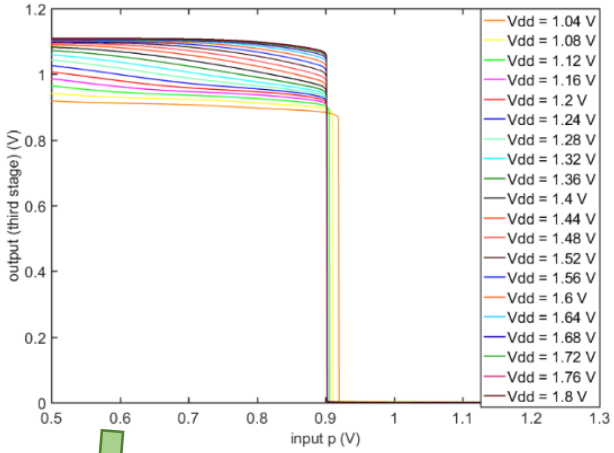




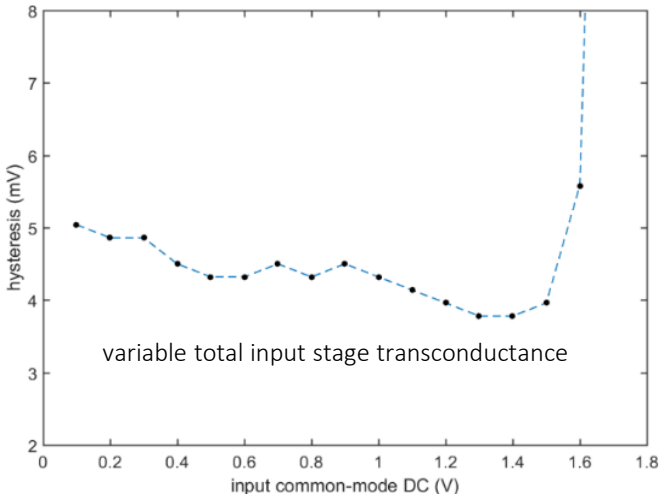
The delay degradation related to the applied voltage -> significant (exceeding 10 ns) for overdrive voltages **below 100 mV**

single conversion step (register access): **2.76 µs**

Comparator output for different supply voltages



Power supply voltages greater than ~**1.1 V** – no severe performance degradation (nominal 1.8 V)

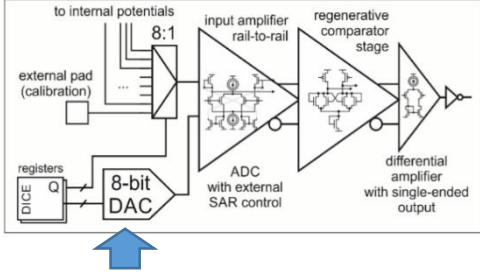


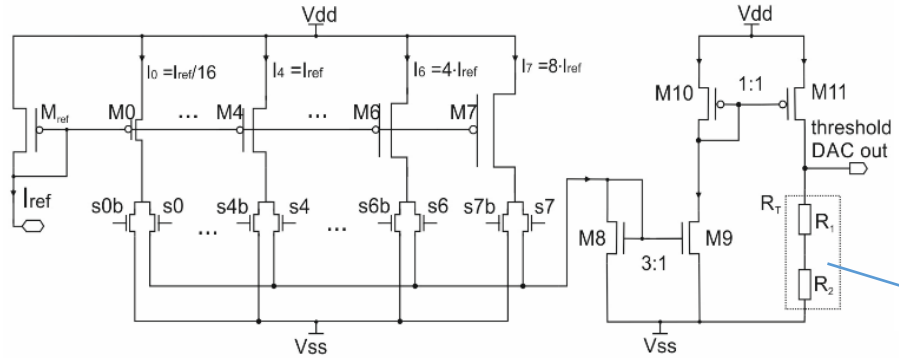
input-referred noise is equal to **82.66 µV_{RMS}**

hysteresis↓ ~2.34 mV/V
delay↑ ~30 ns/V
(power supply drop 1.8 V -1.3 V)

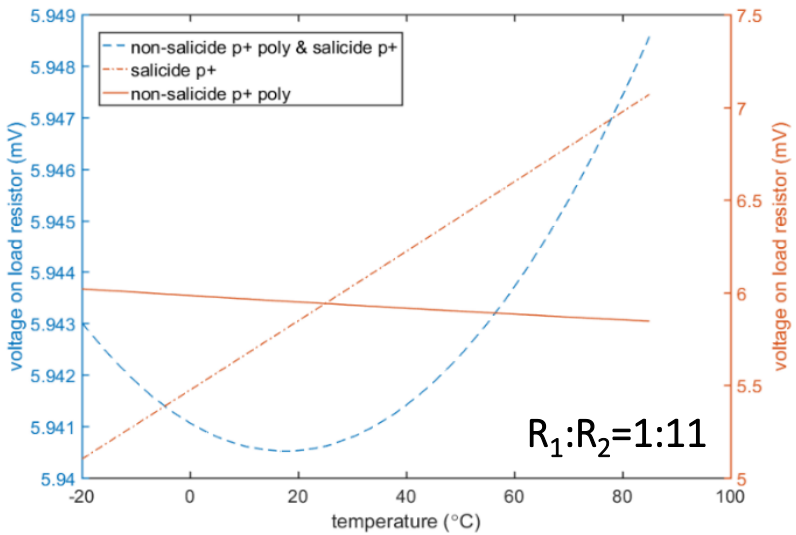
Param.	Nominal conditions (DC=0.9 V, T=27 °C, **V_{dd}=1.8V**)			
	Nominal value	Monte-Carlo mismatch	Monte-Carlo process	Corners
Hysteresis (mV)	4.43	µ=3.46 σ=3.07	µ=4.07 σ=1.02	µ=4.29 σ=1.01
Offset (mV)	0 (42.08 fV)	µ≈0 (43.31 uV) σ=3.85	µ≈0 (50nV) σ≈0 (364.58nV)	µ≈0 (25uV) σ≈0 (70.71uV)
Delay (ns)	36.5	µ=35.30 σ=10.28	µ=36.12 σ=3.09	µ=37.01 σ=3.20

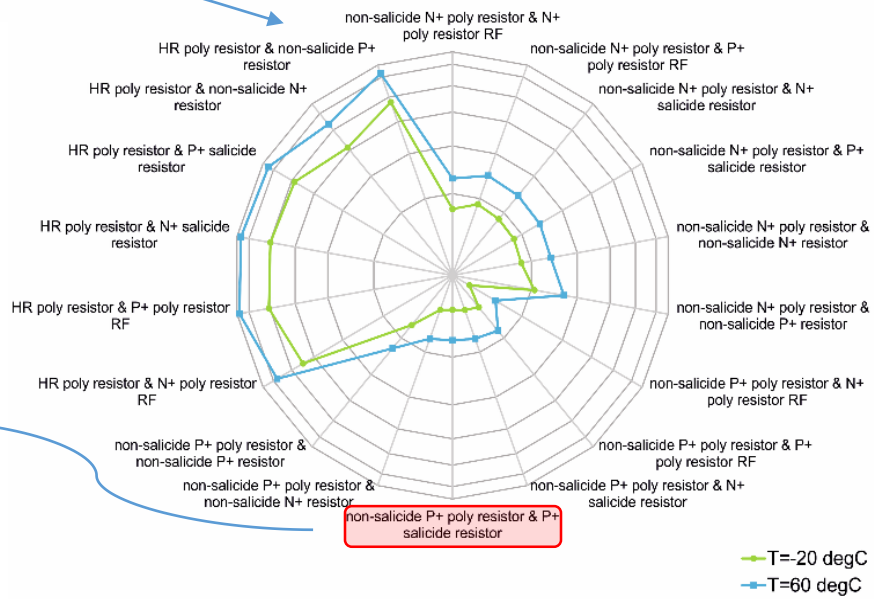
Threshold potentials DAC





The output current from the summing node -> the output voltage via **temperature-compensated** set of resistors connected in series (the resistor pairs with opposite first-order temperature coefficients (TC))

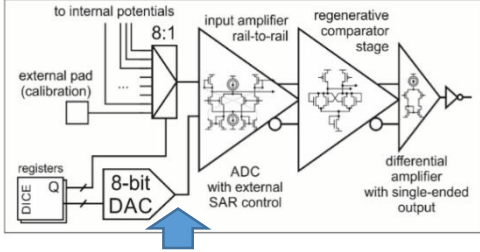




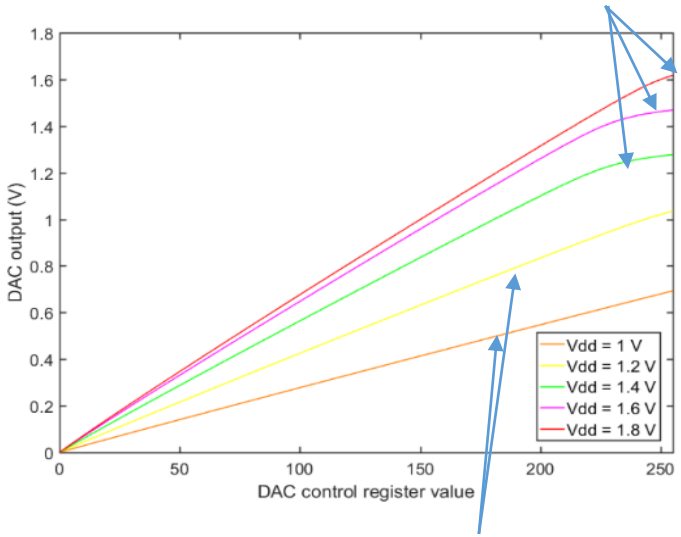
-> absolute change of the output voltage **≈8 µV** in the case of resistors doublet compared to ≈**250 µV** and ≈**2 mV** in case of using non-compensated resistors

18 kΩ in conjunction with 90 µA of output current from DAC -> **0-1.6 V** and LSB equal to **6.27 mV**

Threshold potentials DAC

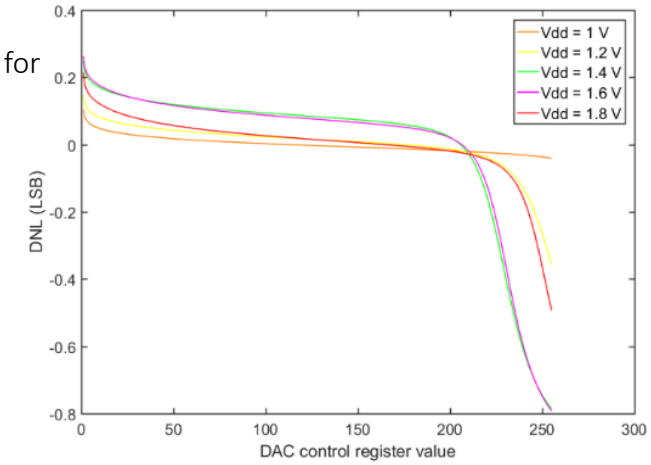


DAC internal circuits impact

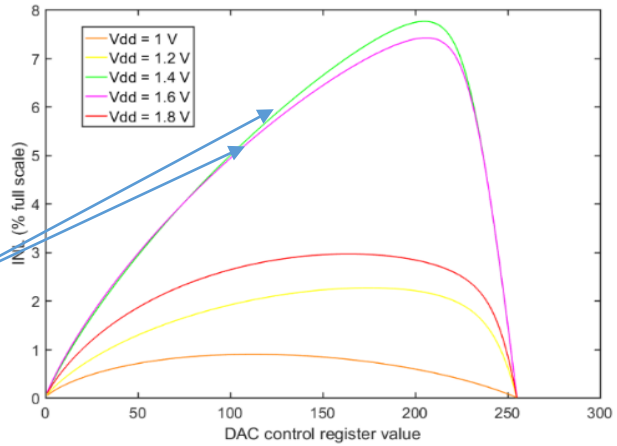


gain error (for voltages below 1.4 V) -> the band-gap reference circuit impact

monotonicity holds for the various supply voltages



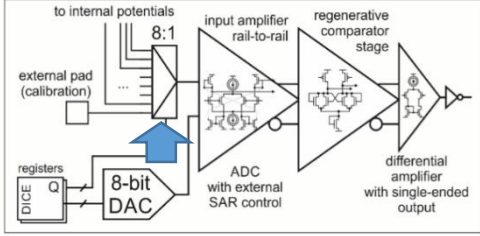
band-gap reference current starts to drop (below approximately 1.4 V)



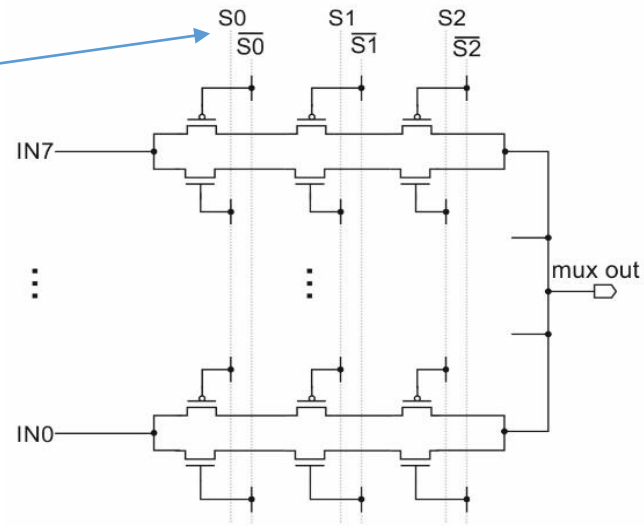
DAC's noise contribution to the entire monitoring circuit's noise: **318.57 μV_{RMS}** at the comparator input

the INL ≤ **2%** of the full-scale (nominal conditions)

Analog 8:1 multiplexer

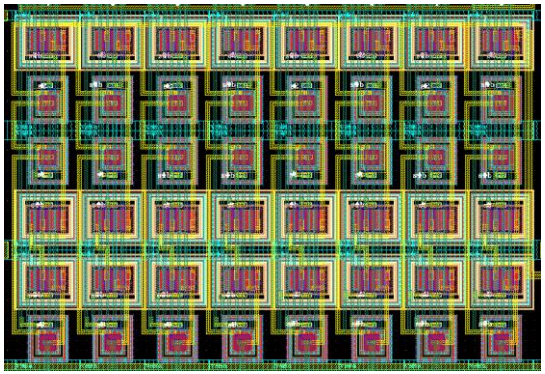


the **decoder** function: 3 complementary control lines are needed

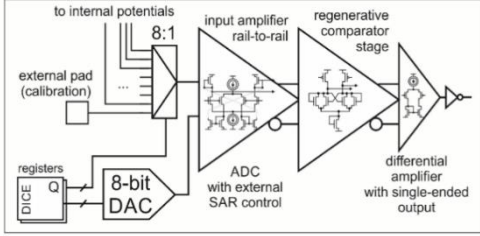


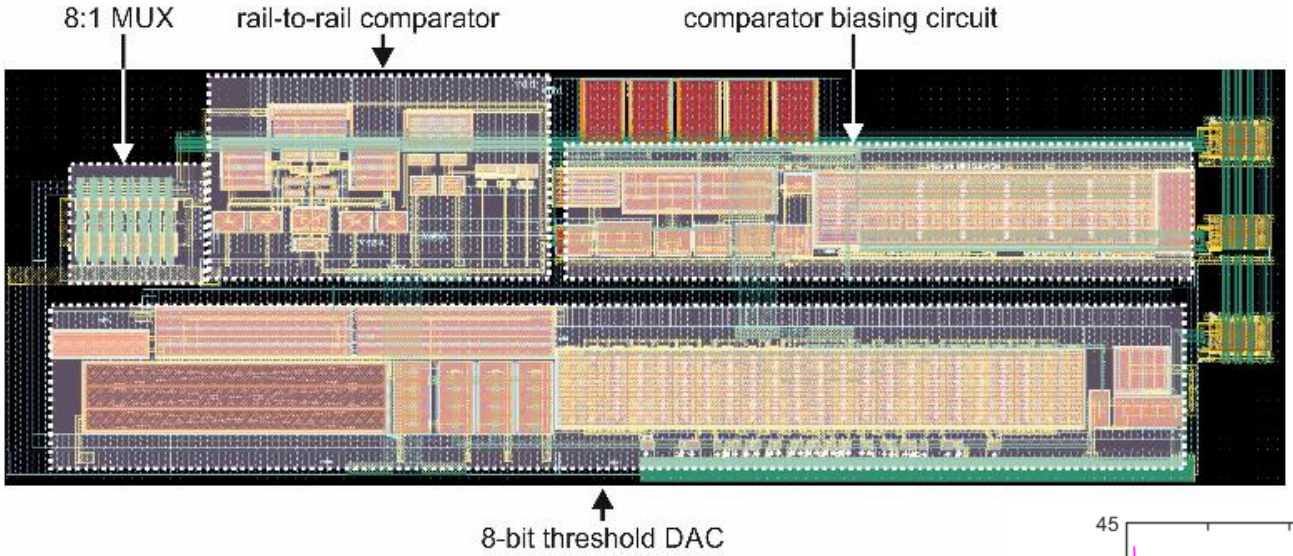
two branches of three transistors in series

- individual control of the input MUX lines,
- scanning - maximum rate of 45 kHz, as a result of 8 successive approximation steps via regular register access through the STS-HCTSP protocol (22 µs in total),
- 8 inputs -> possibility of scaling towards larger numer of input channels,
- one of the inputs -> external potential for calibration of the whole monitoring circuit



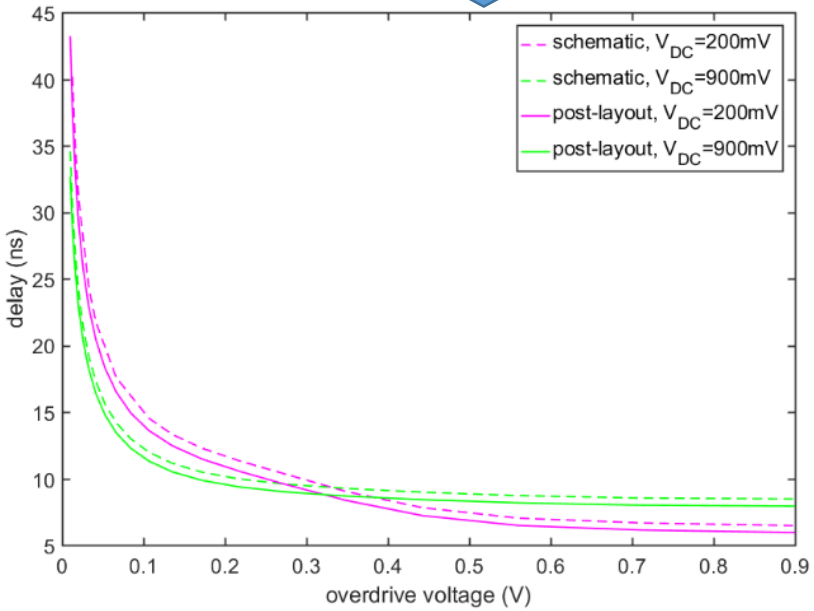
Layout of the diagnostic circuit





Control: three 8-bit memory cells based on dual-interlocked cells for improved single-event upset (SEU) immunity.

Comparator delay vs. overdrive voltage- schematic and post-layout simulation



- area of **660 × 208 μm²** ,
- enclosed-layout transistors (**ELT**) for NMOS devices,
- all transistors are equipped with individual guard rings,
- the first and second stage of comparator -> **symmetric** layout for improved matching,
- **PCAP**-type decoupling capacitors close to the stages generating fast edges.

Summary and future works

Internal potentials monitoring circuit design:

- 1-bit **SAR ADC** with the reference DAC controlled from the higher-level circuit in the CBM DAQ system,
- measurements of **multiple biasing** potentials **close to the supply rails** inside the ASIC, without the necessity of diagnostic pads placement,
- individual control of the 8 input MUX lines,
- setting threshold potentials in a wide range **(0-1.6 V)** with **6.27 mV steps**,
- potentials' scanning at a maximum rate of **45 kHz** (8 successive approximation steps) via regular register access through the dedicated protocol -> single conversion step: **< 3 µs**,
- proper work within extended range of power supply voltage (~ 1 V, by 1.8 V nominal supply) and extended operating temperature range **(-20–85 ºC),**
- radiation-hardened layout.

- Presented circuit will become a part of the new revision of the **STS/MUCH-XYTER2.1** ASIC planned for tape-out in Q4 2017
- Next steps: improvement of band-gap reference circuit.

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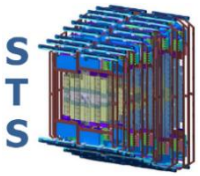

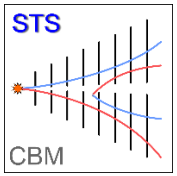

Diamentowy Grant

IEEE SSCS Chapter Poland

Thank you for your attention.

More on STS/MUCH-XYTER2 ASIC: K. Kasiński, W. Zubrzycka, R. Szczygieł, "*Microstrip and Gas Electron Multiplier Readout ASIC for Physics Experiment at FAIR", this conference, June 23rd (Friday), 11:15 (Room A)*