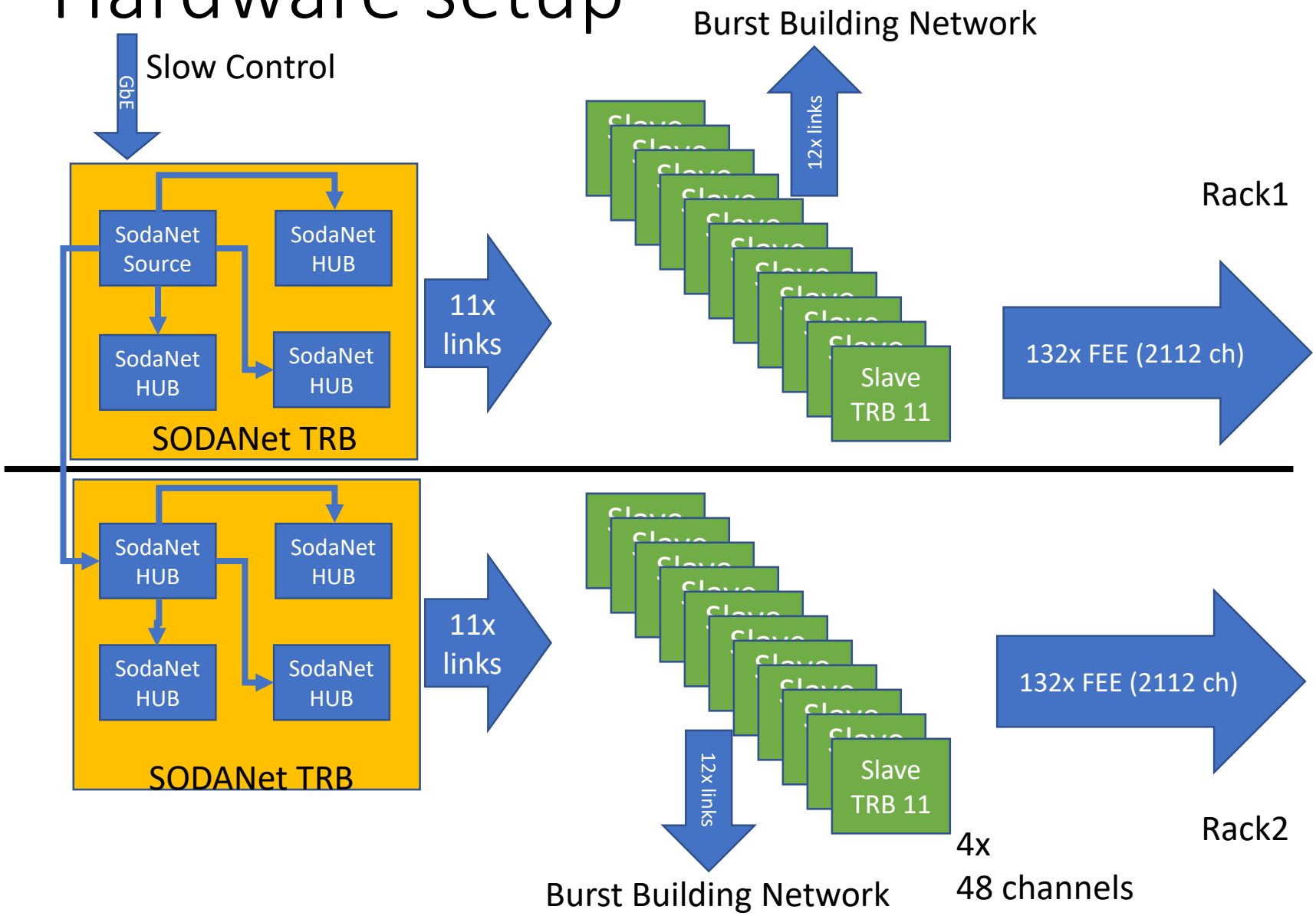
STT with TRBv3

Hardware setup



Hardware summary

- 24x TRBv3 for entire, standalone readout with SodaNet
  - 12x boards per rack
    - 1x for SodaNet
    - 11x for FEE readout
- 8x Optical HUB Addon for SodaNet
  - 31x optical links for SodaNet
- 24x Optical links for TRBv3 readout
  - Burst Building Network
- 1x Optical link Gigabit Ethernet for SodaNet Source slow control
- 264x PASTTREC FEE boards
  - 88x 4Conn Addons for FEE connections
  - 264x LVDS tapes for FEE

Data volumes

- SodaNet
  - Superburst = 16 bursts = 16 * (400 ns + 1600 ns) = 32 us (31 kHz)
  - SB Update triggers readout and delivers SB ID

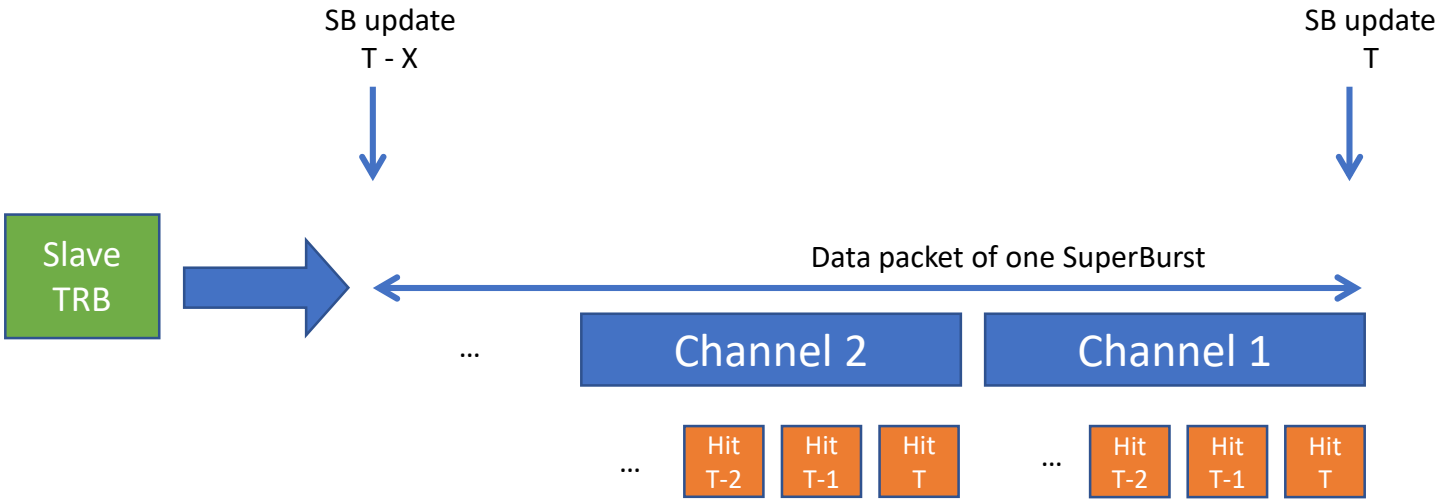
- TRBv3
  - TDC
    - 48 channels
    - Continuous recording, readout at SB Update
      - Time window – period between two SB Updates
    - Data format: 32b – rising Edge, 32b – falling Edge, 32b – epoch counter (inserted each 10,24 us)
    - Ring buffer - 50 hits per channel (latest hits saved)
    - Output buffer – 2k hits per TDC
  - Central – readout
    - 64 kB central buffer

- 80 kHz / straw (max inner rate)
  - 3 hits per SB – 3 * 8B = 24B
  - 24B * 192 channels = 4.6 kB per TRB per SB
  - 4.6 kB * 31 kHz = 142 MBps per TRB per s

- 80 kHz – 32 kHz ~ 56 kHz (average rate)
  - 2 hits per SB – 2 * 8B = 16B
  - 16B * 192 channels = 3 kB per TRB per SB
  - 3 * 31 kHz = 93 MBps per TRB per s

Data ordering

- Time ordered data on channel by channel basis



Readout

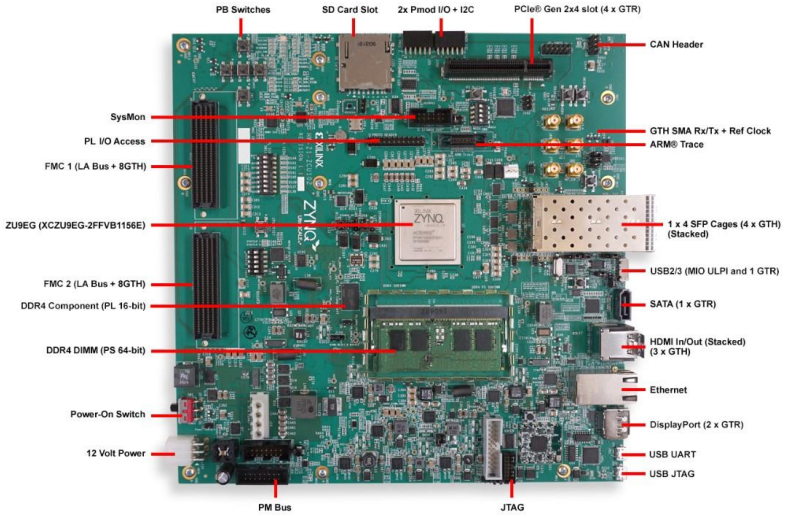
- Individual optical link from each Slave TRB
  - 22x links to the Burst Building Network
  - 1 Gigabit Ethernet (can go through switch)
    - UDP packets
  - Raw (point-to-point, directly to the Compute Node)
    - 8b/10b encoding
    - 3.3 Gbps (limited by internal communication to 1.2 Gbps)

Preprocessing

10x SFP+ FMC Addon

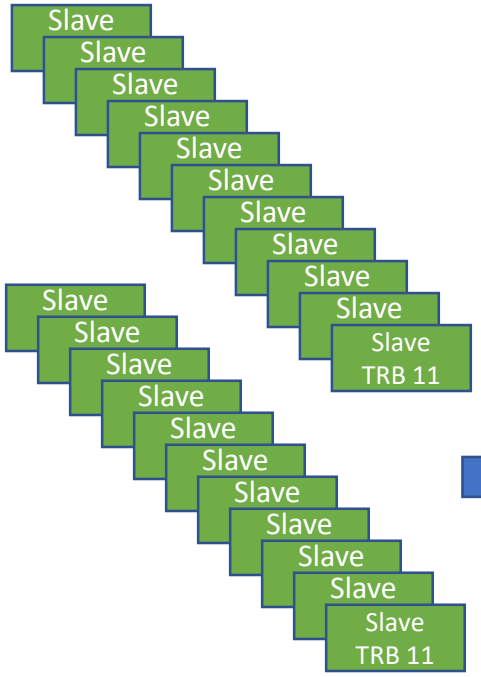
1k EUR

- Use GbE network and commercial switch
- Keep TRBs as they are
- Introduce high-level processing on ZCU102 platform



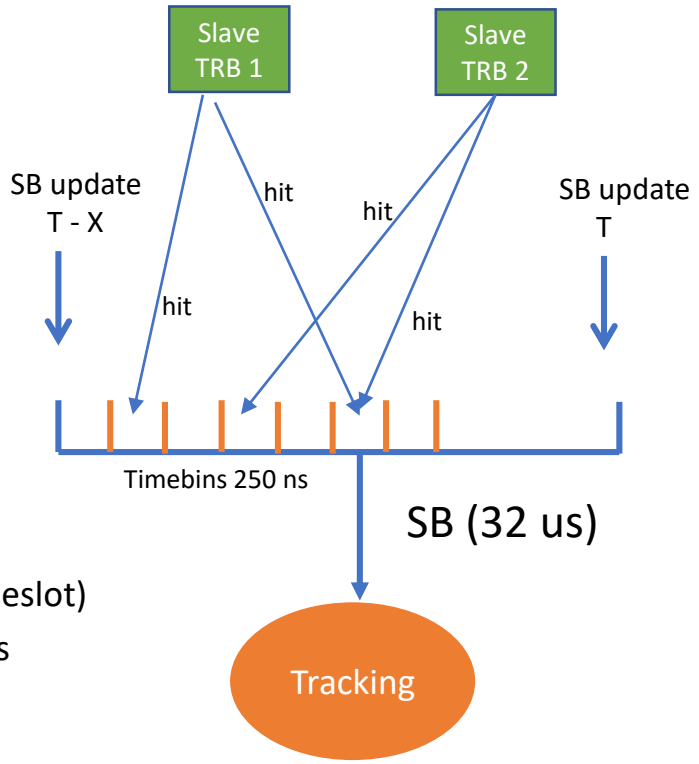
ZCU102
Zynq Ultrascale+ MPSoC
XCZU9EG-2FFVB1156
4GB DDR4
20 SFP+ links

2.6k EUR

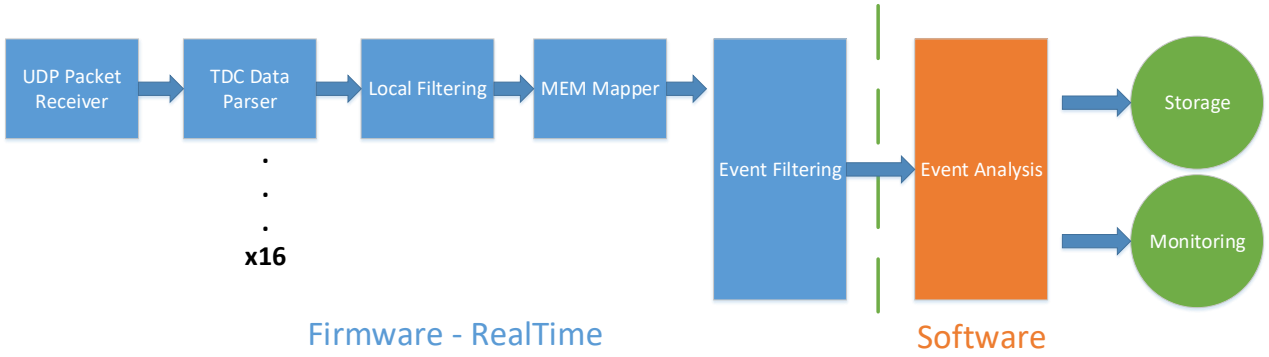


1k EUR

Preprocessing



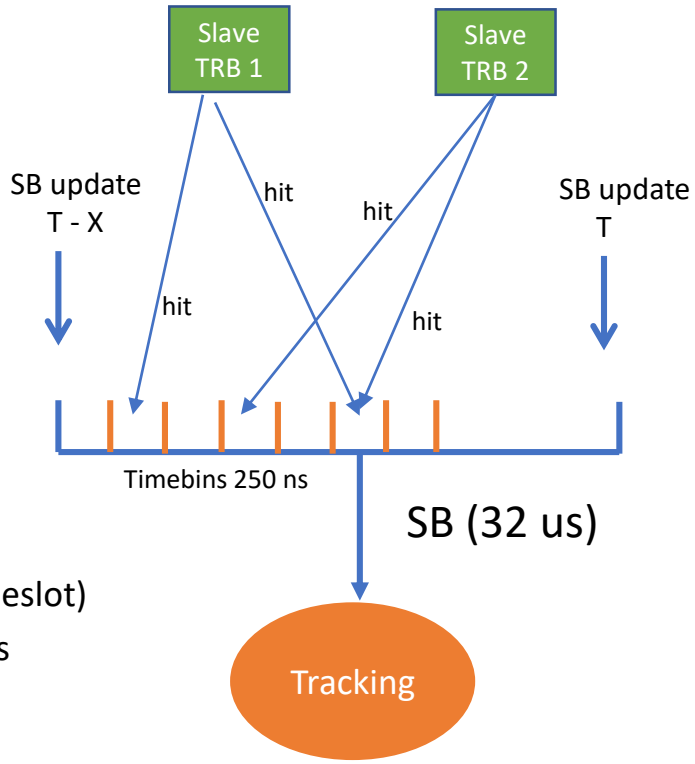
- Hardware:
  - Receive and reassemble SB fragments
  - Parse and decode HIT data
  - Apply calibration constants
  - Qualify HITs into Timebins (e.g.: 32 us / 128 = 250 ns timeslot)
  - Preprocess Timebins in parallel and find track candidates
  - Forward data to the integrated processor
- Software:
  - Determine T0
  - Calculate track candidate parameters

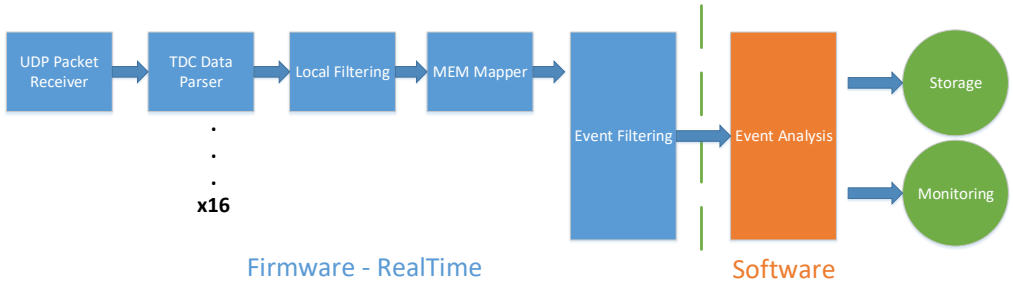


Preprocessing

Hardware available on market

- Hardware:
  - Receive and reassemble SB fragments
  - Parse and decode HIT data
  - Apply calibration constants
  - Qualify HITs into Timebins (e.g.: 32 us / 128 = 250 ns timeslot)
  - Preprocess Timebins in parallel and find track candidates
  - Forward data to the processor
- Software:
  - Determine T0
  - Calculate track candidates parameters





Proof-of-concept up and running: J-PET system – 8 TRBs, 20us and 128 timebins

Power consumption

- TRBv3
  - Board: 48V – 0.3A = 14.4 W
  - Channel: 0,15 mA (0.3 / 192) = 7.2 mW
  - All boards: 24 * 0.3 = 7.2 A = 345 W
  - Per rack: 3.6 A = 173 W

- PASTTREC
  - FEE: 5V – 0.15 A = 750 mW
  - Channel: 0.01 A (0.15 / 16) = 50 mW
  - All FEEs: 264 * 0.15 = 40 A = 200 W
  - Per rack: 20 A = 100 W

Data format

- TRBv3 TDC data format

Data Format	Bits	Description
0x0	31	Time Data Marker
	30-29	reserved
	28-22	channel number
	21-12	fine time - sum of the two transition of the WUL
	11	the type of the measured edge - '1' rising, '0' falling edge
	10-0	coarse time - 5ns granularity
0x1	31	Time Data Marker
	30-29	reserved
	28-22	channel number
	21	reserved
	20-12	fine time - individual values of the two transition of the WUL
	11	the type of the measured edge - '1' rising, '0' falling edge
	10-0	coarse time - 5ns granularity

Table 5: The data format of the *TIME DATA* word.

3 bits	1 bit	28 bits
"011"	reserved	EPOCH Counter

Table 10: The data format of the *EPOCH Counter* word.