PANDA Lecture Week
Introduction into Front End Electronics
Part IV: Time and Analogue to Digital Converter

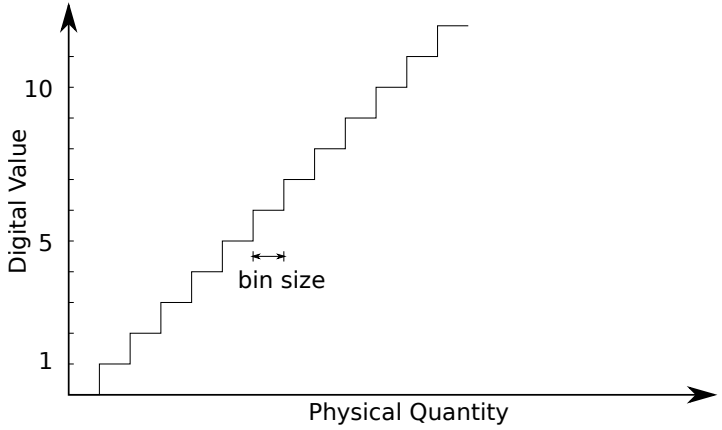
Holger Flemming

GSI Helmholtzzentrum für Schwerionenforschung GmbH
Experiment Electronics Department

07.06.2017

Outline

Introduction



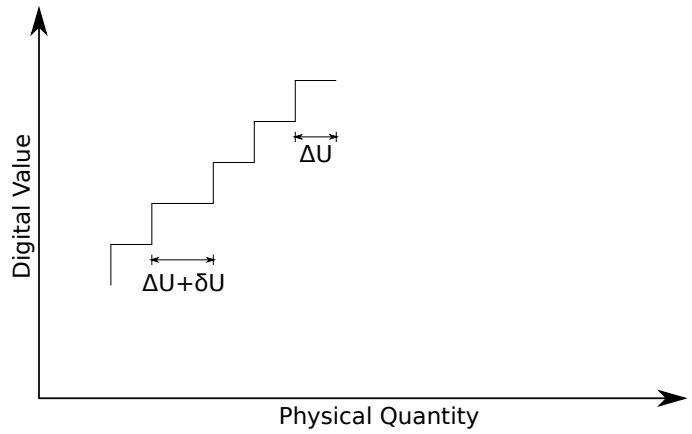
- Task of converter is to convert a digital quantity into a numerical value
  - **T**ime to **D**igital **C**onverter
    Time
  - **A**nalogue to **D**igital **C**onverter
    Voltage, charge, current
- Analogue values in interval $U_i \pm \frac{\Delta U}{2}$ are converted to i
- Bin size: ΔU
- Converter Characteristics:

$$d = \alpha U \tag{1}$$

with $\alpha = \frac{1}{\Delta U}$

Introduction

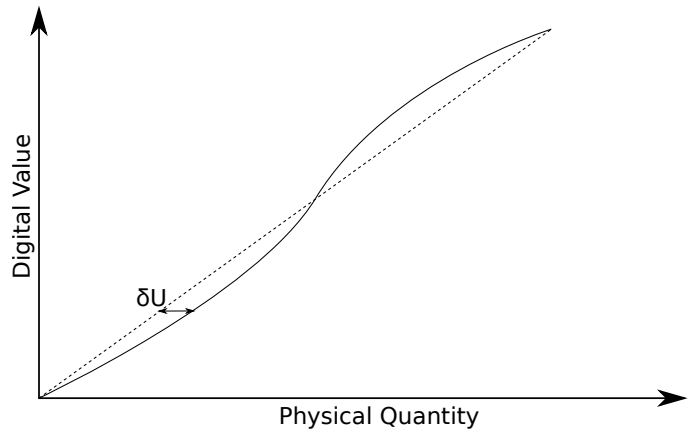
Converter Errors: Differential Non linearity



- Ideal converter characteristics: Identical Bin size over whole ADC/TDC characteristics
- Variation of bin size is called differential non linearity
- Quantified by deviation from ideal bin size δU_{DNL}

Introduction

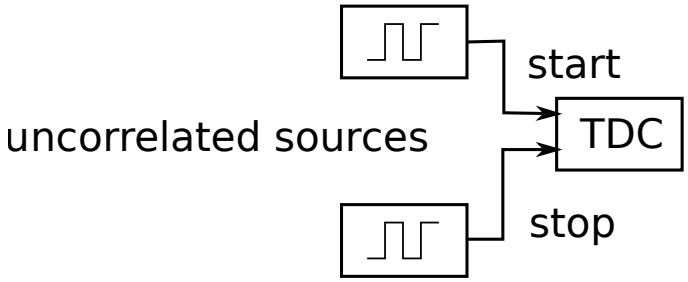
Converter Errors: Integral Non linearity

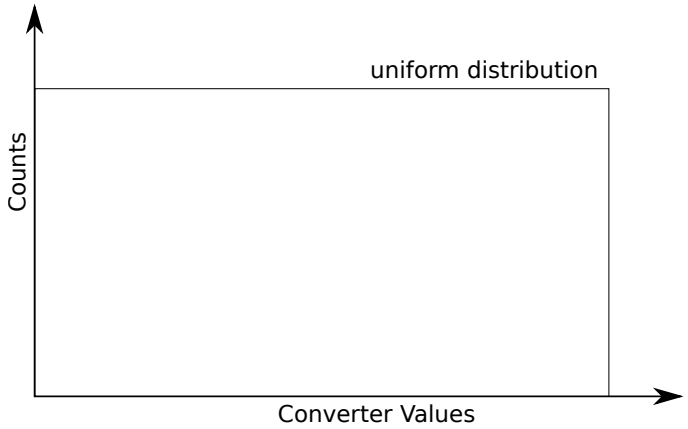


- Ideal converter characteristics: Linear relation between physical quantity and digital value
- Deviation from linear relation is called integral non linearity
- Quantified by deviation δU_{INL} or relative deviation $\delta U_{INL}/U$

Introduction

Linearity Test





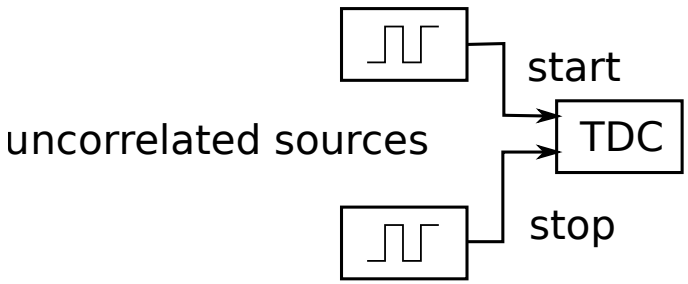
Linearity test setup:

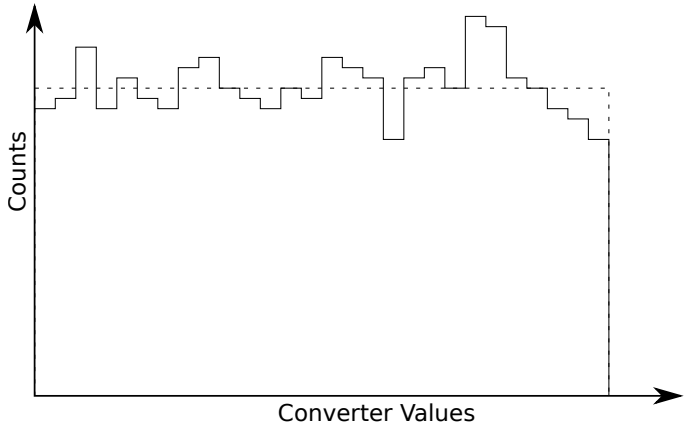
- Feed converter with uniform distributed input
- E.g. for TDC use uncorrelated sources for start and stop/reference
- Construct a histogram with all converter values
- For ideal converter histogram should be uniform distributed

$$n_i = \frac{\Delta U}{U_{max} - U_{min}} N \qquad (2)$$

Introduction

Linearity Test





Linearity test setup:

- With real converter ⇒ non-uniform distribution

$$n_i = \frac{\Delta U + \delta U}{U_{max} - U_{min}} N \quad (3)$$

$$= \bar{n} + \frac{\delta U}{U_{max} - U_{min}} N \quad (4)$$

- Differential non linearity can be determined from distribution:

$$\delta U_{DNL,i} = (n_i - \bar{n}) \frac{U_{max} - U_{min}}{N} \quad (5)$$

Introduction

Linearity Test

- Integral non linearity by summation of differential non linearities:

$$\delta U_{INL}(k\Delta U) = \sum_{i=0}^{k} \delta U_i \tag{6}$$

- If non linearities are stable in time $\delta U_{INL}(k\Delta U)$ can be used as correction function

Introduction I

Resolution, Trueness and Precision

Terms Resolution, Trueness and Precision are defined in International vocabulary of metrology[BiPM et al., 2008]. They are often used wrong.

1. Trueness:
   [BiPM et al., 2008], 2.14: closeness of agreement between the average of an infinite number of replicate measured quantity values and a reference quantity value

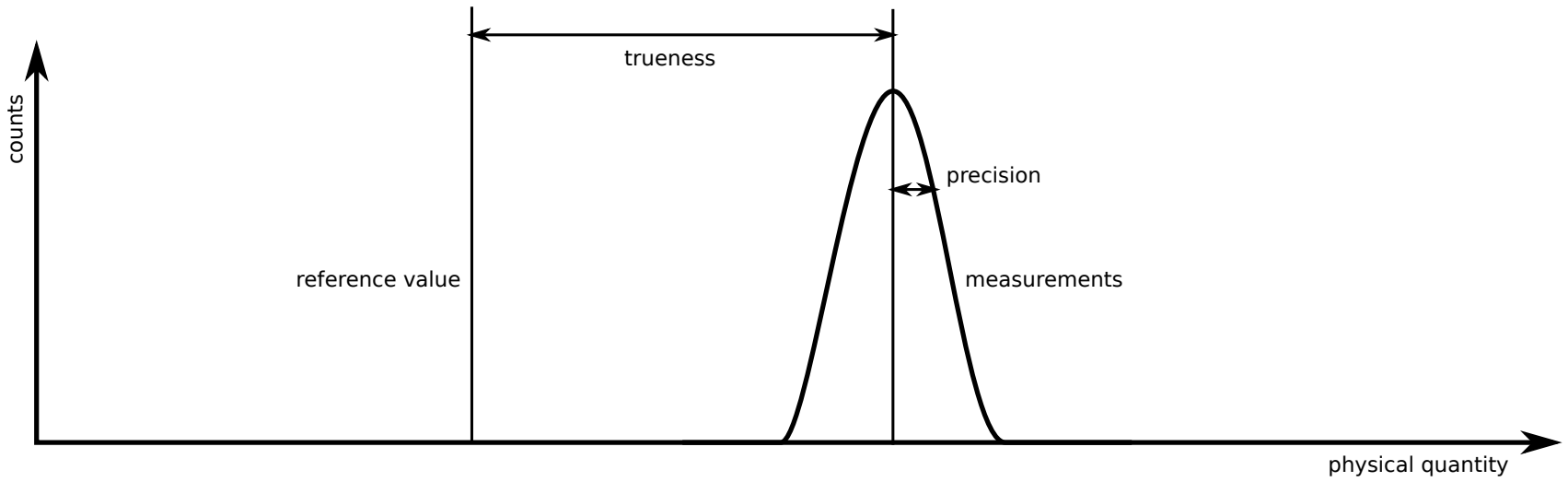
Introduction II

Resolution, Trueness and Precision

2. Precision:
   [BiPM et al., 2008], 2.15: closeness of agreement between indications or measured quantity values obtained by replicate measurements on the same or similar objects under specified conditions
3. Resolution:
   [BiPM et al., 2008], 4.14: smallest change in a quantity being measured that causes a perceptible change in the corresponding indication

Introduction III

Resolution, Trueness and Precision



Introduction

Resolution, Trueness and Precision

In case of ADC / TDC:

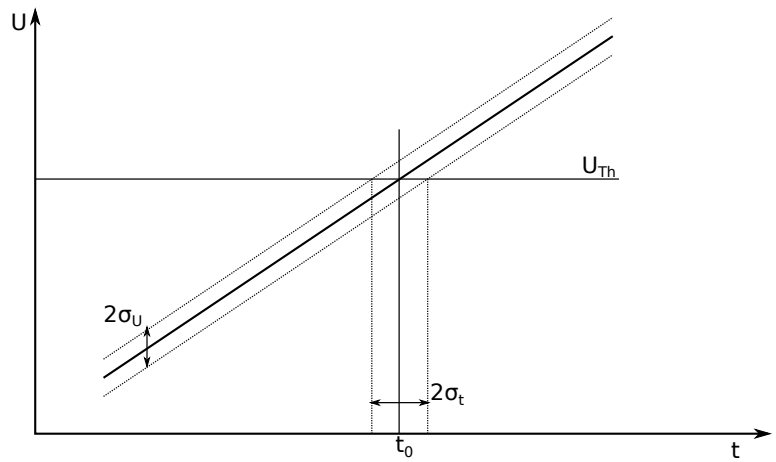
1. Resolution:
   Identical to bin size
2. Precision:

$$\begin{aligned}\sigma^2 &= <\delta^2> \\ &= \frac{1}{\Delta U}\int_0^{\Delta U}\left(t-\frac{\Delta U}{2}\right)^2 dt \\ &= \frac{1}{12}\Delta U^2\end{aligned}$$

$$\sigma = \sqrt{\frac{1}{12}}\Delta U \tag{7}$$

Introduction

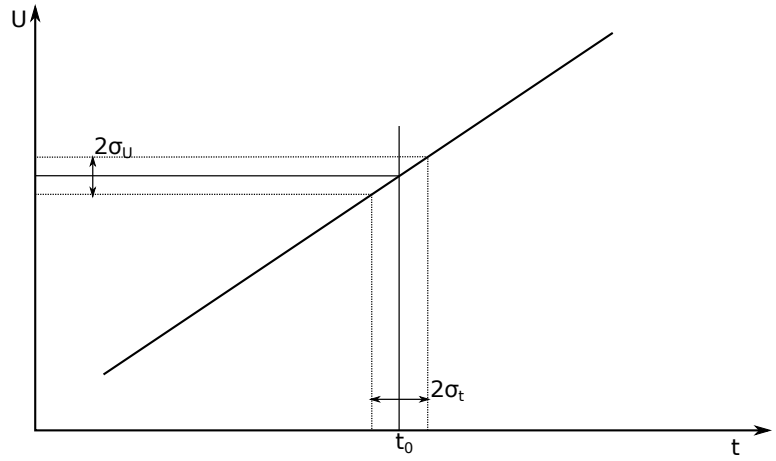
Influence of Noise on Timing Precision



- Signal noise σ_U results in timing jitter σ_t after discrimination
- $$\sigma_t = \sigma_U \cdot \left(\frac{dU}{dt}\right)^{-1} \quad (8)$$

Introduction

Influence of Clock Jitter on Amplitude Precision



- A clock jitter of an sampling ADC leads to additional noise

$$\sigma_U = \sigma_t \cdot \frac{dU}{dt} \qquad (9)$$

- Required clock jitter τ_{pp} for a given ADC resolution of n bits and signal frequency f

$$\tau_{pp} \leq \frac{1}{\pi f 2^n} \qquad (10)$$

Outline

Digital Signal Processing

Comparison Analogue and Digital Signal Processing

General remark to compare analogue and digital signal processing

- Many algorithms which are easy to implement digitally are difficult to implement in an analogue way or it is even impossible
- But:

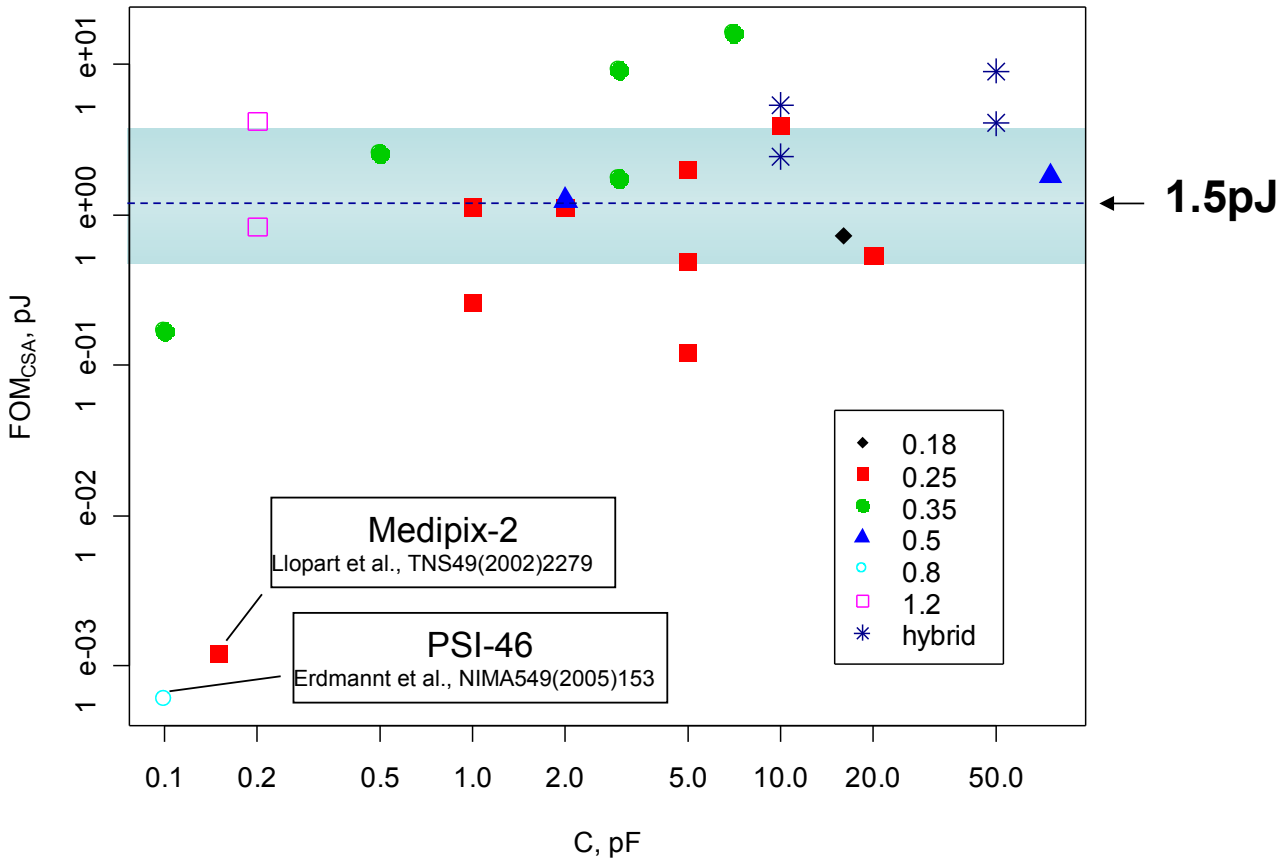
$$FOM_{CSA} = \frac{P_d \times \tau_p}{Q_{max}/\sigma_Q} \tag{11}$$

  - Express power costs of analogue CSA to achiev SNR and speed
  - Corresponds to figure of merit for analogue digital converters:

$$FOM_{ADC} = \frac{P_d}{2^{ENOB} \times f_S} \tag{12}$$

Digital Signal Processing

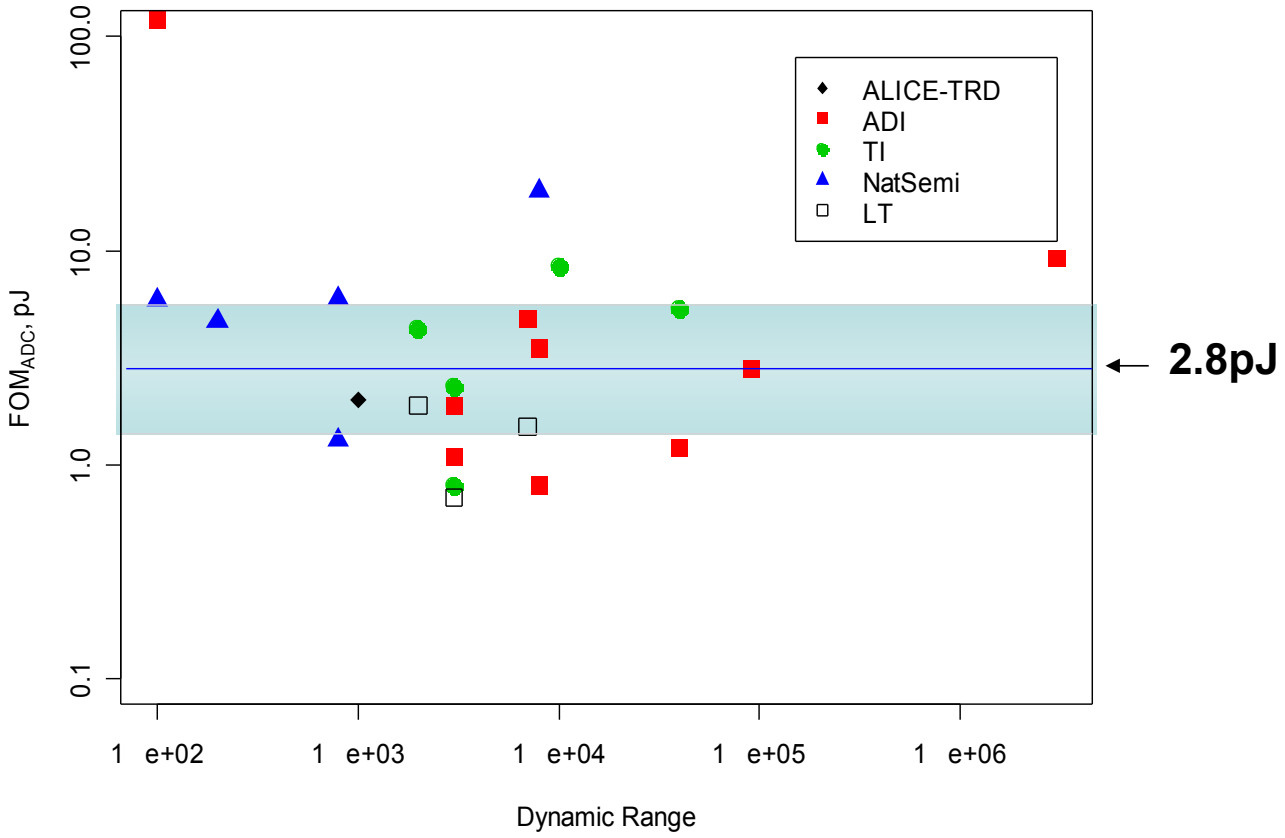
Comparison Analogue and Digital Signal Processing



[o'Conner, 2006]

Digital Signal Processing

Comparison Analogue and Digital Signal Processing



[o'Conner, 2006]

Digital Signal Processing

Effects of Quantisation

- ADC converts continuous voltage range into discrete ADC values
- Input voltage given by digital value and residual voltage

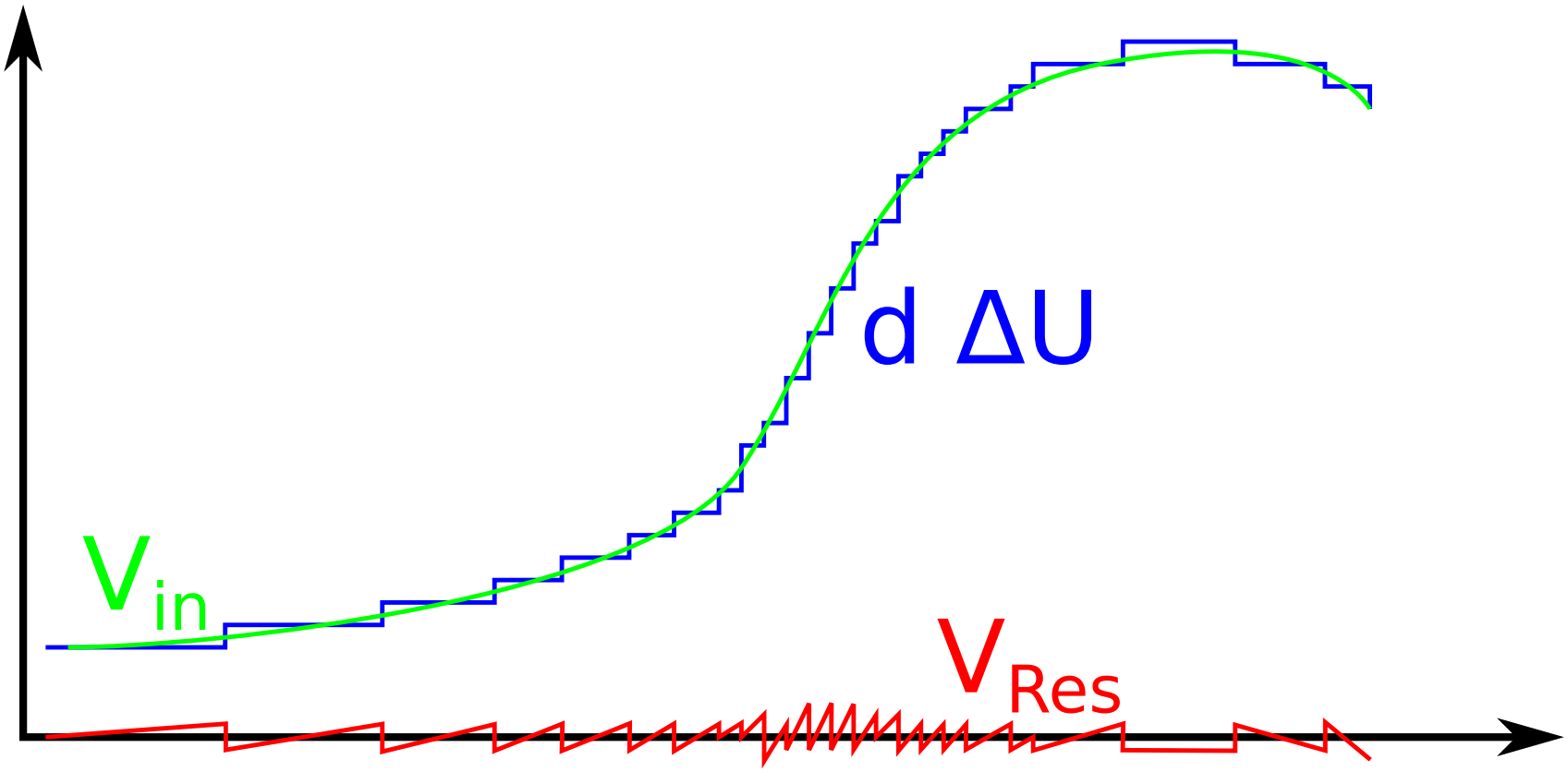
$$V_{in} = d \cdot \Delta U + V_{Res} \tag{13}$$

- $V_{Res}(t)$ is called Quantisation Noise
- RMS of Quantisation Noise:

$$\sigma_{V_{Res}} = \frac{1}{\sqrt{12}} \Delta U \tag{14}$$

Digital Signal Processing

Effects of Quantisation



Digital Signal Processing

Effects of Quantisation

- Signal to Noise Ratio:
  - Full scale input:

$$V_{pp} = 2^n \cdot \Delta U \tag{15}$$

  - In case of sine input:

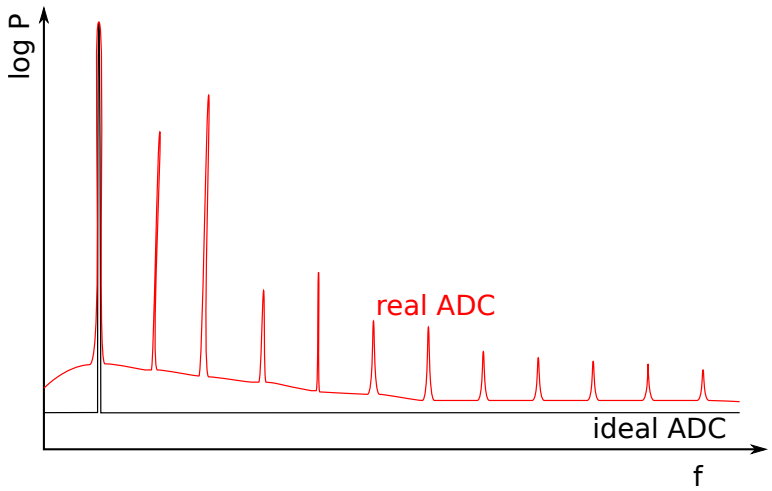
$$V_{rms} = \frac{1}{2\sqrt{2}} V_{pp} = \frac{1}{2\sqrt{2}} 2^n \cdot \Delta U \tag{16}$$

  - Signal to Noise Ratio of ideal ADC:

$$S[\mathrm{dB}] = 20 \log_{10} \frac{V_{rms}}{\sigma_{V_{Res}}} = 6.02 \cdot n + 1.76 \tag{17}$$

Digital Signal Processing

Effects of Quantisation

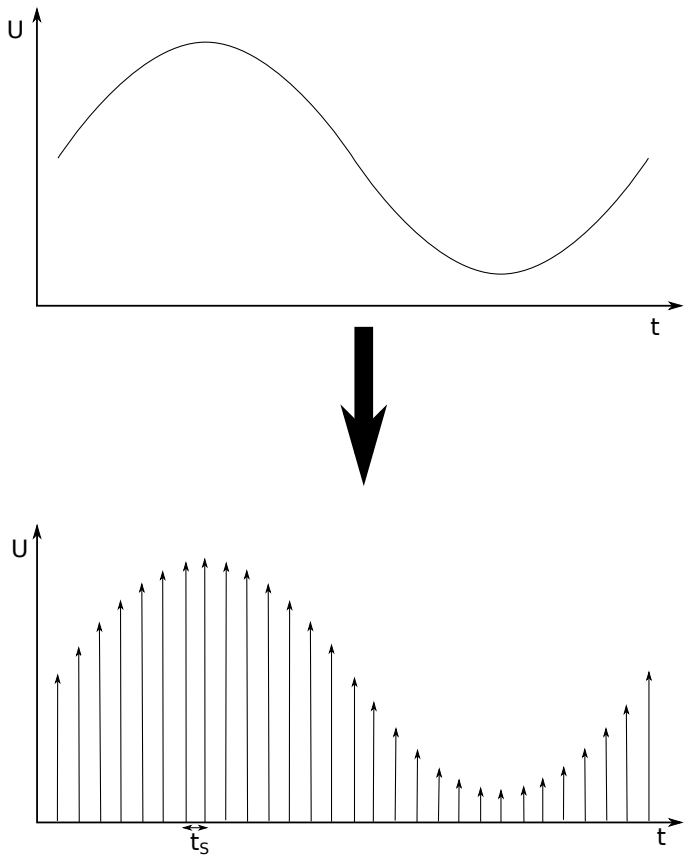


FFT of ideal and real ADC with sine input

- Real ADCs always worse than ideal ADCs
- Additional noise by electronic components
- Harmonic distortion by non linearities
- SNR reduced by noise and distortions
- Often characterised by Effective number of Bits (ENOBs)

Digital Signal Processing

Effects of Sampling



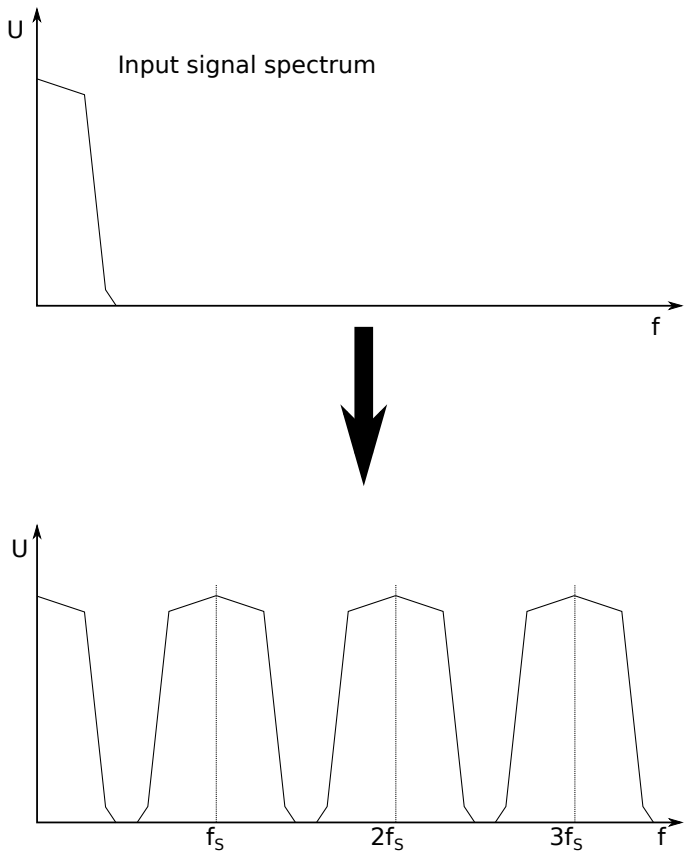
- From continuous analogue signal to time discrete samples
- Description as sequence of Dirac pulses with intensity given by signal amplitude

$$A_S(t) = \sum_{k=-\infty}^{\infty} A(kt_S)\delta(t - kt_s) \tag{18}$$

- Transformation in frequency domain by Fourier transformation

Digital Signal Processing

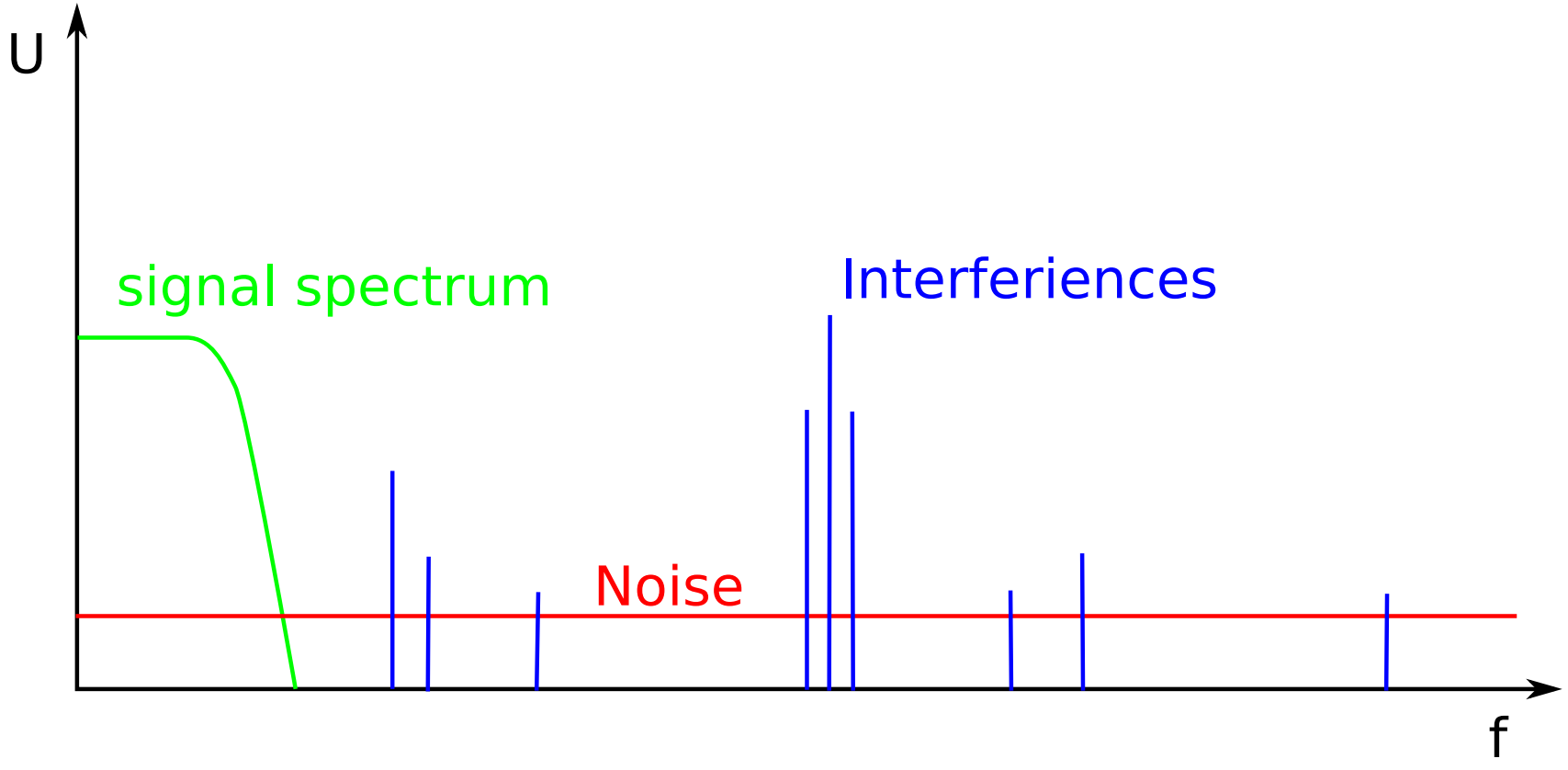
Effects of Sampling



- Spectrum periodic in $f_S = 1/t_S$
- Isolated periodic spectra if $f_{max} < f_S/2$
- Sampling theorem by C. Shannon[Shannon, 1949]

Digital Signal Processing

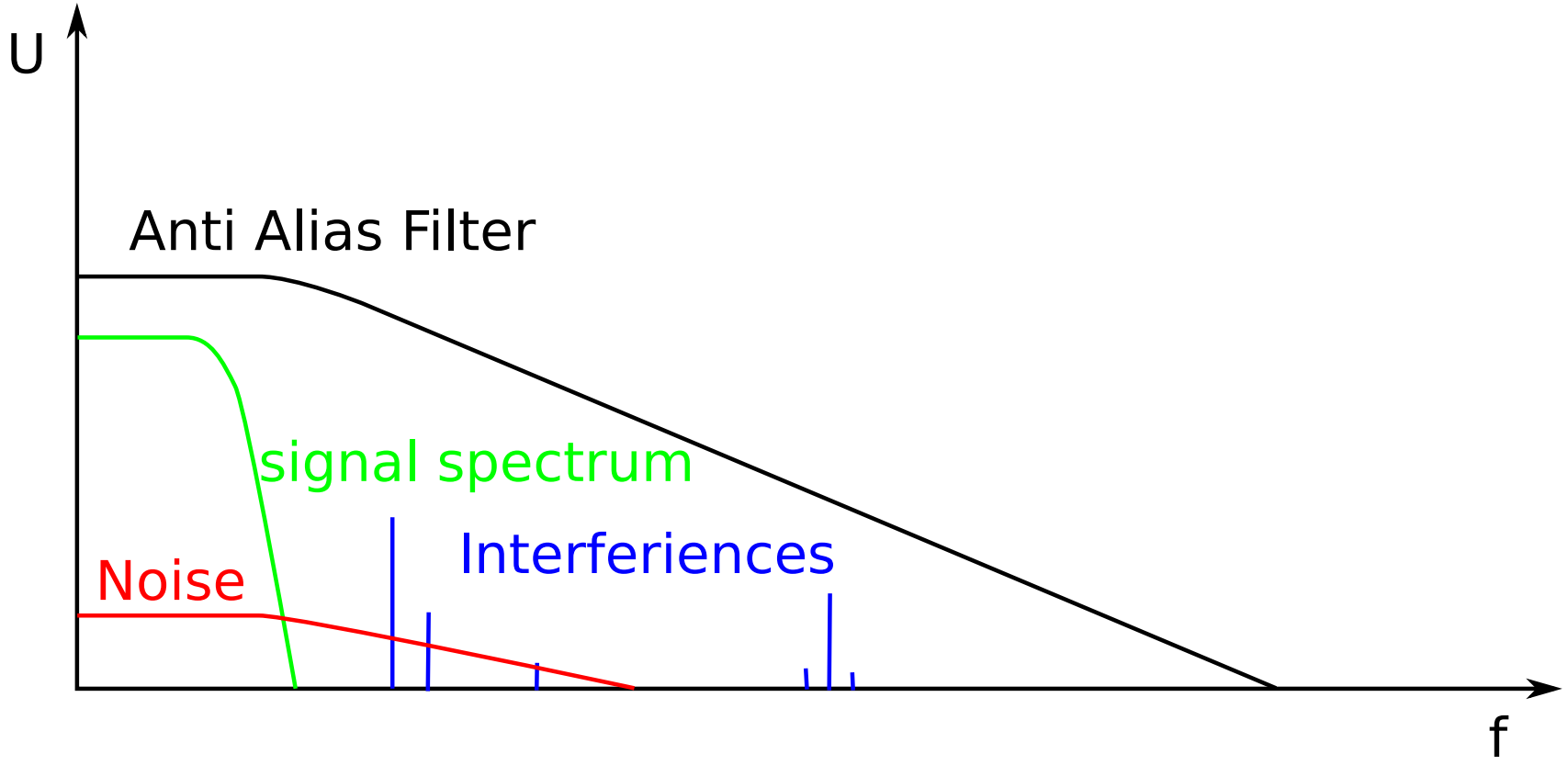
Example of Signal Digitisation



Spectrum of analogue detector signal with noise and interference

Digital Signal Processing

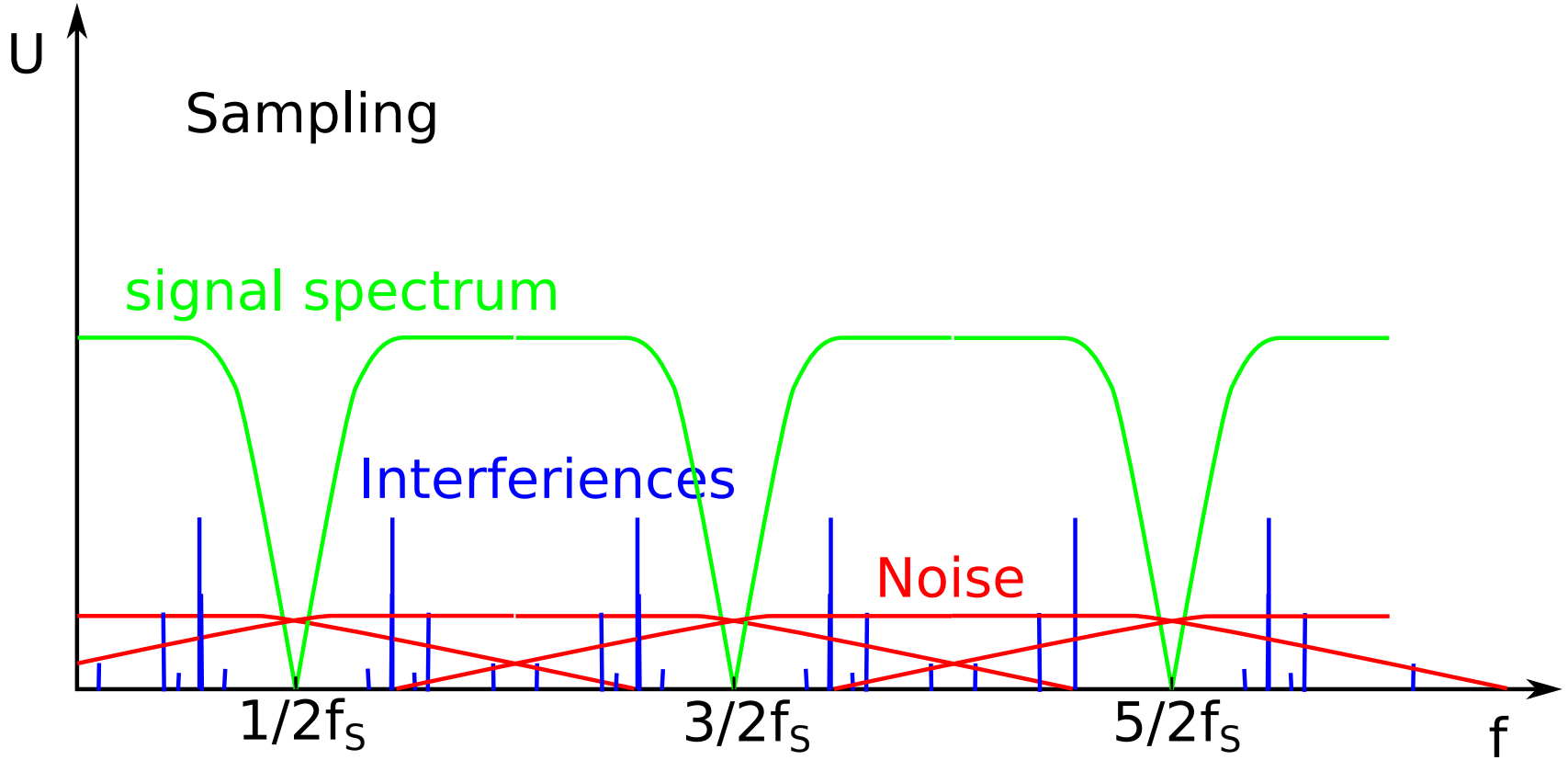
Example of Signal Digitisation



Spectrum after analogue anti alias filter

Digital Signal Processing

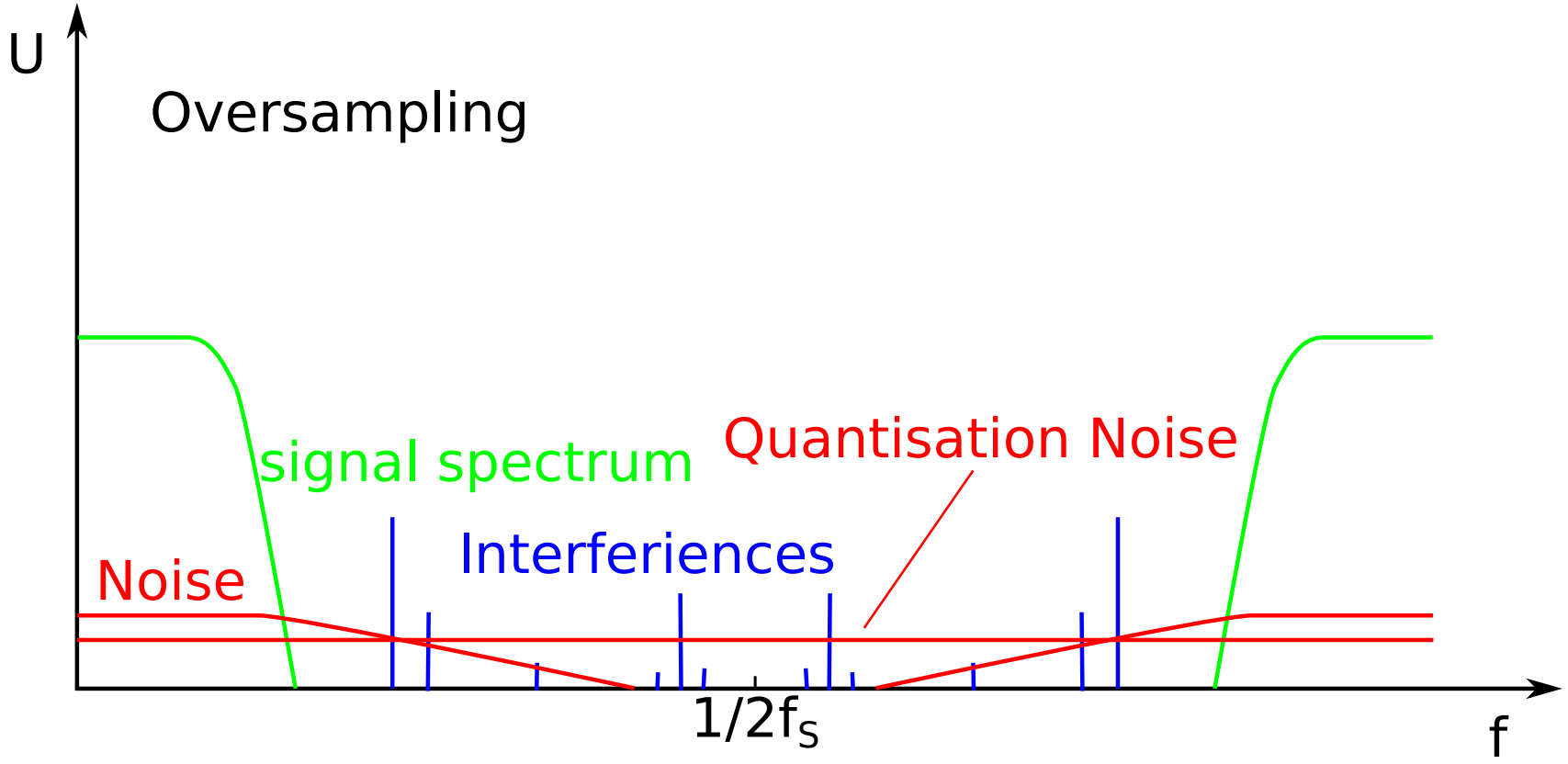
Example of Signal Digitisation



Spectrum after Sampling with minimum f_S

Digital Signal Processing

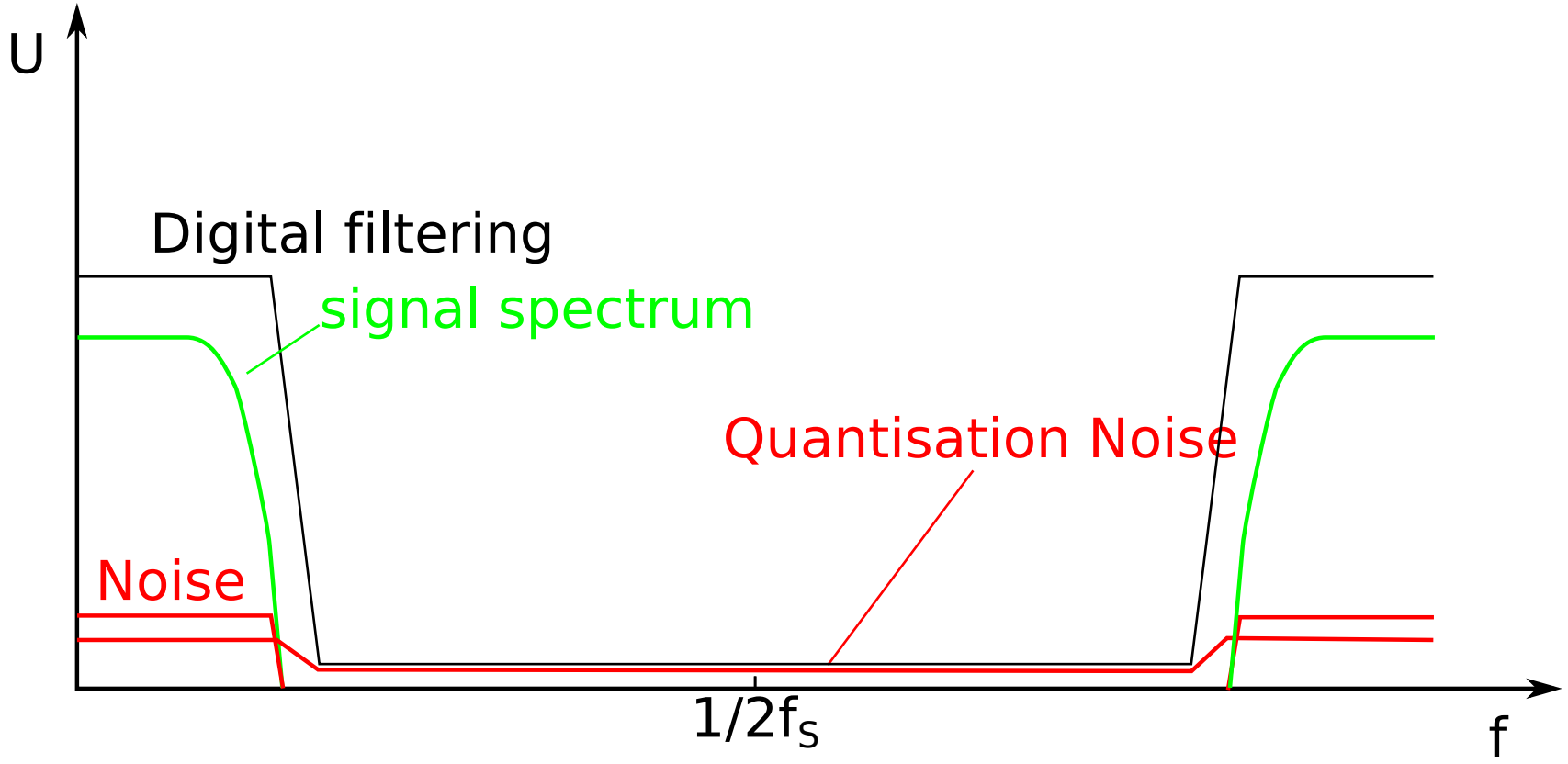
Example of Signal Digitisation



Avoiding in band interference's by oversampling

Digital Signal Processing

Example of Signal Digitisation



Noise and interference reduction by digital filtering

Outline

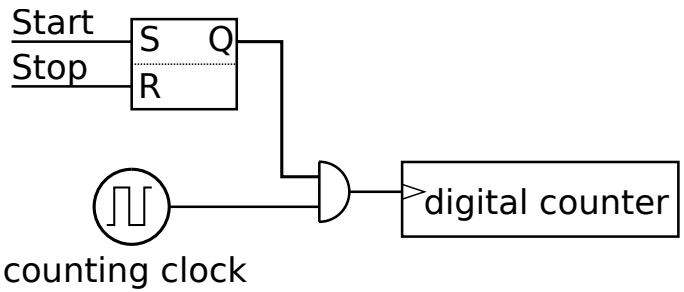
Time to Digital Converter

Task of a Time to Digital Converter (TDC) is
Measure and digitise time interval between

- a start and a stop signal (relative time measurement) or
- an input signal and the next edge of a reference clock signal (absolute time measurement)

Time to Digital Converter

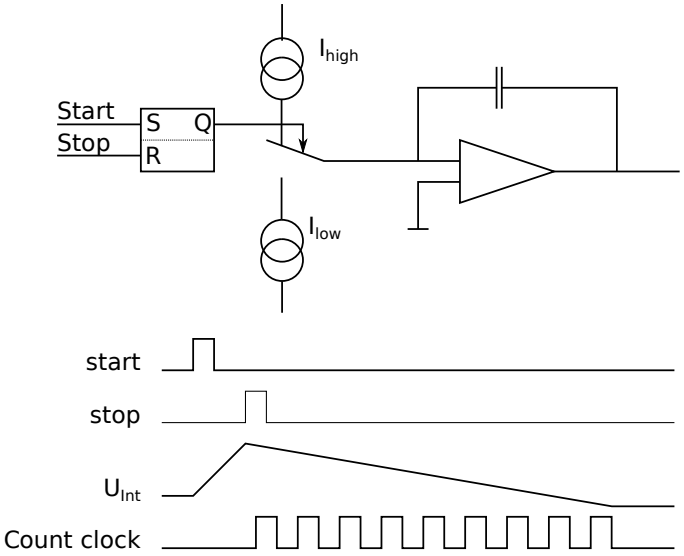
Counter



- Very simple design
- Resolution directly connected to counting clock
- Good resolution requires large frequencies
- practical limit O(1 GHz) $\Rightarrow$ $\tau_{bin} = 1$ ns
- Design Example: [Gao and Partridge, 1991]

Time to Digital Converter

Time to Amplitude converter: Dual Slope



- Improvement of counter TDC by time stretching
- Charging of integrator with high current during start-stop interval
- Discharging with low current afterwards
- Time measurement during discharging phase with counter-TDC

Time to Digital Converter

Time to Amplitude converter: Dual Slope

Pros:

- Simple design
- Low power consumption

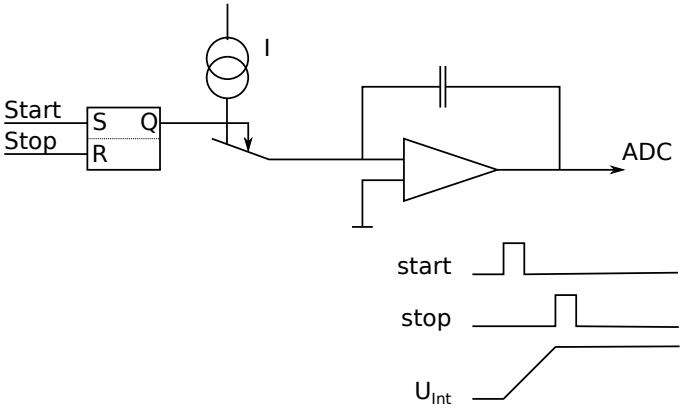
Cons:

- Long dead time during discharging phase
- Non-Linearities due to non ideal current sources and integrator
- **P**rocess, **V**oltage and **T**emperatur variations

Design Example: [Chen et al., 2006, Kim et al., 2011]

Time to Digital Converter

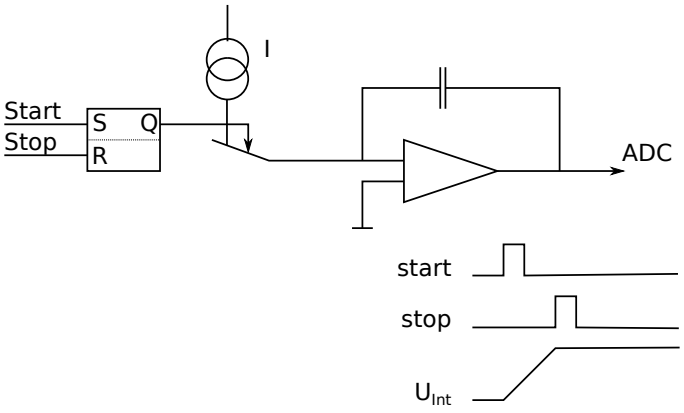
Time to Amplitude converter: Single Slope



- Discharging and Counter replaced by ADC
- More complex (ADC required)
- In case of fast ADC dead time reduced
- Design Example: [Rolo et al., 2012]

Time to Digital Converter

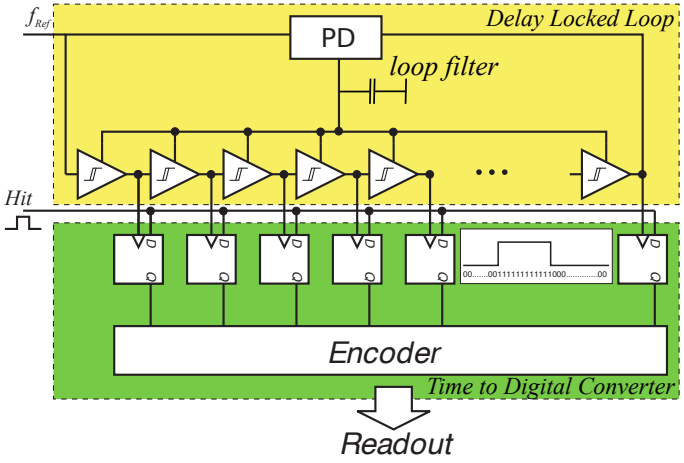
Time to Amplitude converter: Dual Slope



- Optional architecture: Delay chain based
- Can be stabilised with DLL to compensate PVT variations
- Precision better than 10 ps feasible
- Design Example: [Koch et al., 2005, Flemming and Deppe, 2007]

Time to Digital Converter

PLL or DLL based TDCs



- Self calibrating due to closed loop, calibrates PVT variations
- Total delay of delay chain equal to clock cycle time
- Time bin τ_{bin} corresponds to delay of one delay element:

$$\tau_{bin} = \frac{1}{N} T_{cyc} \qquad (19)$$

Time to Digital Converter

PLL or DLL based TDCs

Pros:

- Full digital architecture
- No offline calibration needed
- Very good multi hit resolution
- Low dead time
- High rate capability

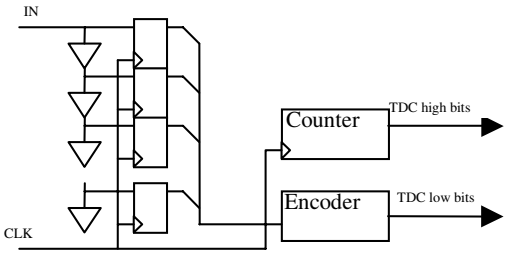
Cons:

- Minimum τ_{bin} limited by technology node e.g. $\tau_{bin} = 50 \ldots 60$ ps for 180 nm CMOS
  $\Rightarrow$ Improvement by time interpolation with passive RC networks[Mota and Christiansen, 1999]

Design Example:
[Deppe and Flemming, 2009, Perktold and Christiansen, 2013]

Time to Digital Converter

FPGA Tapped Delay Line TDCs



[Wu et al., 2003]

- Full digital logic implemented in **F**ield *P*rogrammable **G**ate **A**rrays
- Fast structures e.h. carry chains used as delay line
- Sensitive to PVT variations: calibration required
- Very bad DNL
- Precision improvement by multi edge sampling[Bayer and Traxler, 2011]

Outline

Analogue to Digital Converter

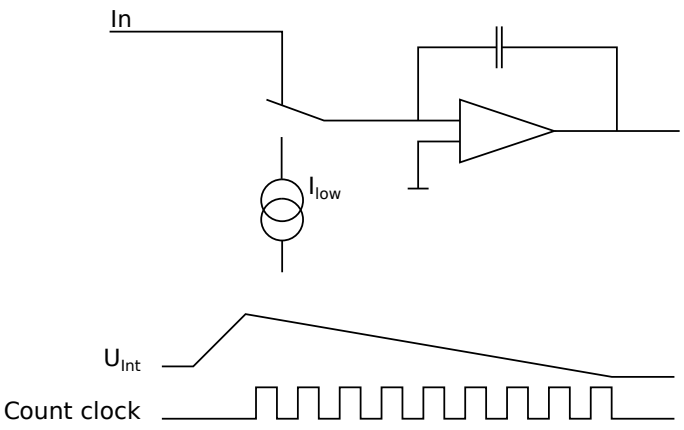
Time Over Threshold Measurement

Using a CR-RC^n pulse shaper and a time-over-threshold discriminator and measure the pulse width with a TDC

- Very simple design
- Non linear
- high resolution requires long shaping times $\Rightarrow$ long dead time
- Used in many application with modest dynamic range and linearity requirements

Analogue to Digital Converter

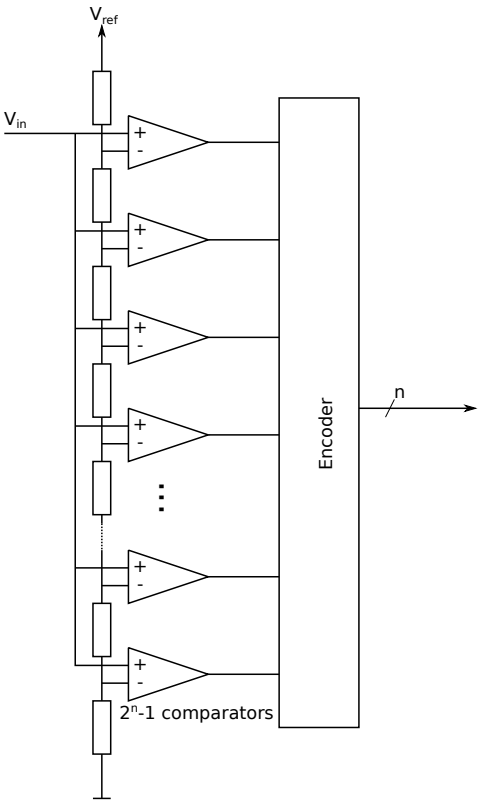
Wilkinson ADC



- Modification of Dual Slope TDC, Analogue to time converter and counter
- Large dynamic range, good precision
- Extremly slow
- Design Example for ILC: [Bouchel et al., 2007]

Analogue to Digital Converter

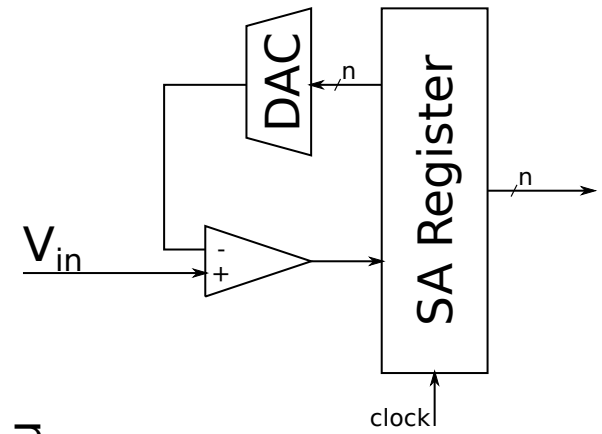
Flash ADC

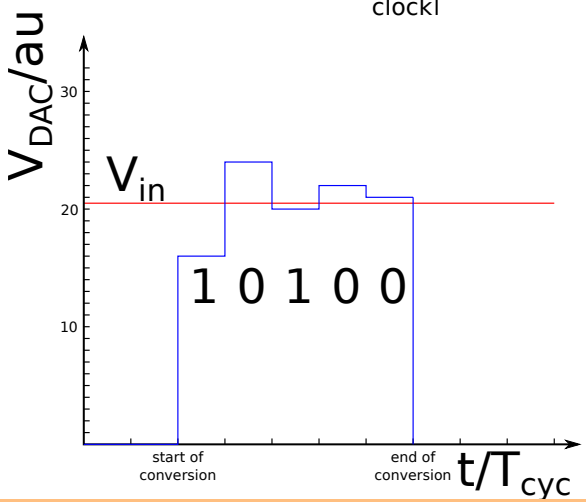


- Operation of $2^n - 1$ comparators in parallel
- Very fast
- Increase of dynamic range requires exponentially increasing number of comparators
- Large power and area consumption

Analogue to Digital Converter

Successive Approximation ADC

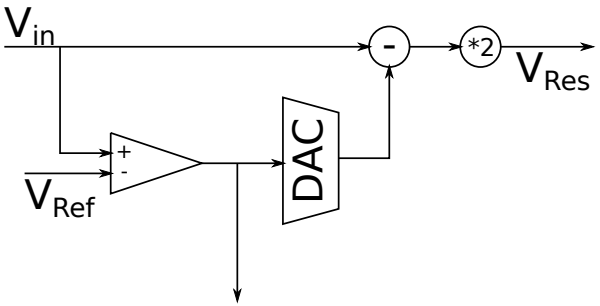




- Bit wise approximation of input voltage with DAC voltage
- *n* clock cycles for *n* bits
- Slower than flash ADC but less circuit complexity and less power consumption
- Linearity defined by DAC

Analogue to Digital Converter

Pipeline ADC



Single stage of a Pipeline ADC

- k-bit digitisation per stage
- In case of $k = 1$

$$V_{in} = d \cdot V_{Ref} + \frac{1}{2} V_{Res} \qquad (20)$$

- Second stage:

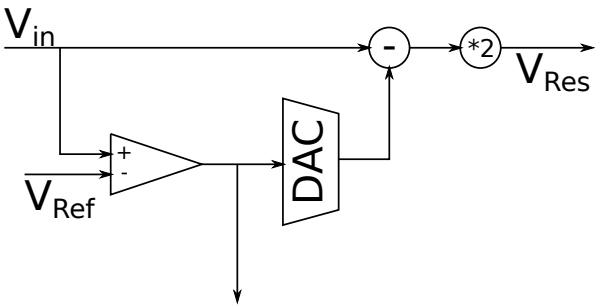
$$V_{in} = d_1 \cdot V_{Ref} + \frac{1}{2} d_2 \cdot V_{Ref} + \frac{1}{4} V_{Res} \qquad (21)$$

- n-Stages:

$$V_{in} = \sum_{i=1}^{n} \frac{1}{2^{i-1}} d_i \cdot V_{Ref} + \frac{1}{2^n} V_{Res} \qquad (22)$$

Analogue to Digital Converter

Pipeline ADC



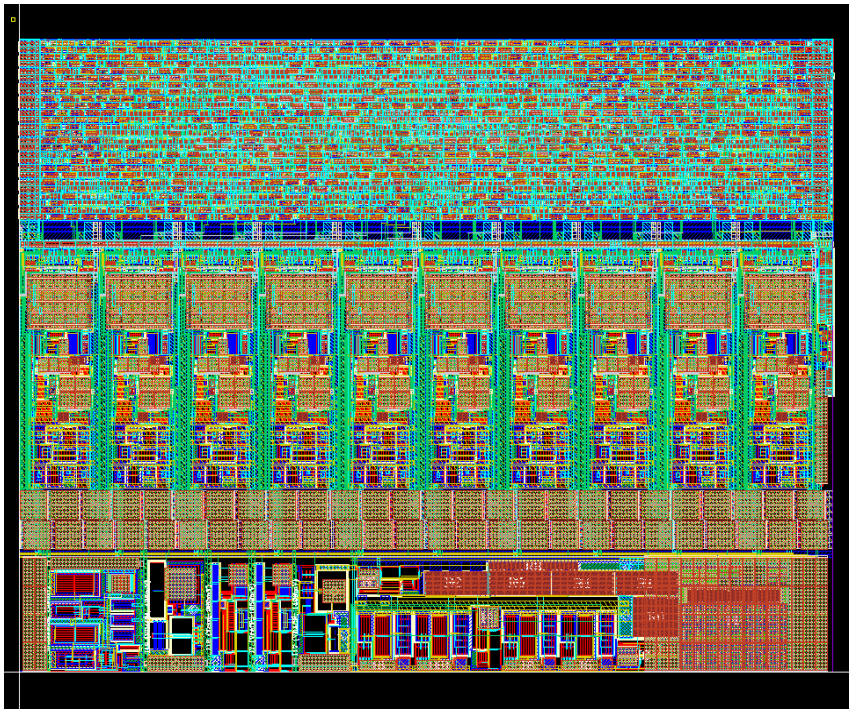
Single stage of a Pipeline ADC

- One ADC value per clock cycle
- Latency of *n* clock cycles
- High dynamic range and clock frequency possible
- Medium circuit complexity but very high demand on matching
- DNL depends extremely on amplification factor

⇒ In practice: Digital calibration

Analogue to Digital Converter

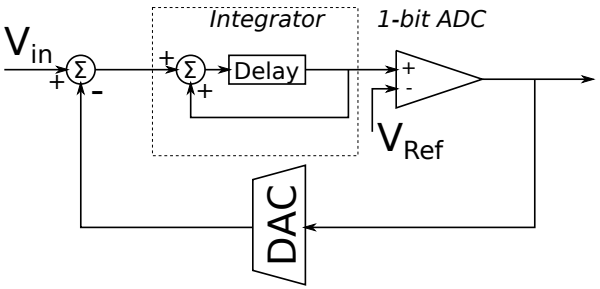
Pipeline ADC



Design Example: 12 Bit Pipeline ADC with 10 + 1 stages and digital calibration unit on the top side.

Analogue to Digital Converter

Oversampling



A first-order sigma-delta modulator [Boyce et al., 1998]

- For signal bandwidth F the minimum sampling rate is Nyquist frequency $f_N = 2F$
- Concept of oversampling ADCs: gain in dynamic range by $f_S \gg f_N$
- Simple analogue design due to 1-bit ADC and DAC
- Digital signal processing is used to filter out of band quantisation noise
- Example of sigma-delta-ADC in CMOS-Pixel: [Fowler et al., 1994]

Outline

Bayer, E. and Traxler, M. (2011). A high-resolution ($lt; 10$ *rmps* rms) 48-channel time-to-digital converter (tdc) implemented in a field programmable gate array (fpga). *IEEE Transactions on Nuclear Science*, 58(4):1547–1552.

BiPM, I., IFCC, I., ISO, I., and IUPAP, O. (2008). International vocabulary of metrology–basic and general concepts and associated terms, 2008. *JCGM*, 200:99–12.

Bouchel, M., Dulucq, F., Fleury, J., de La Taille, C., Martin-Chassard, G., and Raux, L. (2007). Spiroc (sipm integrated read-out chip): Dedicated very front-end electronics for an ilc prototype hadronic calorimeter with sipm read-out. In *2007 IEEE Nuclear Science Symposium Conference Record*, volume 3, pages 1857–1860.

Boyce, D. E., Li, H. W., and Baker, R. J. (1998). *CMOS Circuit Design, Layout, and Simulation*. IEEE Press.

Chen, P., Chen, C. C., and Shen, Y. S. (2006). A low-cost low-power cmos time-to-digital converter based on pulse stretching. *IEEE Transactions on Nuclear Science*, 53(4):2215–2220.

Deppe, H. and Flemming, H. (2009). The gsi event-driven tdc with 4 channels get4. In *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, pages 295–298.

Flemming, H. and Deppe, H. (2007). Development of high resolution tdc asics at gsi. In *2007 IEEE Nuclear Science Symposium Conference Record*, volume 1, pages 322–325.

Fowler, B., Gamal, A. E., and Yang, D. X. D. (1994). A cmos area image sensor with pixel-level a/d conversion. In *Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International*, pages 226–227.

Gao, G. S. and Partridge, R. (1991). High speed digital tdc for d0 vertex reconstruction. *IEEE Transactions on Nuclear Science*, 38(2):286–289.

Kim, M., Lee, H., Woo, J. K., Xing, N., Kim, M. O., and Kim, S. (2011). A low-cost and low-power time-to-digital converter using triple-slope time stretching. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 58(3):169–173.

Koch, K., Hardel, H., Schulze, R., Badura, E., and Hoffmann, J. (2005). A new tac-based multichannel front-end electronics for tof experiments with very high time resolution. *IEEE Transactions on Nuclear Science*, 52(3):745–747.

Mota, M. and Christiansen, J. (1999). A high-resolution time interpolator based on a delay locked loop and an rc delay line. *IEEE Journal of Solid-State Circuits*, 34(10):1360–1366.

o'Conner, P. (2006). Noise and power tradeoffs in cmos front ends. Presented at VIth International Meeting on Front End Electronics FEE2006, Perugia, Italy.

Perktold, L. and Christiansen, J. (2013). A fine time-resolution ($<$ 3 ps-rms) time-to-digital converter for highly integrated designs. In *2013 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, pages 1092–1097.

Rolo, M. D., Bugalho, R., Gonçalves, F., Rivetti, A., Mazza, G., Silva, J. C., Silva, R., and Varela, J. (2012). A 64-channel asic for tofpet applications. In *2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC)*, pages 1460–1464.

Shannon, C. E. (1949). Communication in the presence of noise. *Proceedings of the IRE*, 37(1):10–21.

Wu, J., Shi, Z., and Wang, I. Y. (2003). Firmware-only implementation of time-to-digital converter (tdc) in field-programmable gate array (fpga). In *2003 IEEE Nuclear Science Symposium. Conference Record (IEEE Cat. No.03CH37515)*, volume 1, pages 177–181 Vol.1.