PANDA Lecture Week
Introduction into Front End Electronics
Part I: Basics

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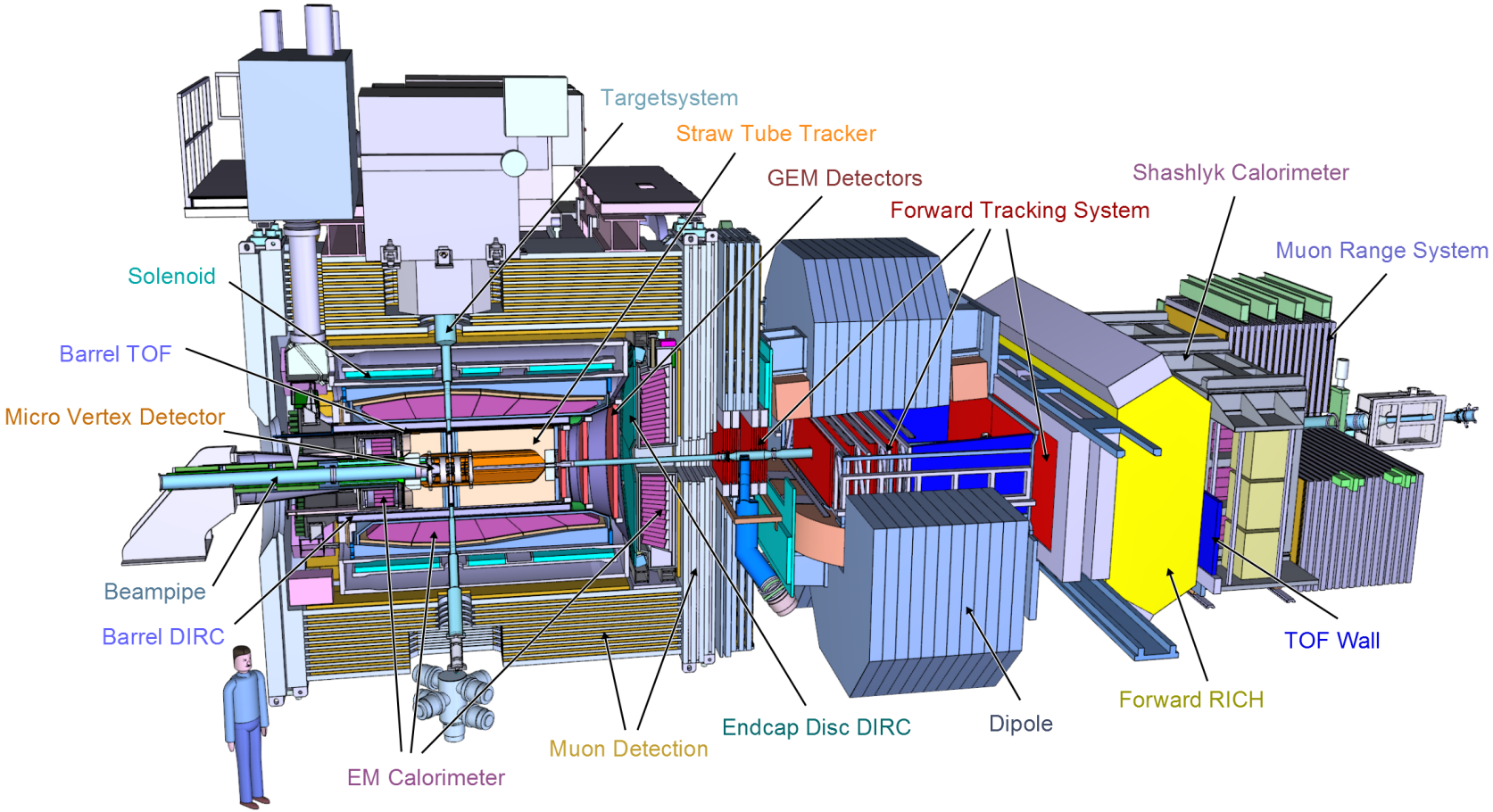
Outline

1. Motivation
2. Reminder of Semiconductor Physics
3. The MOS Transistor
4. MOS Transistor stages
5. CMOS Scaling and Future Technologies
6. Literature

Motivation


Targetsystem
Straw Tube Tracker
GEM Detectors
Shashlyk Calorimeter
Forward Tracking System
Muon Range System
Solenoid
Barrel TOF
Micro Vertex Detector
Beampipe
Barrel DIRC
TOF Wall
Forward RICH
Dipole
Endcap Disc DIRC
Muon Detection
EM Calorimeter

Motivation

Why being concerned with electronics?

- Getting physics data requires detectors
- detector readout done by electronics
- Front end electronics defines detectors performance
  - Noise
  - Precision
  - Dynamic range
  - Ageing, Radiation damage
- It is fascinating and challenging
- You might enjoy it!

Motivation I

Structure of these Lectures:

1. Basics
   - Basic theory which is needed for understanding
   - Outlook: Future technologies, CMOS scaling
2. Charge Sensitive Amplifier and Noise
   - Noise sources
   - Degrees of freedom for noise optimisation
   - Outlook: Noise performance with CMOS scaling
3. Radiation effects
   - Total ionising dose effects
   - Single event effects
   - Mitigation

Motivation II

4. TDCs and ADCs
   - Basic theory of Conversion
   - Basics on Digital signal processing
   - TDC and ADC architectures

Outline

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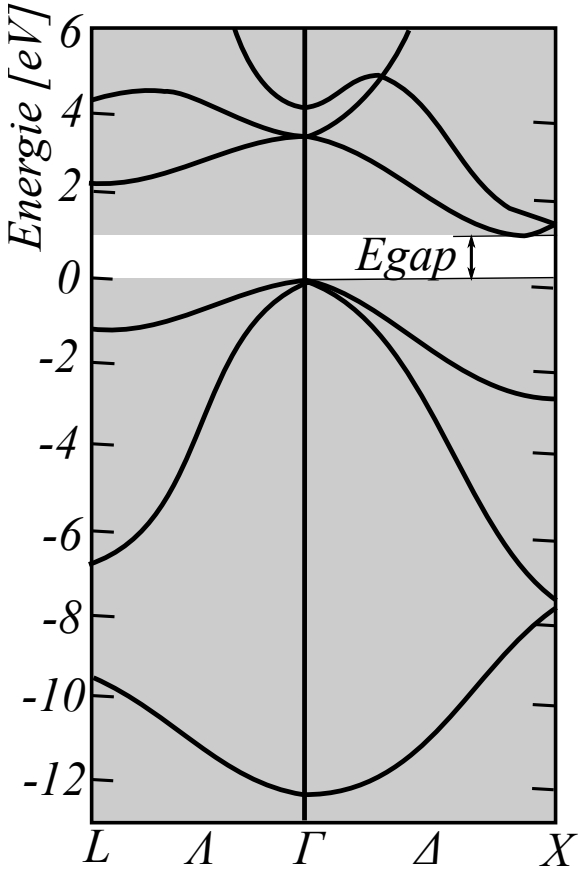
Reminder of Semiconductor Physics

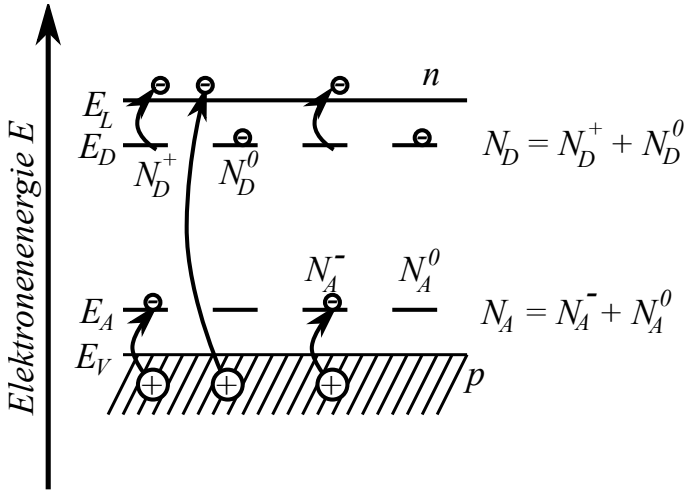


Structure of energy bands of silicon[Chelikowsky and Cohen, 1976]

- Semiconductors: Crystals with energy gap in the order of 1 eV
- Often used semiconductors: germanium, silicon, GaAs
- Silicon: $E_{gap} = 1.12$ eV (@ 300 K)
- Standard text book: [Sze, 1981]

Reminder of Semiconductor Physics

Doping

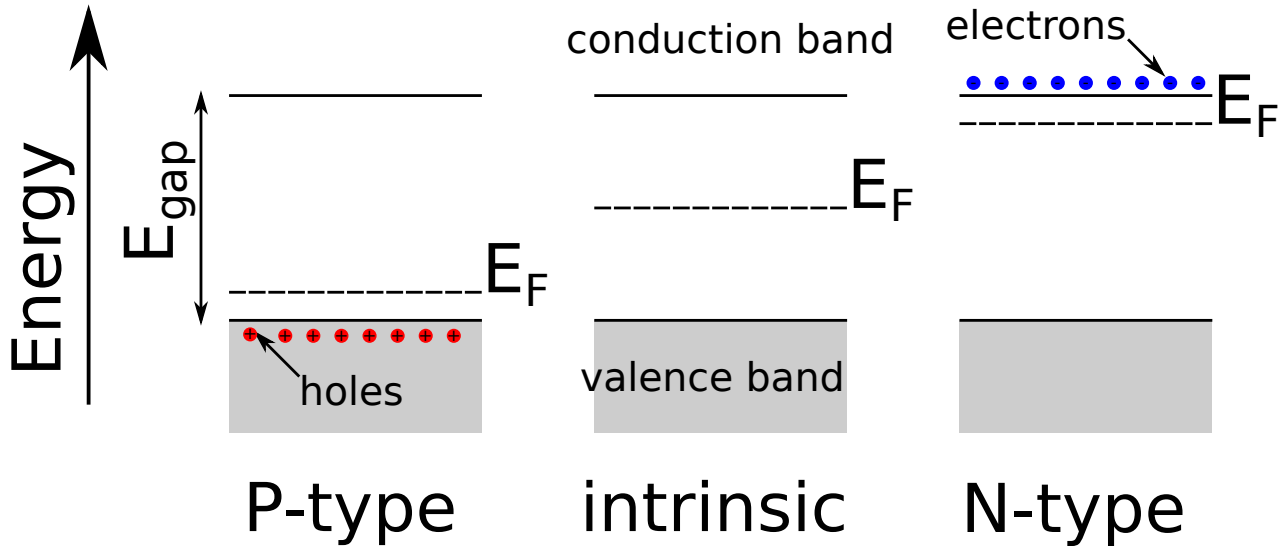


Charge carrier and doping[Ibach and Lüth, 1999]

- Very low charge carrier density in undoped semiconductor ⇒ nearly insulator
- Charge carrier density strongly depends on doping
- V-group elements (N, P, As) ⇒ generate free electrons ⇒ N-type semiconductor
- III-group elements (B, Ga) ⇒ generate free holes ⇒ P-type semiconductor

Reminder of Semiconductor Physics

Semiconductor Types and Fermi Level



$$n_p = n_i \exp\left(\frac{-q\Psi_B}{kT}\right) \quad (1) \qquad n_n = n_i \exp\left(\frac{q\Psi_B}{kT}\right) \quad (2)$$

With P- and N-Type charge carrier concentration n_p, n_n, $q\Psi_B = E_F - E_I$ and intrinsic Fermi level E_I.

Outline

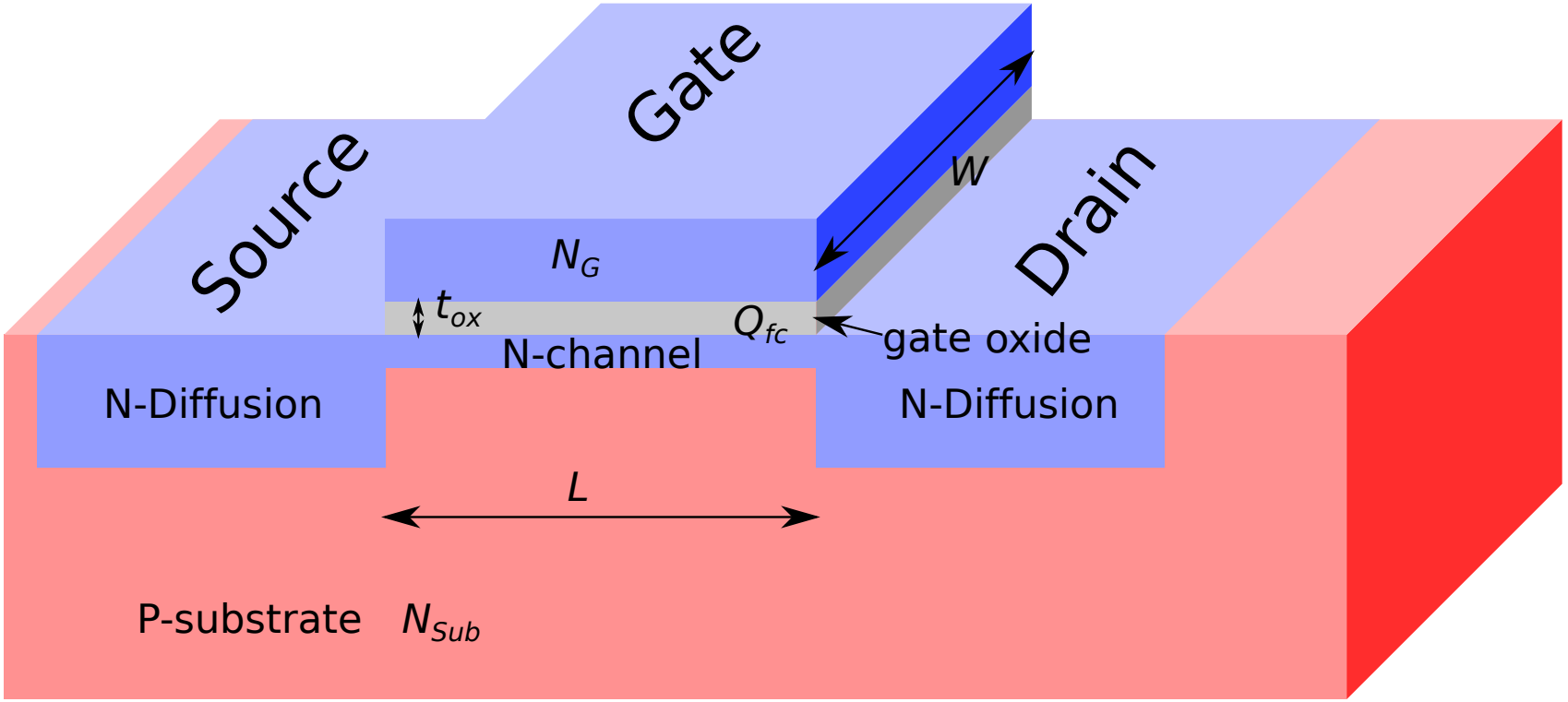
1 Motivation

2 Reminder of Semiconductor Physics

3 The MOS Transistor
- The Metal Insulator Semiconductor (MIS) Diode
- Operation Modes
- Small Signal Model
- Noise

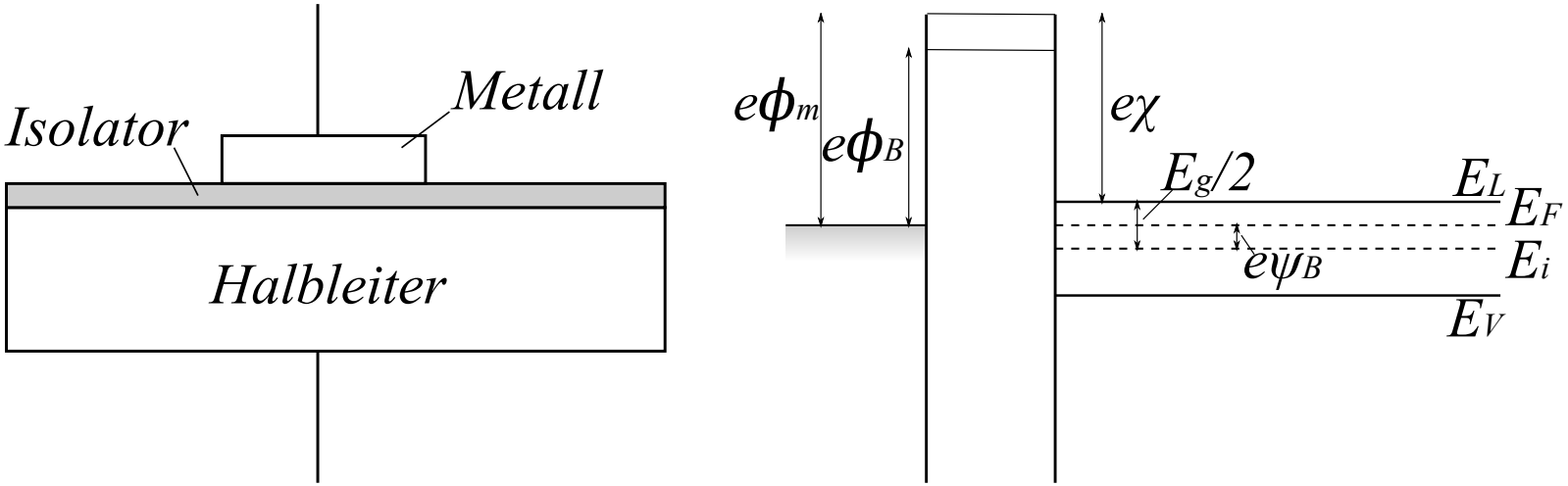
4 MOS Transistor stages

The MOS Transistor



The MOS Transistor

The Metal Insulator Semiconductor (MIS) Diode



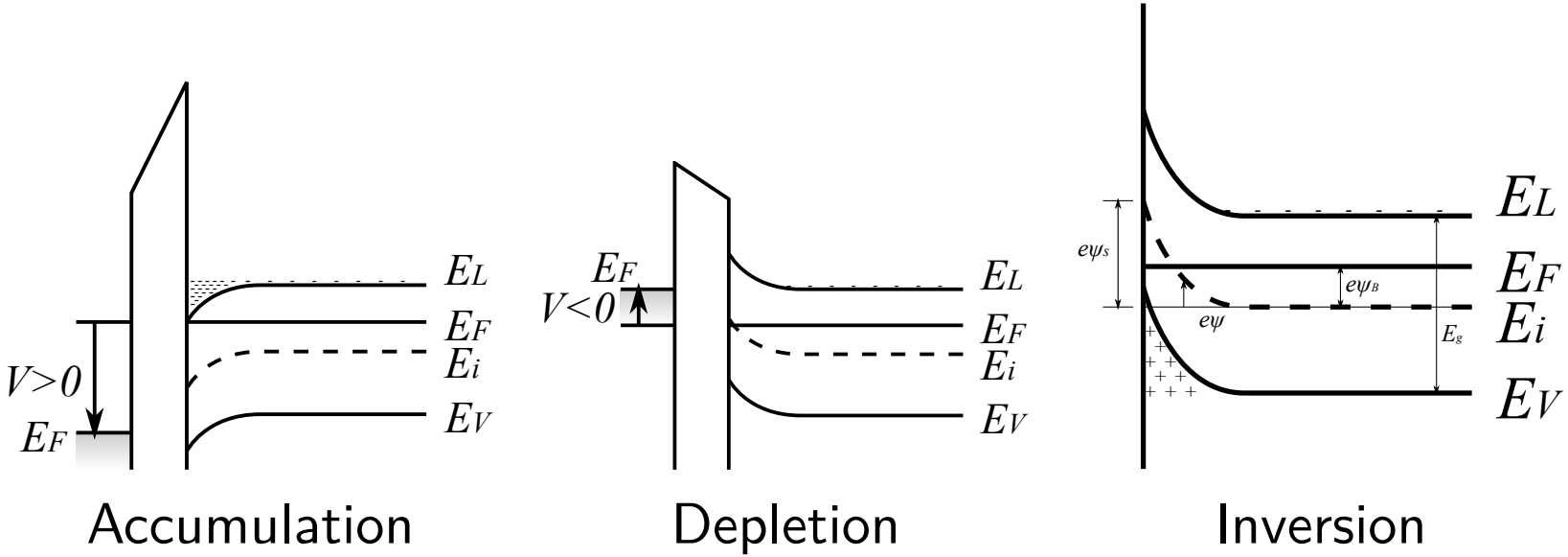
Cross section of a metal insulator semiconductor diode and band structure.

ϕ_m	work function (metal)	ϕ_B	potential barrier
χ	work function (sem.)	E_g	band gap
E_F	Fermi level	E_i	intrinsic Fermi level

The MOS Transistor

The Metal Insulator Semiconductor (MIS) Diode

MIS diode with external voltage:



The MOS Transistor

Capacitances in the MOS Transistor

- Gate-Channel Capacitance

$$C_{GC} = WLC_{ox} \tag{3}$$

with

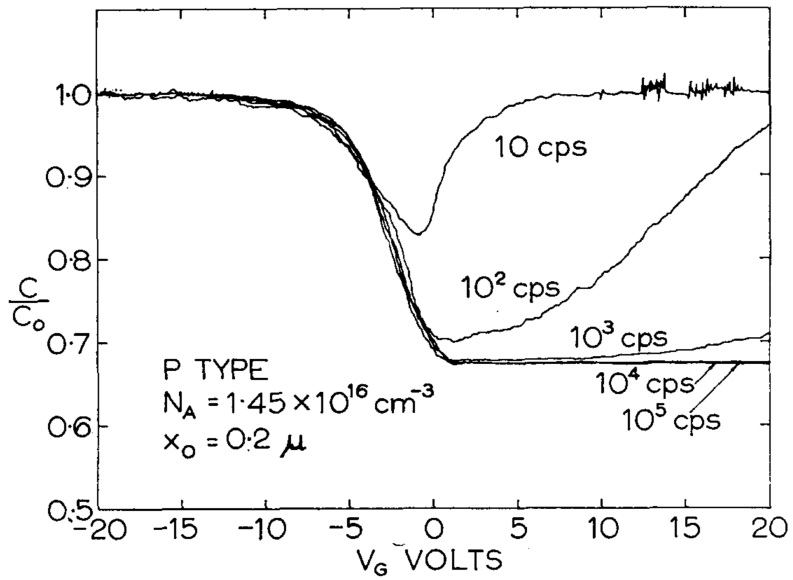
$$C_{ox} = \frac{\epsilon_0 \epsilon_{r_{SiO_2}}}{t_{ox}} \tag{4}$$

$\epsilon_0 = 8.854 \cdot 10^{-12}$ C/Vm and $\epsilon_{r_{SiO_2}} = 3.9$ is the dielectric constant of SiO_2, t_{ox} is the oxide thickness

The MOS Transistor

Capacitances in the MOS Transistor

- Gate-Channel Capacitance
  Due to the increase of effective t_{ox} in depletion mode the gate-channel capacitance is a function of V_{GS}:



[Grove et al., 1965]

The MOS Transistor

Capacitances in the MOS Transistor

- Channel-Bulk-Capacitance[Laker and Sansen, 1994]

$$C_{BC} = WLC_j \tag{5}$$

$$C_j = \frac{\epsilon_0 \epsilon_{Si}}{t_j} \tag{6}$$

$\epsilon_{Si} = 11.9$, thickness of junction t_j:

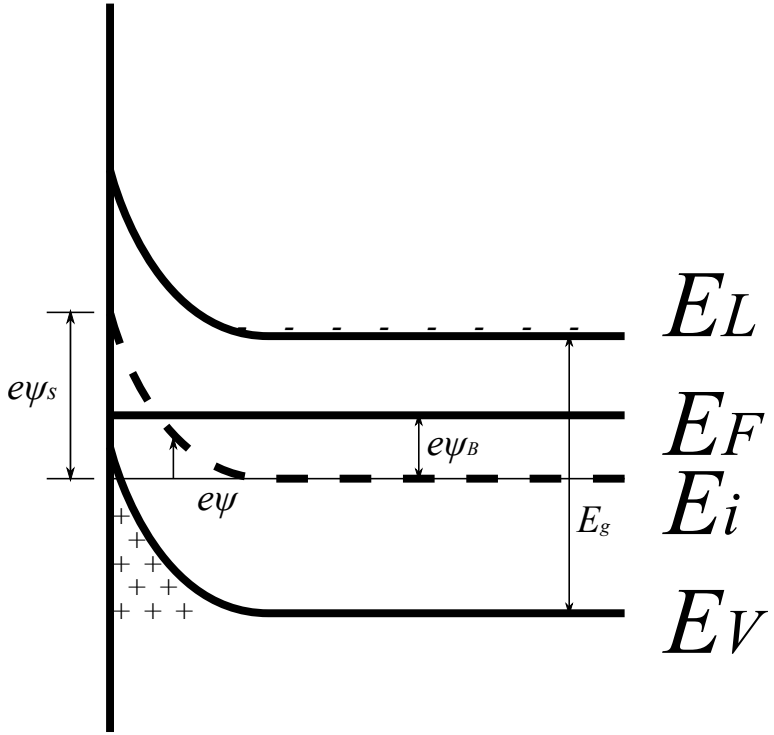
$$t_j = \sqrt{\frac{2\epsilon_0 \epsilon_{Si}(\phi_j - v_{BC})}{qN_{Sub}}} \tag{7}$$

with built-in bulk channel junction voltage ϕ_j:

$$\phi_j = \frac{kT}{q} \ln \frac{N_C N_{SUB}}{n_i^2} \tag{8}$$

The MOS Transistor

Threshold Voltage for Strong Inversion



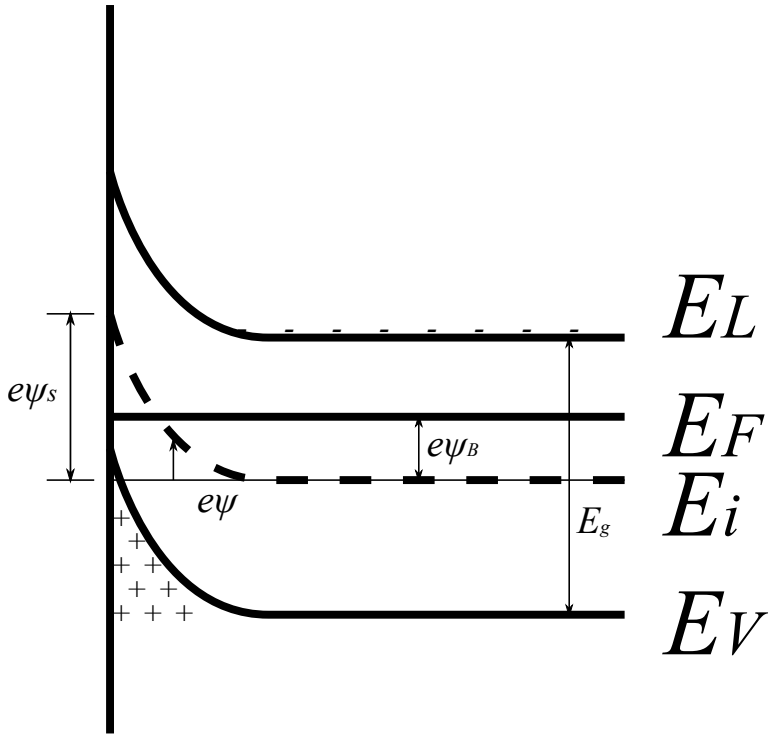
Threshold voltage for strong inversion[Weste and Eshraghian, 1985]:

$$V_{t0} = V_{t-mos} + V_{fb} \quad (9)$$

- V_{t-mos} Threshold voltage of ideal MOS Diode
- V_{fb} Flat band voltage

The MOS Transistor

Threshold Voltage for Strong Inversion



Threshold voltage of ideal MOS Diode V_{t-mos}:

$$V_{t-mos} = 2\Psi_B + \frac{Q_b}{C_{ox}} \quad (10)$$

with

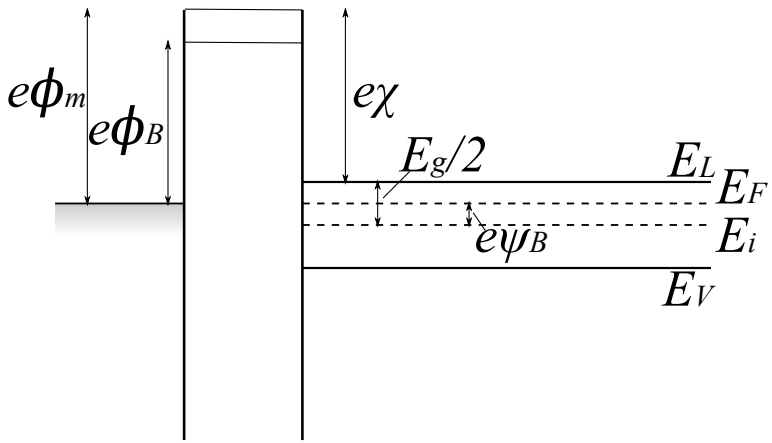
$$\Psi_B = \frac{kT}{q} \ln \frac{N_{SUB}}{n_i} \quad (11)$$

C_{ox} is the oxide capacitance given in eq. 4 and Q_b the bulk charge term

$$Q_b = \sqrt{2\epsilon_0 \epsilon_{Si} q N_{Sub} 2\Psi_B} \quad (12)$$

The MOS Transistor

Threshold Voltage for Strong Inversion



Q_{fc}: fixed charge due to surface states at the silicon oxide interface. C_{ox} is the oxide capacitance.

Flatband voltage V_{fb} :

$$V_{fb} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}} \qquad (13)$$

ϕ_{ms} is the work function difference between the metal and the semiconductor $\phi_{ms} = \phi_m - \chi$ or:

$$\phi_{ms} = -\left(\frac{E_g}{2} + \Psi_B\right) \qquad (14)$$

- nMOS: $\phi_{ms} \approx -0.9$ V
- pMOS: $\phi_{ms} \approx -0.2$ V

The MOS Transistor

The Metal Insulator Semiconductor (MIS) Diode

A bulk-source voltage $V_{BS} \neq 0$ causes an increase of the depletion layer $\Rightarrow$ Q_b increases, eq. 12 modified to

$$\frac{Q_b}{C_{ox}} = \gamma\sqrt{2\Psi_B - V_{BS}} \tag{15}$$

So Threshold voltage is given by

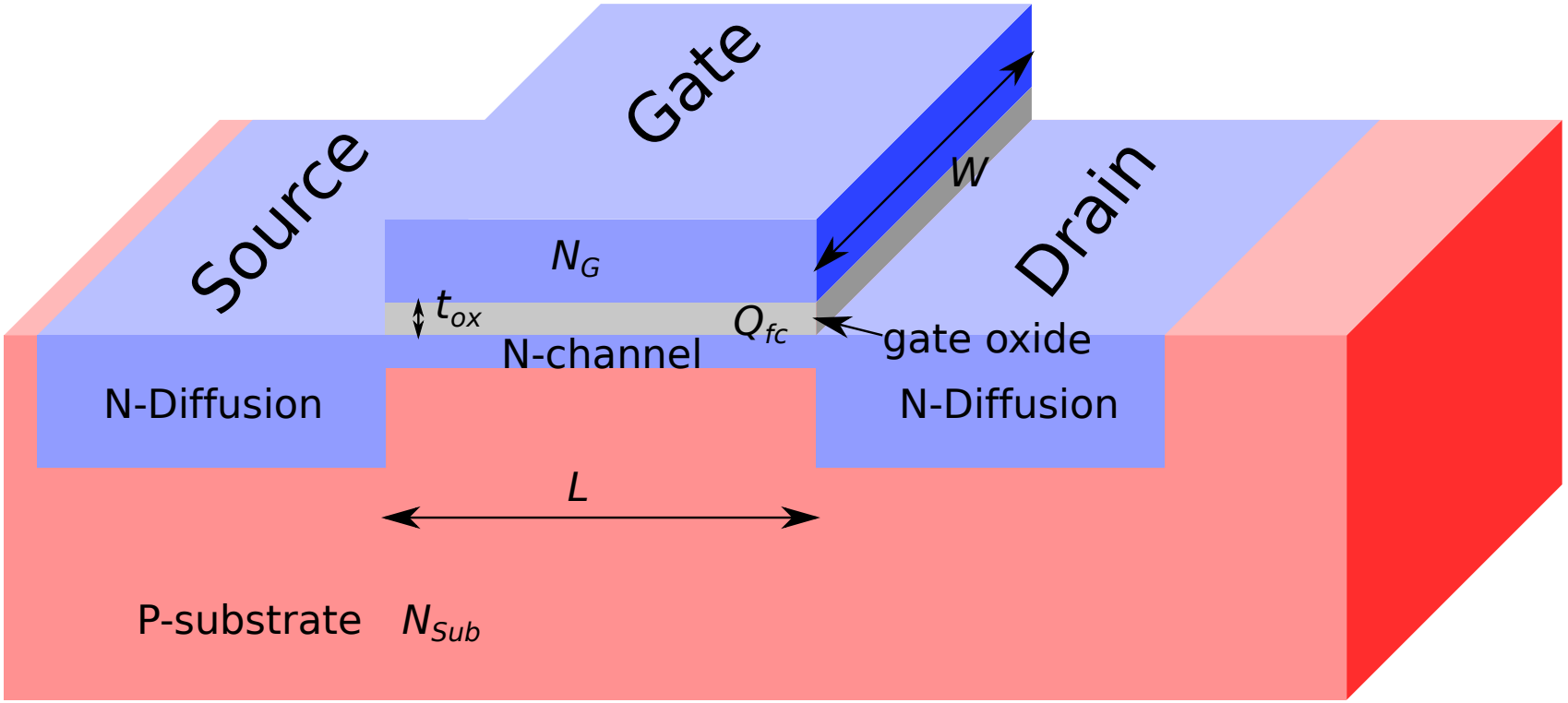
$$V_t = V_{t0} + \gamma\left(\sqrt{1\Psi_B + V_{BS}} - \sqrt{2\Psi_B}\right) \tag{16}$$

With Bulk polarisation γ

$$\gamma = \frac{\sqrt{2\epsilon_{Si} q N_{Sub}}}{C_{ox}} \tag{17}$$

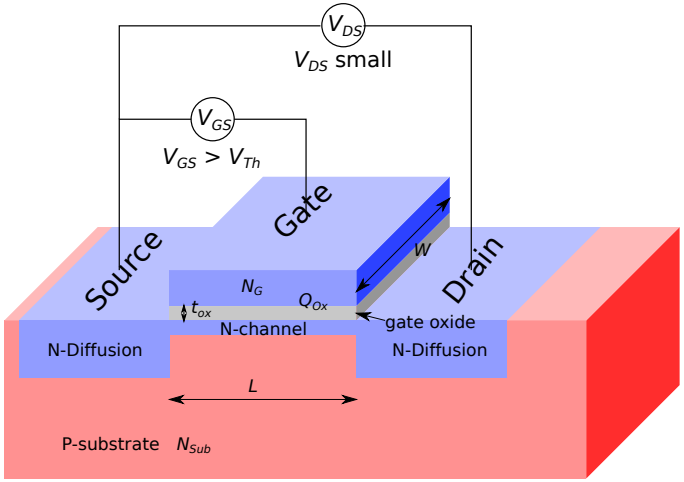
The MOS Transistor

Transistor Geometry



The MOS Transistor

Operation Modes – Linear Region



$U_{GS} > V_t$ and U_{DS} small:

$$Q_m = C_{ox}(U_{GS} - V_t) \quad (18)$$

$$R_{DS} = \frac{L}{W}\frac{1}{\mu Q_m} \quad (19)$$

$$\beta = \frac{W}{L}KP \quad (20)$$

$$KP = \mu C_{ox} \quad (21)$$

$$\Rightarrow \quad R_{DS} = \frac{1}{\beta(U_{GS} - V_t)} \quad (22)$$

[Laker and Sansen, 1994]

The MOS Transistor

Operation Modes – Linear Region

Example:

Given:

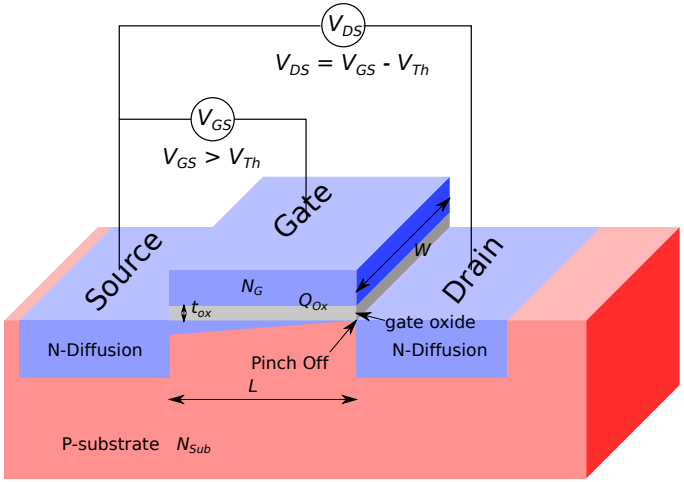
$$
\begin{aligned}
t_{ox} &= 7.5 \text{ nm} \\
\mu &= 4.35 \cdot 10^{-2} \frac{\text{m}^2}{\text{Vs}} \\
W/L &= 10 \\
V_t &= 0.45 \text{ V}
\end{aligned}
$$

Calculation of R_{DS} for $V_{GS} = 0.5$ V and $V_{GS} = 3.3$ V:

$$
\begin{aligned}
C_{ox} &= \frac{\epsilon_0 \epsilon_r}{t_{ox}} \\
&= 4.6 \cdot 10^{-3} \text{ F/m}^2 \\
\beta &= \frac{W}{L} \mu C_{ox} \\
&= 2 \text{ mA/V}^2 \\
R_{DS}(0.5 \text{ V}) &= 10 \text{ k}\Omega \\
R_{DS}(3.3 \text{ V}) &= 175 \ \Omega
\end{aligned}
$$

The MOS Transistor

Operation Modes – Pinch Off



$U_{GS} > V_t$ and $U_{DS} \leq U_{GS} - V_t$:

- Voltage drop along the channel

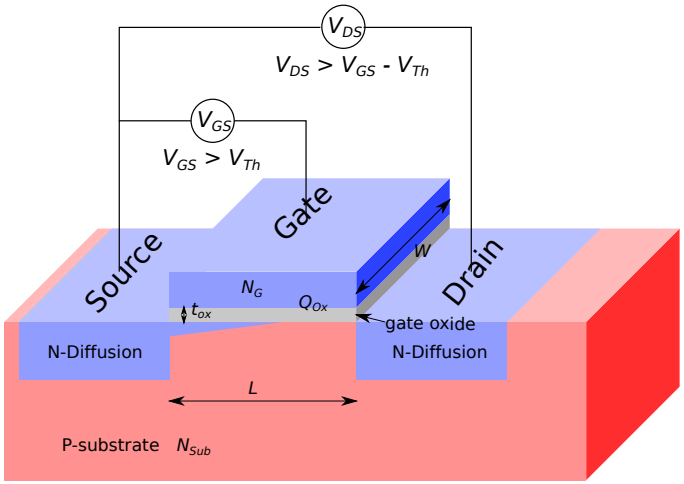
$\Rightarrow$ Gate channel voltage U_{GC} becomes position dependent

- In case of $U_{DS} = U_{GS} - V_t$ N-channel is pinched off at drain
- R_{DS} increases with U_{DS}
- First order model for drain current[Laker and Sansen, 1994]:

$$I_D = \beta \left(U_{GS} - V_t - \frac{U_{DS}}{2} \right) U_{DS} \tag{23}$$

The MOS Transistor

Operation Modes – Saturation



$U_{GS} > V_t$ and $U_{DS} > U_{GS} - V_t$:

- First order model: drain - source current saturates

$$I_{DS_{Sat}} = \frac{\beta}{2}(U_{GS} - V_t)^2 \quad (24)$$

The MOS Transistor

Operation Modes – Saturation

Example:

Given:

$$\begin{aligned} t_{ox} &= 7.5 \text{ nm} \\ \mu &= 4.35 \cdot 10^{-2} \frac{\text{m}^2}{\text{Vs}} \\ W/L &= 10 \\ V_t &= 0.45 \text{ V} \end{aligned}$$

Calculation of $I_{DS_{Sat}}$ for $V_{GS} = 0.5$ V and $V_{GS} = 3.3$ V:
From first Example: $\beta = 2$ mA/V^2

$$\begin{aligned} I_{DS_{Sat}} &= \frac{\beta}{2}(U_{GS} - V_t)^2 \\ I_{DS_{Sat}}(0.5 \text{ V}) &= 2.5\ \mu\text{A} \\ I_{DS_{Sat}}(3.3 \text{ V}) &= 8.1 \text{ mA} \end{aligned}$$

The MOS Transistor

Operation Modes – Saturation

Corrections:

- Observed saturation current lower than given by eq 24 ⇒ correction factor n[Laker and Sansen, 1994]:

$$n = 1 + \frac{C_{BC}}{C_{ox}} + \frac{qN_{FS}}{C_{ox}} \tag{25}$$

$$\frac{C_{BC}}{C_{ox}} = \frac{\gamma}{2\sqrt{\phi_j - V_{BS}}} \tag{26}$$

Then

$$I_{DS} = \beta \left(V_{GS} - V_t - \frac{n}{2} V_{DS} \right) V_{DS} \tag{27}$$

$$I_{DS_{Sat}} = \frac{\beta}{2n} \left(V_{GS} - V_t \right)^2 \tag{28}$$

The MOS Transistor

Operation Modes – Saturation

Corrections:

- Channel length Modulation leads to current increasing with U_{DS}

$$I_{DS_{Sat}} = \frac{\beta}{2}\left(U_{GS} - V_t\right)^2 \left(1 + \lambda V_{DS}\right) \tag{29}$$

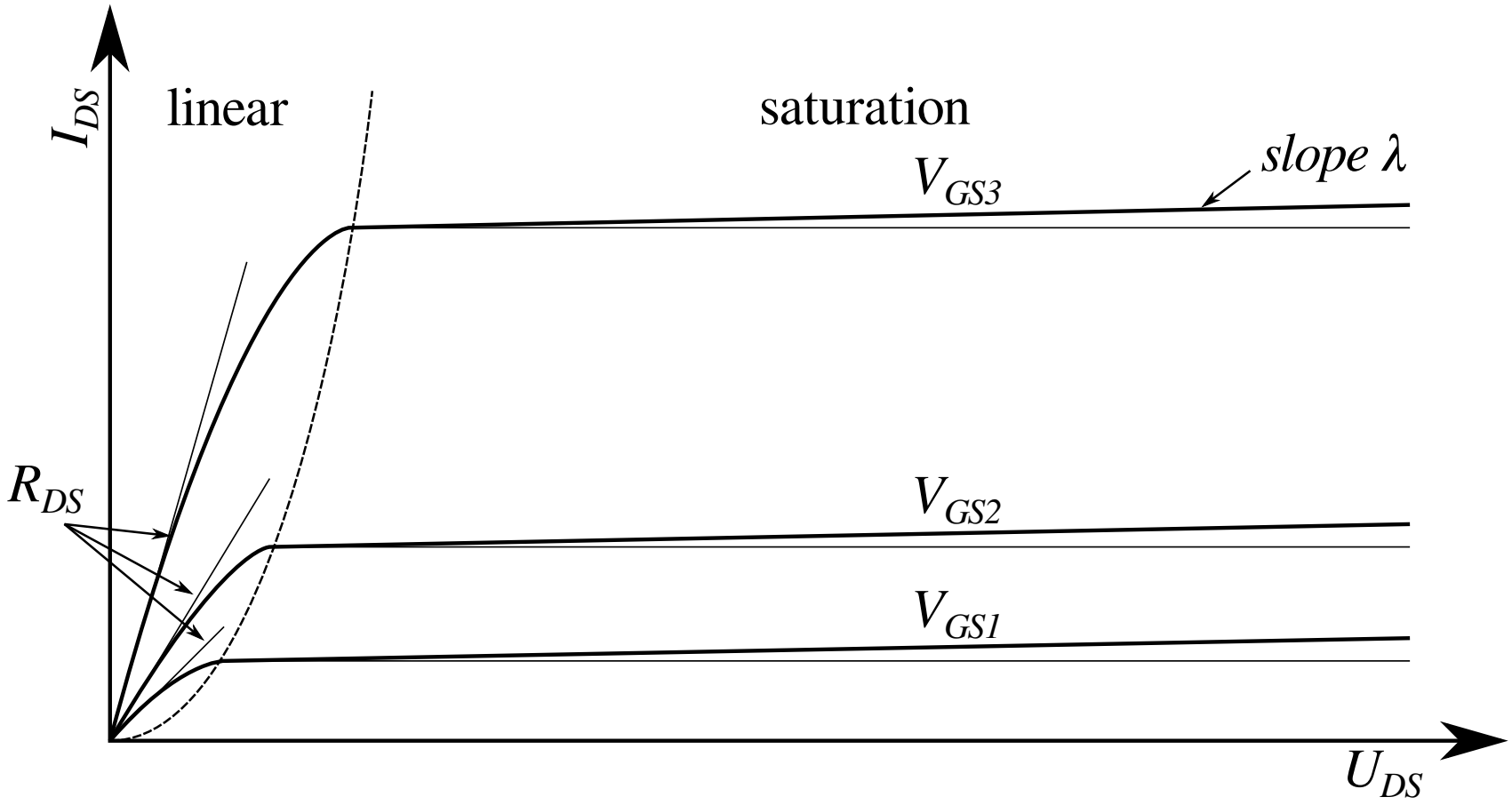
λ increases with decreasing channel length. To parameterise λ Early voltage per channel length V_E is defined:

$$V_E = \frac{1}{\lambda L} \tag{30}$$

Typical values for V_E[Laker and Sansen, 1994]:
$V_{E_n} = 4\ \mathrm{V}/\mu\mathrm{m}$ and $V_{E_p} = 7\ \mathrm{V}/\mu\mathrm{m}$

The MOS Transistor

Operation Modes – Saturation



The MOS Transistor

Operation Modes – Sub threshold

$U_{GS} < V_t$:

- In weak inversion drain source current increases exponentially

$$I_{DS_{Sat}} = \frac{W}{L} I_{D0} \exp\left(\frac{U_{GS}}{nKT/q}\right) \tag{31}$$

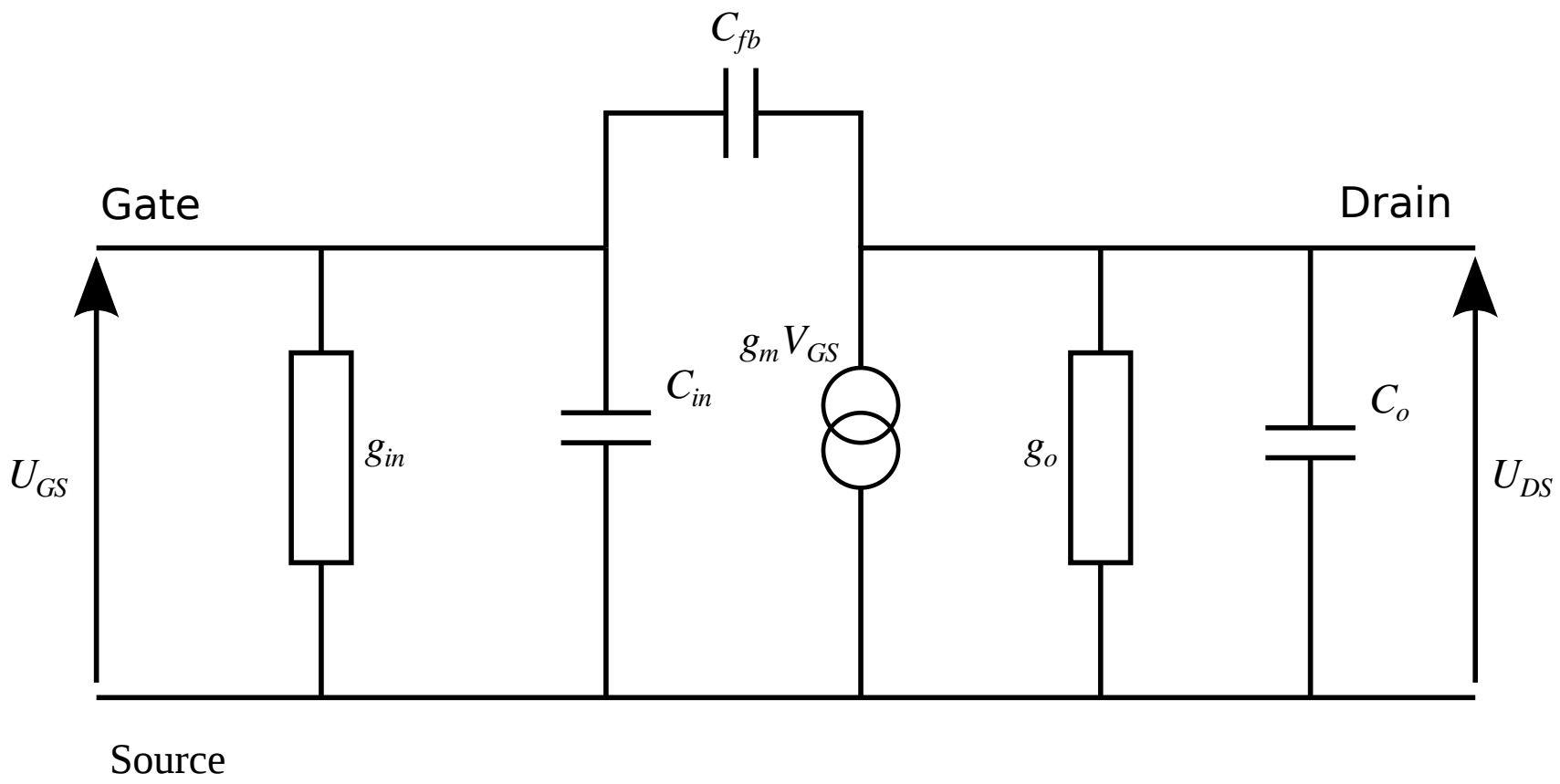
With slope:

$$S = \frac{nkT}{q} \ln 10 \tag{32}$$

Minimum slope for $n = 1$ is 60 mV/decade

The MOS Transistor

Small Signal Model



[Ihantola and Moll, 1964]

The MOS Transistor

Small Signal Model in Saturation Mode

Transconductance g_m: Eq. 24:

$$I_{DS_{Sat}} = \frac{\beta}{2n}(U_{GS} - V_t)^2 \text{ with } \beta = \frac{W}{L}KP \text{ (Eq. 20)}$$

$$\begin{aligned} g_m &= \frac{\partial I_{DS}}{\partial U_{GS}} && (33) \\ &= \frac{\partial}{\partial U_{GS}}\left[\frac{\beta}{2n}(U_{GS} - V_t)^2\right] && (34) \\ &= \frac{\beta}{n}(U_{GS} - V_t) && (35) \end{aligned}$$

Optionally $g_m = \sqrt{2 I_{DS}\beta/n}$ or $g_m = I_{DS}/(V_{GS} - V_t)$.

The MOS Transistor

Small Signal Model

	Linear	Saturation	Weak Inversion
$g_m = \frac{\partial I_D}{\partial V_{GS}}$	βV_{DS}	$\frac{\beta}{n}(V_{GS} - V_t)$	$\frac{I_{DS}}{nKT/q}$
$g_o = \frac{\partial I_{DS}}{\partial U_{DS}}$	$\beta(V_{GS} - V_t - V_{DS})$	$\lambda I_{DS_{Sat}}$	
$g_{in} = \frac{\partial I_G}{\partial V_{GS}}$		≈ 0	

Optional g_o in saturation mode: $g_o = \frac{I_{DS_{Sat}}}{V_E L}$

The MOS Transistor I

Noise

- Thermal channel noise

$$i_d^2 = 4kT\frac{2}{3}g_m \tag{36}$$

- Gate current noise
  noise current in gate due to capacitive coupling
  negligible for $f < f_t = g_m/2\pi C_{GS}$

$$i_g = 4kT\frac{g_m}{5}\left(\frac{f}{f_T}\right)^2 \tag{37}$$

The MOS Transistor II

Noise

- $1/f$-noise

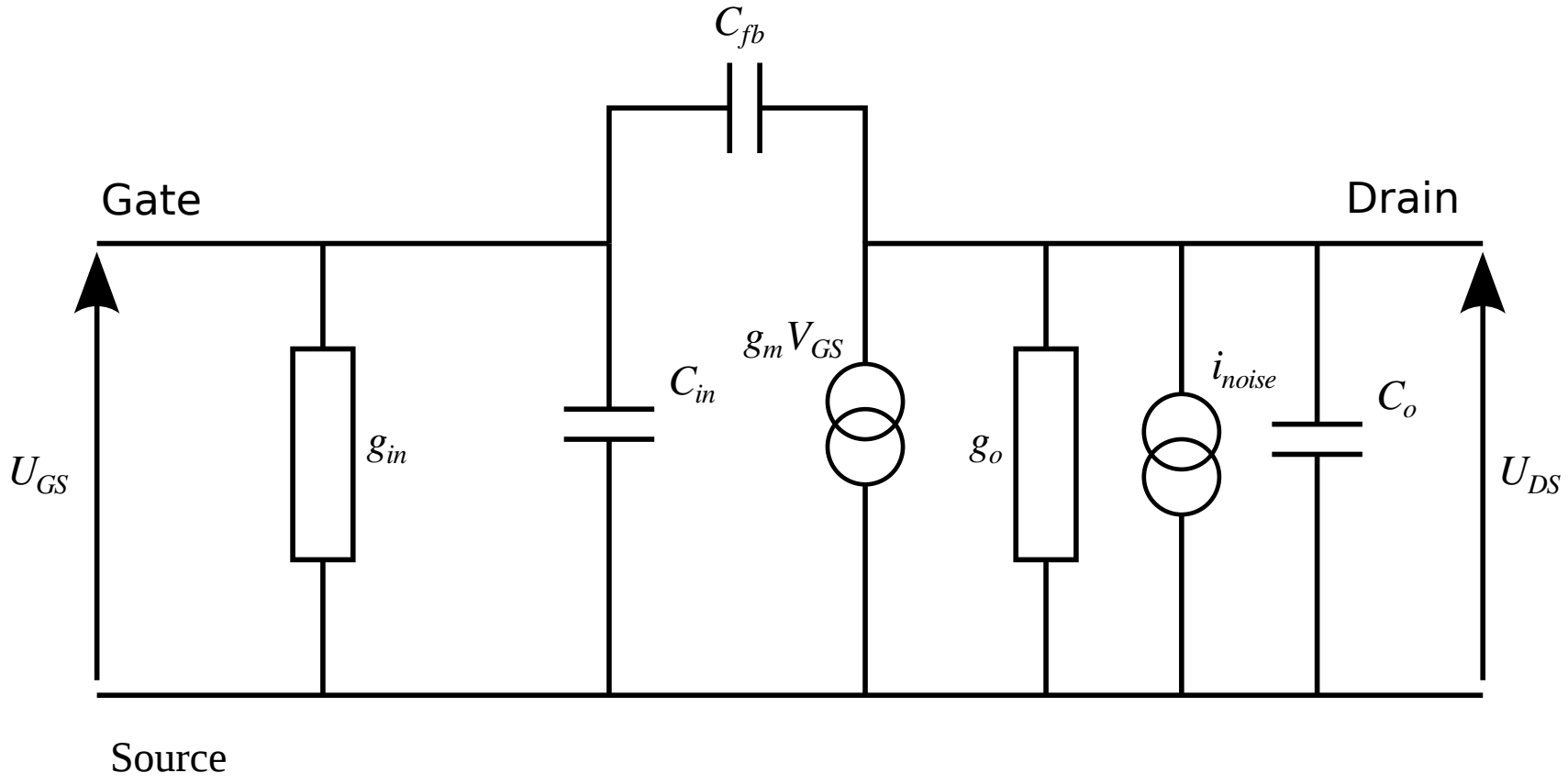
$$i_d^2(f) = \frac{K_F I_{DS}}{C_{ox} L^2 f} \tag{38}$$

K_F constant for different transistor types
Empirical values for K_f [Chang and Sansen, 1991]:

pJFET	$K_f \approx 10^{-33}\ \mathrm{C}^2/\mathrm{cm}^2$
pMOS	$K_f \approx 10^{-32}\ \mathrm{C}^2/\mathrm{cm}^2$
nMOS	$K_f \approx 4 \cdot 10^{-31}\ \mathrm{C}^2/\mathrm{cm}^2$

The MOS Transistor

Small Signal Model Including Noise



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- Single MOST Amplifier Stage

5 CMOS Scaling and Future Technologies

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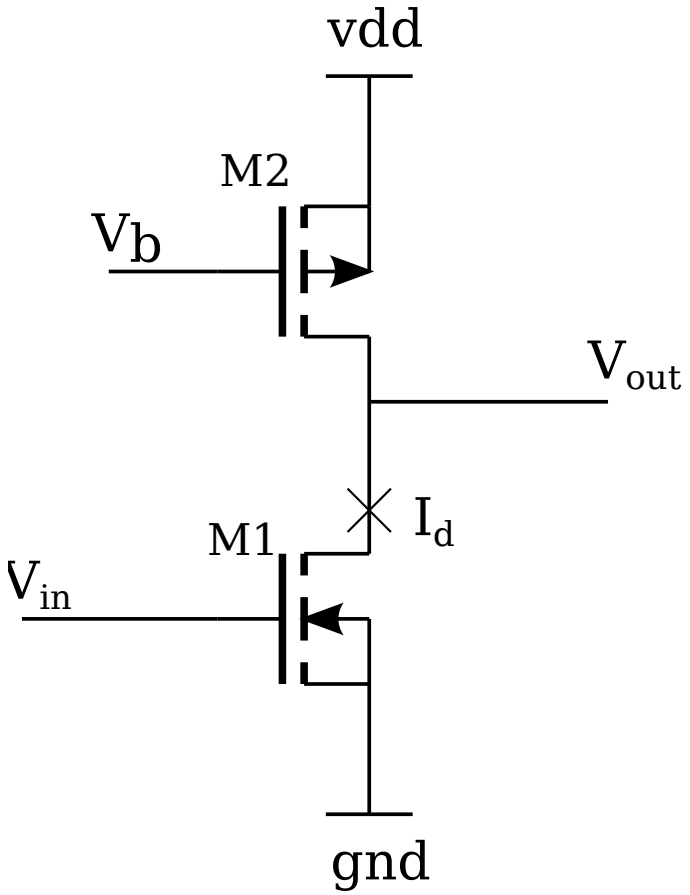
MOS Transistor stages

Single MOST Amplifier Stage



Example case 350 nm Technology

- *vdd*: 3.3 V
- Technology parameter:
  - t_{ox} : 7.5 nm
  - μ_N: $4.35 \cdot 10^{-2}\ \frac{m^2}{Vs}$
  - μ_P: $2.66 \cdot 10^{-2}\ \frac{m^2}{Vs}$
  - V_{tN}: 450 mV
  - V_{tP}: 700 mV
  - V_{E_p}: 7 V/µm
  - V_{E_n}: 4 V/µm
  - n: 1.2

MOS Transistor stages I

Single MOST Amplifier Stage

First Try: $I_{DS} = 100\ \mu\text{A}$ and $V_{in} = V_{Out} = 1.65$ V:
From t_{ox}, μ_N and μ_P one gets

$$\begin{aligned} KP_n &= 200\ \mu\text{A/V}^2 \\ KP_p &= 122\ \mu\text{A/V}^2 \end{aligned}$$

Transistor dimension of nMOS ($L_{min=0.35}\ \mu$m):

$$\begin{aligned} W/L &= \frac{2nI_{DS}}{KP_n(V_{GS} - V_t)^2} \\ &= 0.833 \end{aligned}$$

MOS Transistor stages II

Single MOST Amplifier Stage

We chose $L = 1\ \mu\text{m},\ W = 0.85\ \mu\text{m}$
For pMOS with $V_b = vdd - 1$ V:

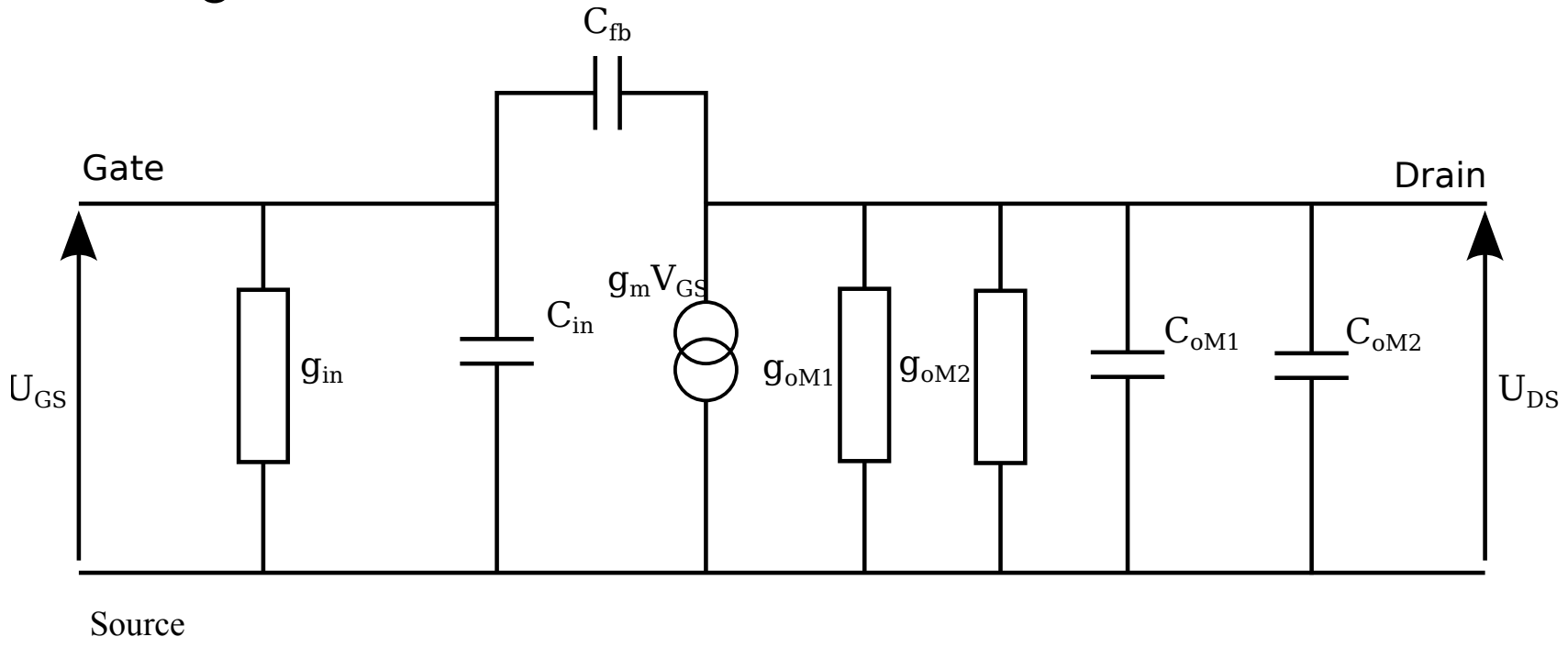
$$\begin{aligned} W/L &= \frac{2nI_{DS}}{KP_p(V_{GS} - V_t)^2} \\ &= 21.9 \end{aligned}$$

Chosen: $L = 1\ \mu\text{m},\ W = 22\ \mu\text{m}$

MOS Transistor stages

Single MOST Amplifier Stage

Small Signal Model:



MOS Transistor stages

Single MOST Amplifier Stage

For small signal amplification A_0 at low frequencies:

$$A_0 = \frac{V_{Out}}{V_{In}} = -\frac{g_m}{g_{oM1} + g_{oM2}}$$

With $g_m = I_{DS}/(V_{GS} - V_t)$ and $g_o = I_{DS}/(V_E L)$ one gets $g_m = 83.3\ \mu\text{S}$, $g_{oM1} = 25\ \mu\text{S}$ and $g_{oM2} = 14.2\ \mu\text{S}$

$$A_0 = -2.125$$

MOS Transistor stages

Single MOST Amplifier Stage

Second try: $I_{DS} = 100\ \mu$A, $V_{in} = 0.5$ V and $V_{out} = 1.65$ V:
Transistor dimension for $M1$:

$$W/L = 480$$

We chose $L = 0.35\ \mu$m and $W = 168\ \mu$m
For $M2$ with $V_b = vdd - 2$ V:

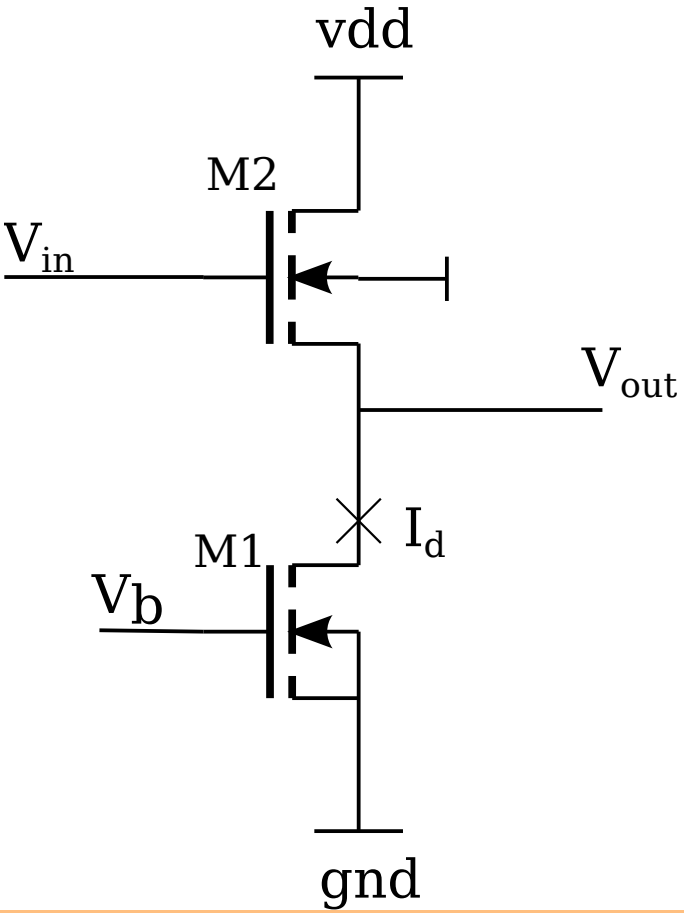
$$W/L = 1.164$$

We chose: $L = 5\ \mu$m and $W = 5.8\ \mu$m
For small signal amplification one gets:
$g_m = 1$ mS, $g_{oM1} = 71\ \mu$S and $g_{oM2} = 2.85\ \mu$S

$$A_0 = -13.5$$

MOS Transistor stages

Exercises

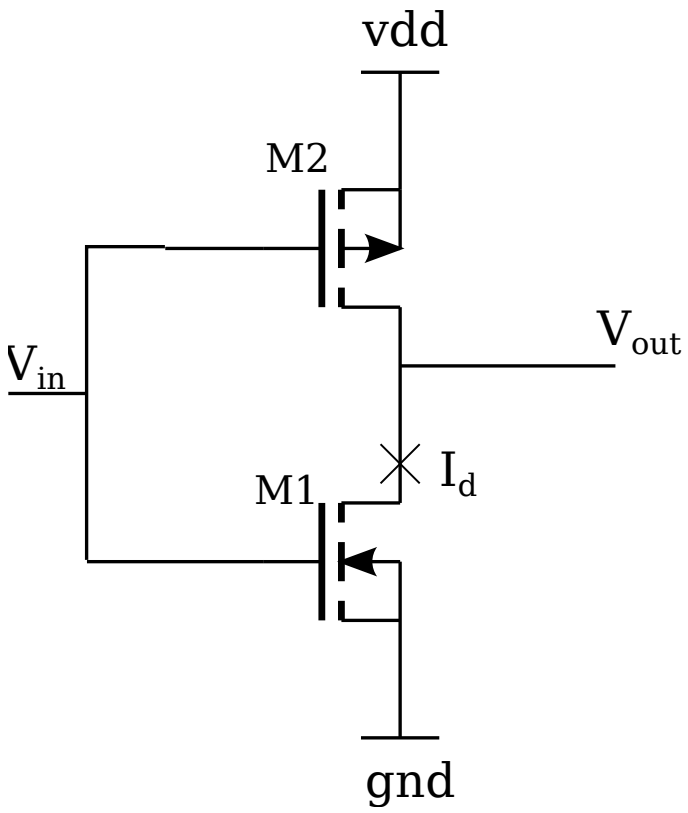


Source Follower Stage

- M1: NMOS
- M2: NMOS
- I_d: 100 µA
- V_{In}: 1.65 V
- V_b: 2 V

MOS Transistor stages

Exercises

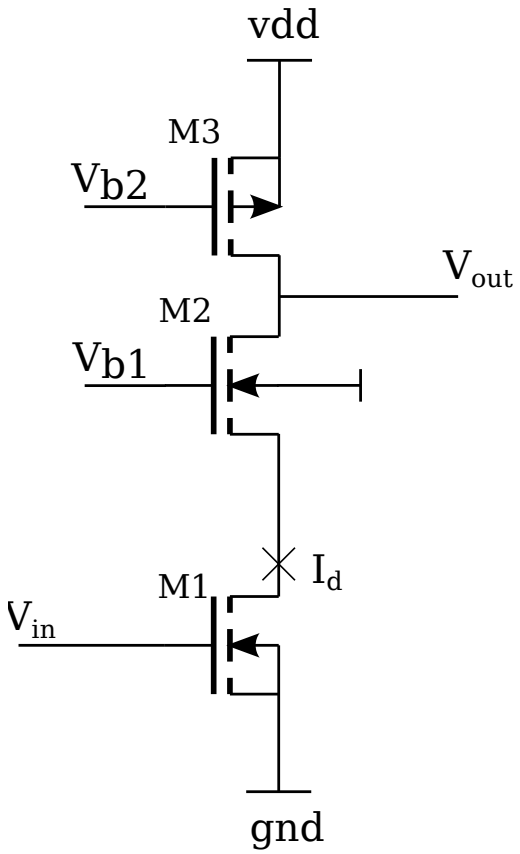


Inverter Stage

- M1: NMOS
- M2: PMOS
- I_d: 100 µA
- V_{In}: 1.65 V
- V_{Out}: 1.65 V

MOS Transistor stages

Exercises

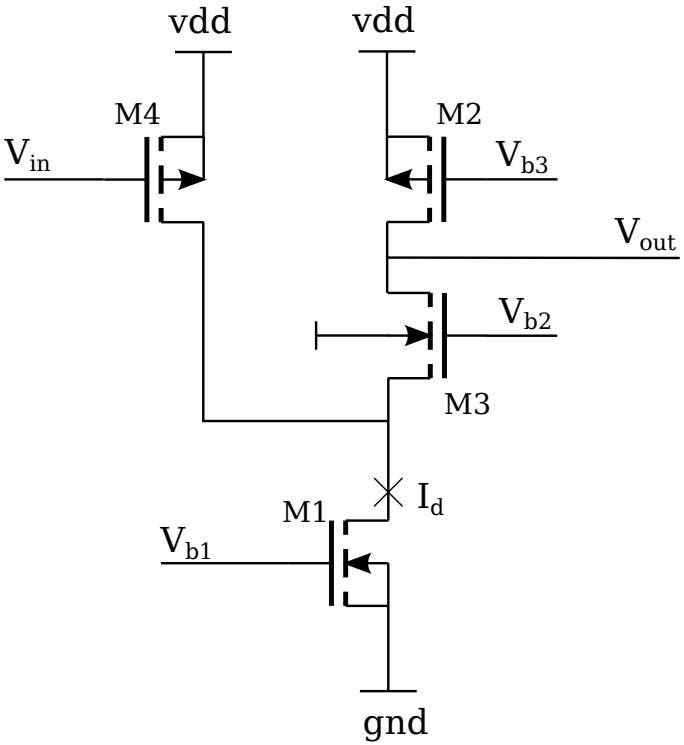


Cascode Stage

- M1: NMOS
- M2: NMOS
- M3: PMOS
- I_d: 100 µA
- V_{In}: 0.5 V
- V_{Out}: 2.5 V
- V_{DM1}: 1 V
- V_{b2}: vdd - 2 V

MOS Transistor stages

Exercises



Folded Cascode Stage

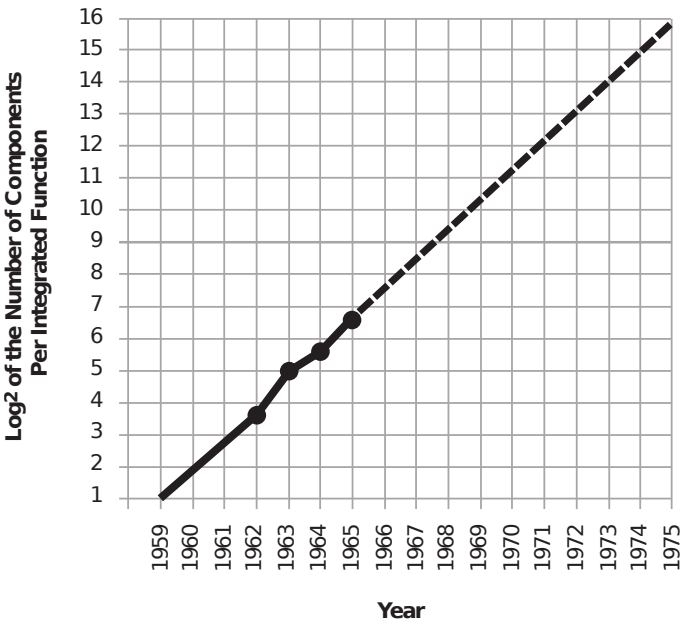
- M1: NMOS
- M2: PMOS
- M3: NMOS
- M4: PMOS
- I_d: 100 µA
- I_{dM4}/I_{dM2}: 9 / 1
- V_{In}: vdd - 0.75 V
- V_{Out}: 2.5 V
- V_{DM1}: 1 V
- V_{b2}: vdd - 2 V

Outline

1. Motivation
2. Reminder of Semiconductor Physics
3. The MOS Transistor
4. MOS Transistor stages
5. CMOS Scaling and Future Technologies
   - Moore's Law
   - Benefits of CMOS Scaling
   - Problems of CMOS Scaling

CMOS Scaling

Moore's Law



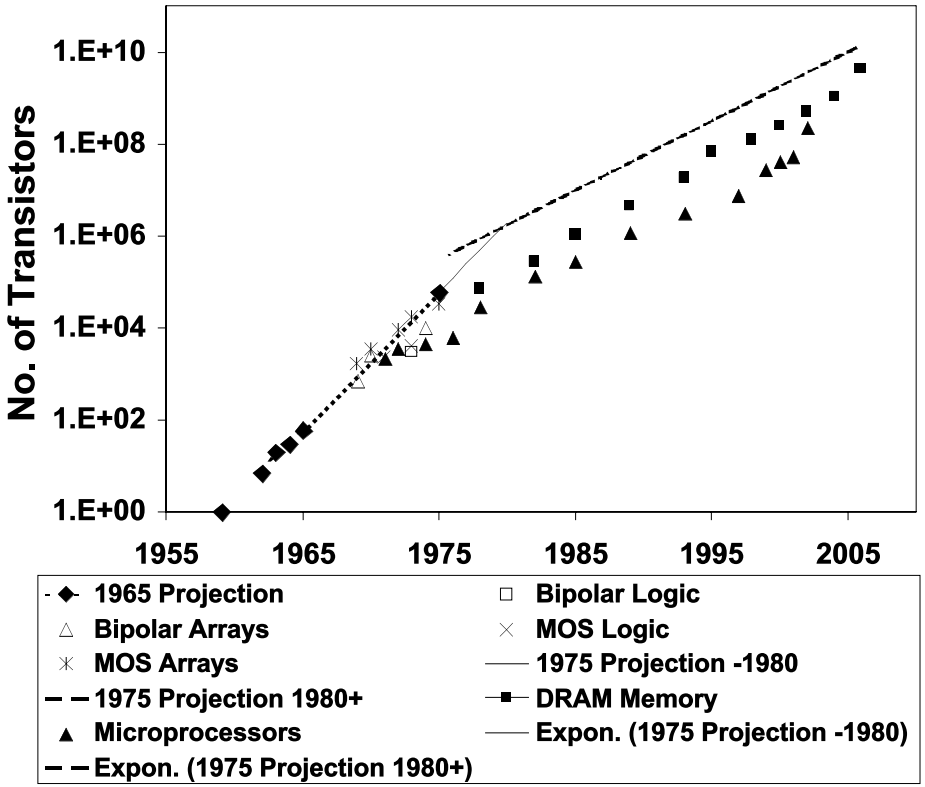
[Moore, 1965]

Moore's Law

- Every 18 Months the number of Transistors per Chip is doubled
- Predicted by Gordon E. Moore in 1965

CMOS Scaling

Moore's Law



[Moore, 2003]

CMOS Scaling

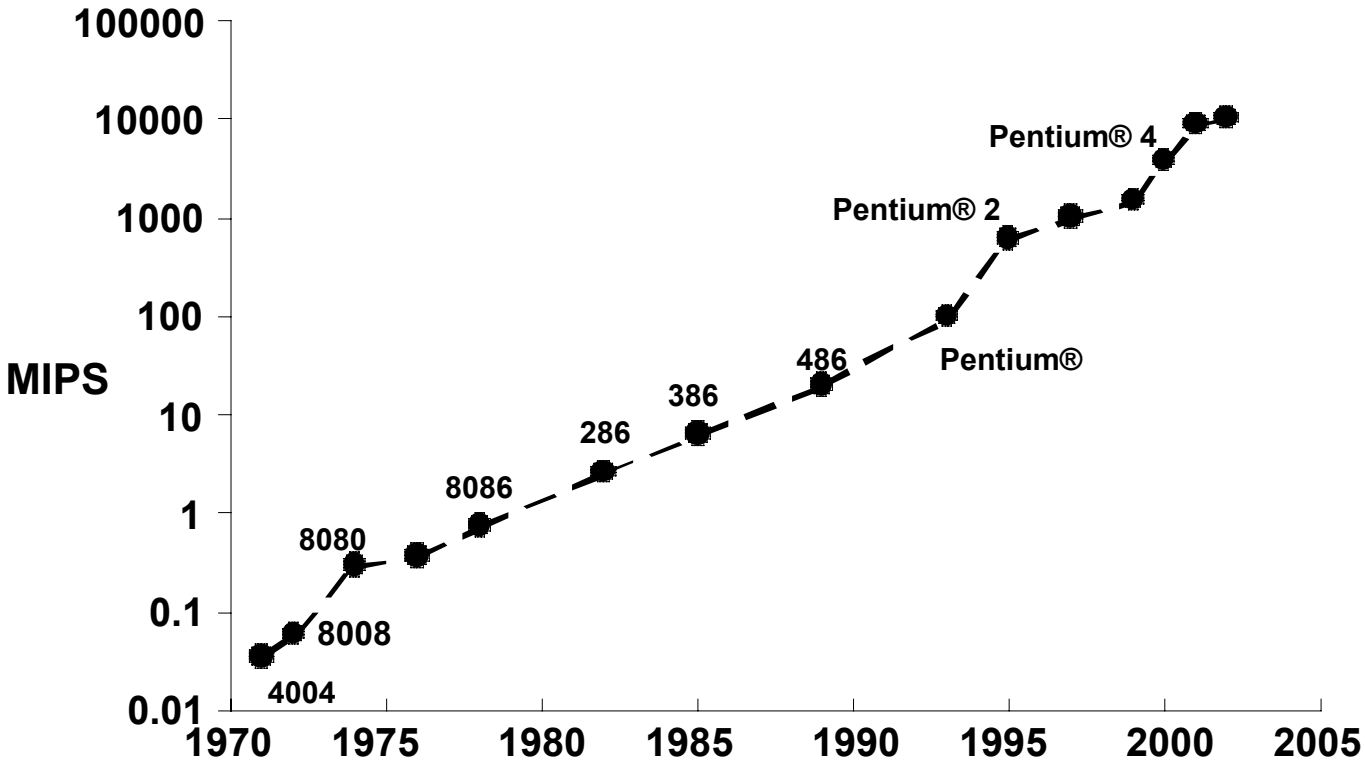
Benefits of CMOS Scaling

parameter	scaling model		
	constant field	constant voltage	lateral
Length	λ	λ	λ
Width	λ	λ	1
Supply Voltage	λ	1	1
Load Capacitance	λ	λ	λ
GateDelay	λ	λ^2	λ^2
Power dissipation	λ^2	λ	λ
Power Delay Product	λ^3	λ	λ
Gate Area	λ^2	λ^2	λ
Power Density	1	$1/\lambda^3$	$1/\lambda^2$

[Weste and Eshraghian, 1985]

CMOS Scaling

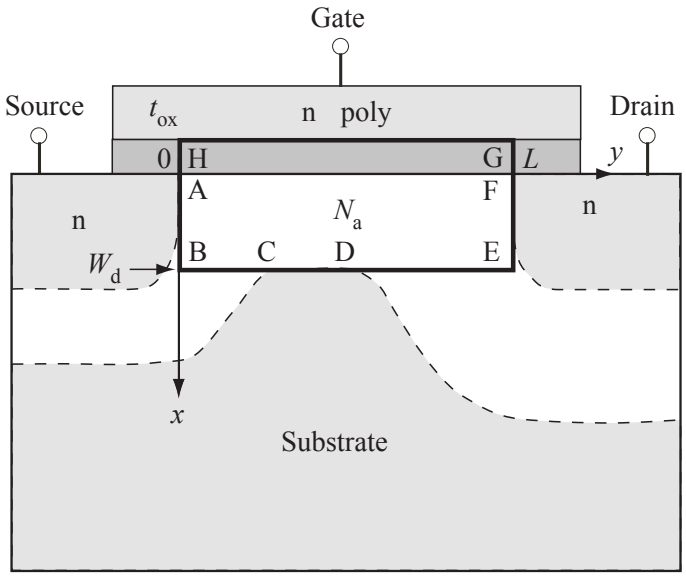
Benefits of CMOS Scaling



[Moore, 2003]

CMOS Scaling

Problems of CMOS Scaling



[Taur, 2002]

- Short channel effects (SCE)
  - 2D electrostatic effects on V_t
  - V_t roll off
  - Drain induced barrier lowering
- Leads to transistor control by drain instead of gate
- To avoid SCE $L_{min} > 2W_{dm}$ with maximum depletion width W_{dm}

$$W_{dm} = \sqrt{\frac{4\epsilon_{si} kT \ln(N_{SUB}/n_i)}{q^2 N_{SUB}}} \quad (39)$$

CMOS Scaling

Problems of CMOS Scaling

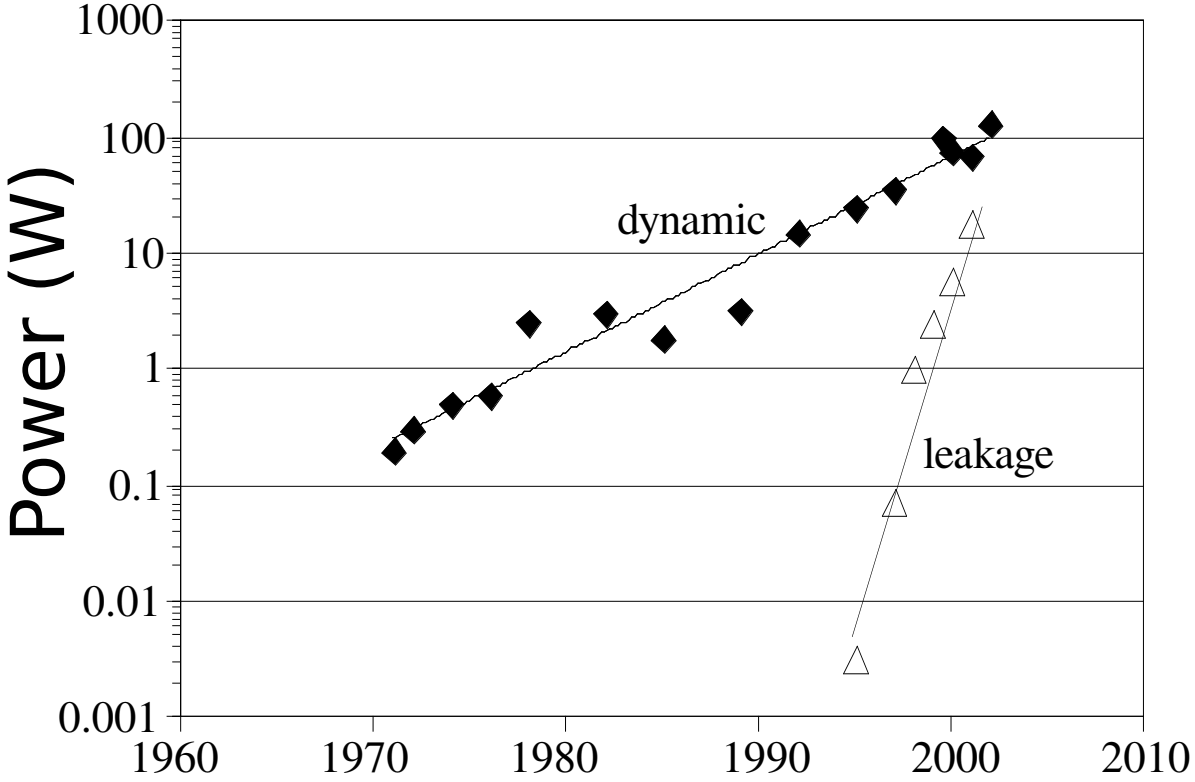
- W_{dm} and t_{ox} control sub threshold slope:

$$S = m\frac{kT}{q}\ln 10 = \left(1 + \frac{\epsilon_{Si} t_{ox}}{\epsilon_{ox} W_{dm}}\right)\frac{kT}{q}\ln 10 \qquad (40)$$

- To get reasonable I_{on}/I_{off} ratio $\Rightarrow m \leq 1.3 \Rightarrow t_{ox}/W_{dm} \leq 0.1$
- Maximum oxide thickness $t_{ox} \approx L/20$ required.
  - Gate Tunnel current due to thin oxides
  - Scaling of supply voltage

CMOS Scaling

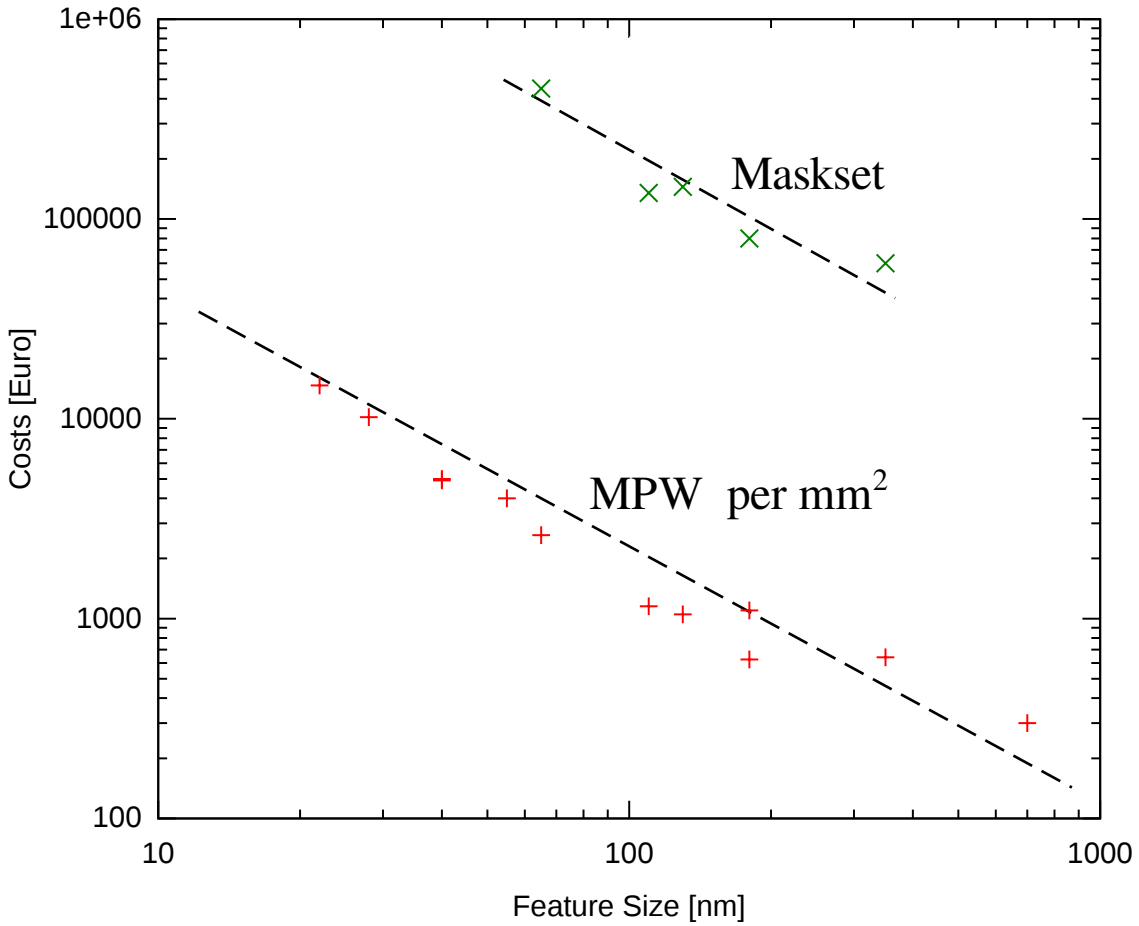
Problems of CMOS Scaling



Power consumption due to active switching and leakage in processors[Moore, 2003]

CMOS Scaling

Problems of CMOS Scaling



CMOS Scaling

Road map

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	FinFET FDSOI	FinFET FDSOI	FinFET LGAA	FinFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D

DEVICE ELECTRICAL SPECS							
Power Supply Voltage - Vdd (V)	0.80	0.75	0.70	0.65	0.55	0.45	0.40
Subthreshold slope - [mV/dec]	75	70	68	65	40	25	25
Inversion layer thickness - [nm]	1.10	1.00	0.90	0.85	0.80	0.80	0.80
Vt sat (mV) at Ioff=100nA/ m - HP Logic	129	129	133	136	84	52	52
Vt sat (mV) at Ioff=100pA/ m - LP Logic	351	336	333	326	201	125	125
Effective mobility (cm2/V.s)	200	150	120	100	100	100	100
Rext (Ohms. m) - HP Logic	280	238	202	172	146	124	106
Ballisticity. Injection velocity (cm/s)	1.20E-07	1.32E-07	1.45E-07	1.60E-07	1.76E-07	1.93E-07	2.13E-07
Vdsat (V) - HP Logic	0.115	0.127	0.136	0.128	0.141	0.155	0.170
Vdsat (V) - LP Logic	0.125	0.141	0.155	0.153	0.169	0.186	0.204
Ion /um) at Ioff=100nA/ m - HP logic w/ Rext=0	2311	2541	2782	2917	3001	2670	2408
Ion (A/ m) at Ioff=100nA/ m - HP logic, after Rext	1177	1287	1397	1476	1546	1456	1391
Ion (A/ m) at Ioff=100pA/ m - LP logic w/ Rext=0	1455	1567	1614	1603	2008	1933	1582
Ion (A/ m) at Ioff=100pA/ m - LP logic, after Rext	596	637	637	629	890	956	821
Cch, total (fF/ m2) - HP/LP Logic	31.38	34.52	38.35	40.61	43.14	43.14	43.14
Cgate, total (fF/ m) - HP Logic	1.81	1.49	1.29	0.97	1.04	1.04	1.04
Cgate, total (fF/ m) - LP Logic	1.96	1.66	1.47	1.17	1.24	1.24	1.24
CV/I (ps) - FO3 load, HP Logic	3.69	2.61	1.94	1.29	1.11	0.96	0.89
I/(CV) (1/ps) - FO3 load, HP Logic	0.27	0.38	0.52	0.78	0.90	1.04	1.12
Energy per switching [CV2] (fj/switching) - FO3 load, HP Logic	3.47	2.52	1.89	1.24	0.94	0.63	0.50

Outline

1 Motivation

2 Reminder of Semiconductor Physics

3 The MOS Transistor

4 MOS Transistor stages

5 CMOS Scaling and Future Technologies

6 Literature

Chang, Z. Y. and Sansen, W. M. (1991). *Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*. Kluwer Avademic Publishers.

Chelikowsky, J. R. and Cohen, M. L. (1976). Nonlocal pseudopotential calculations for the electronic structure of eleven diamond and zinc-blende semiconductors. *Phys. Rev. B*, 14:556–582.

Grove, A., Deal, B., Snow, E., and Sah, C. (1965). Investigation of thermally oxidised silicon surfaces using metal-oxide-semiconductor structures. *Solid-State Electronics*, 8(2):145 – 163.

Ibach, H. and Lüth, H. (1999). *Festkörperphysik*. Springer, Heidelberg, 5 edition.

Ihantola, H. and Moll, J. (1964). Design theory of a surface field-effect transistor. *Solid-State Electronics*, 7(6):423 – 430.

Laker, K. R. and Sansen, W. M. C. (1994). *Design of Analog Integrated Circuits and Systems*. McGraw-Hill series in electrical and cumputer engineering, Electronics and VLSI Circuits. McGraw-Hill.

Moore, G. E. (1965). Cramming more components onto integrated circuits, electronics,(38) 8.

Moore, G. E. (2003). No exponential is forever: but "forever" can be delayed! [semiconductor industry]. In *2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC.*, pages 20–23 vol.1.

Sze, S. M. (1981). *Physics of Semiconductor Devices*. John Wiley & Sons, New York, 2 edition.

Taur, Y. (2002). Cmos design near the limit of scaling. *IBM Journal of Research and Development*, 46(2.3):213–222.

Weste, N. H. and Eshraghian, K. (1985). *Principles of CMOS VLSI design*, volume 188. Addison-Wesley New York.