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Overview of the PANDA MVD

Micro Vertex Detector

Alessandra Lai on behalf of the PANDA MVD group, *IKP1-Forschungszentrum Jülich*, September 6, 2017

MVD design

JDRS: Jülich Digital Readout System for the MVD Prototypes

Simulations in PandaRoot

Present Status

MVD: The Innermost Sub-Detector of PANDA

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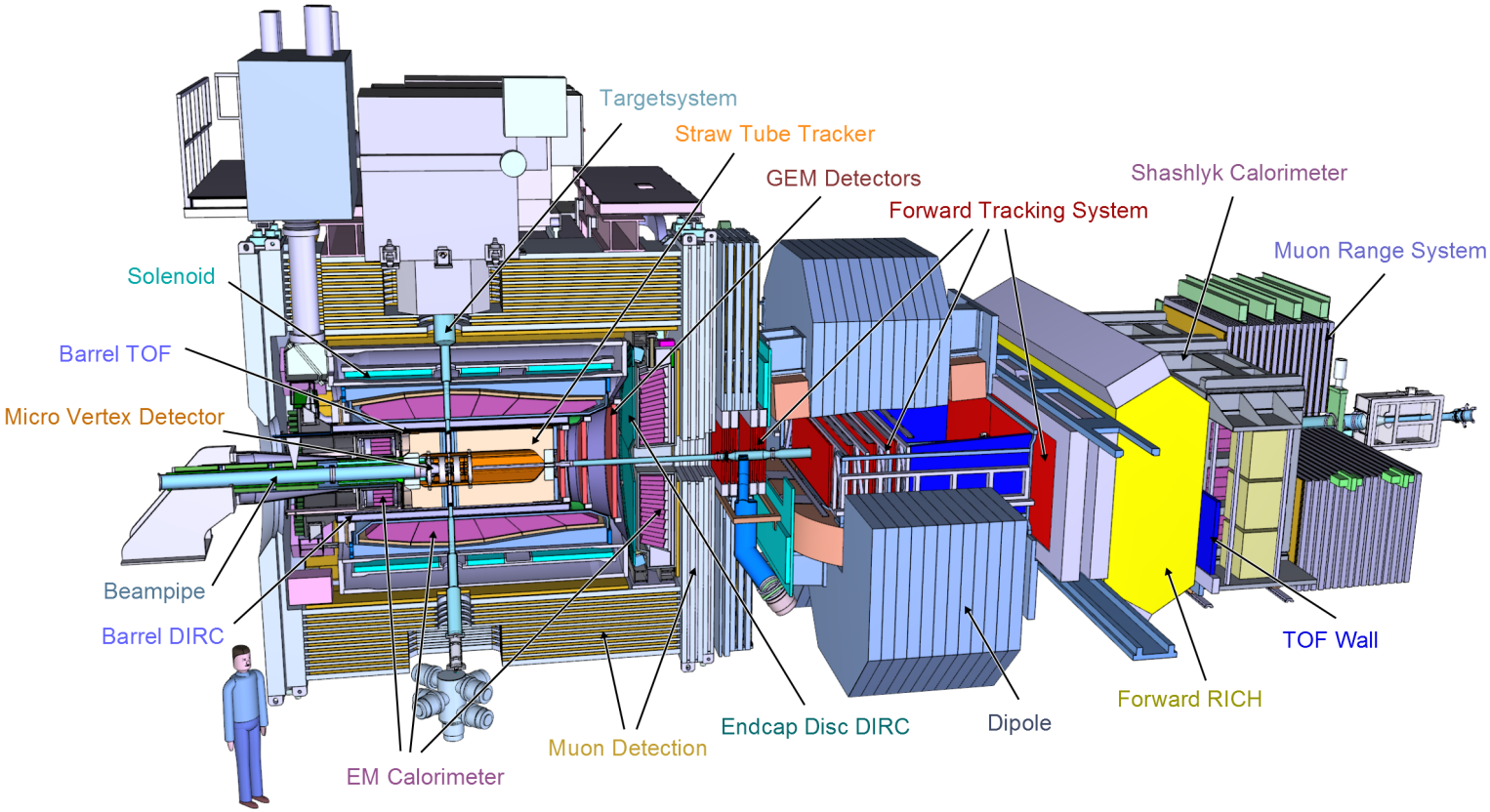


MVD as Tracking Detector

- Main task: charged particle tracking
  $\longrightarrow$ resolve primary as well as displaced vertexes.

reaction channel	detected particle	tracking used for ...
$\bar{p}p \rightarrow \phi\phi$	$2K^+\ 2K^-$	momentum measurement (PID)
$\bar{p}p \rightarrow \eta_c$	$K^\pm\ \pi^\mp\ K^0_S$	momentum measurement (PID)
$\bar{p}p \rightarrow D\overline{D}$	K's and π's	charm detection online momentum measurement (PID)
$\bar{p}A \rightarrow D\overline{D}\ X$	$D\ (\overline{D})$	inclusive charm ID online
$\bar{p}p \rightarrow \psi(2S)$	$\pi^+\ \pi^-\ J/\psi\ (\rightarrow e^+e^-\ /\ \mu^+\mu^-)$	vertex constraint

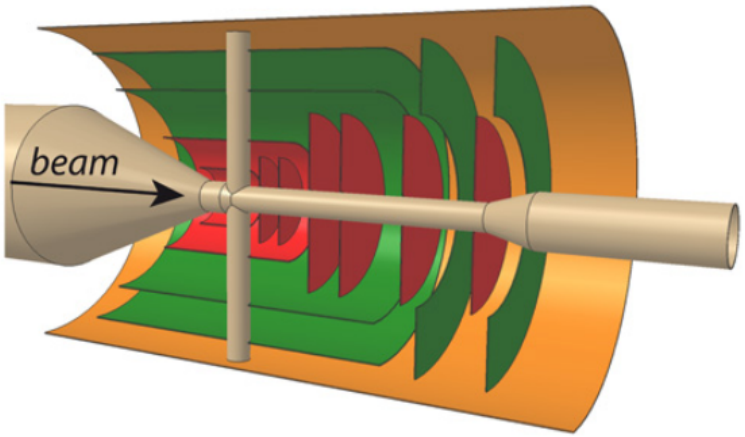
Requirements:

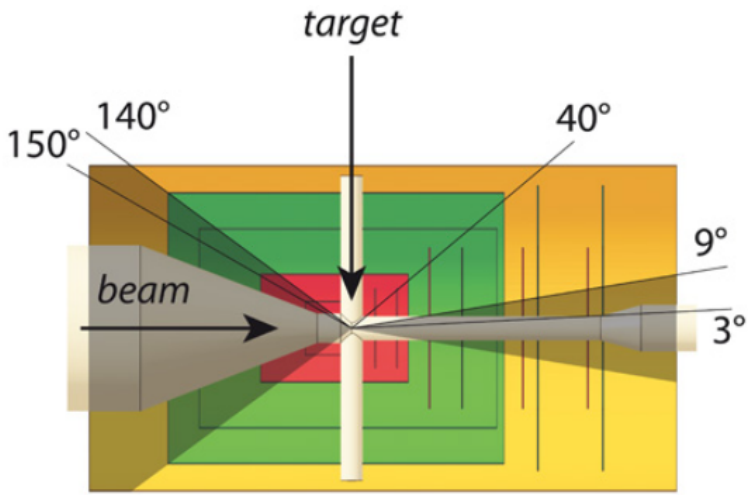
- optimum detector coverage: 3° - 150°;
- 3D hit information with spacial resolution $<$ 100 μm in z and $O(10)$μm in xy;
- time resolution: $\leq$ 10 ns;
- deposited energy for PID with dE/dx;
- low material budget: minimize photon conversion and multiple scattering;
- high rate capability ($2 \cdot 10^7$ interaction/s);
- free running readout (no first level hardware trigger);
- flexibile readout (anisotropic occupancy, depending on target);
- rad-hard technologies (estimated 10^{14} $n_{1\,\mathrm{MeV\,eq}} \cdot \mathrm{cm}^{-2}$).

MVD Design

- four barrel layers around i.p.
- six disk layers in the fw direction

- pixel detectors in the inner part
  $\longrightarrow$ high granularity, precise space information
  $\longrightarrow$ front-end chip: ToPix
- double-sided strip detectors in the outer part
  $\longrightarrow$ can cover large areas with fewer channels
  $\longrightarrow$ front-end chip: PASTA

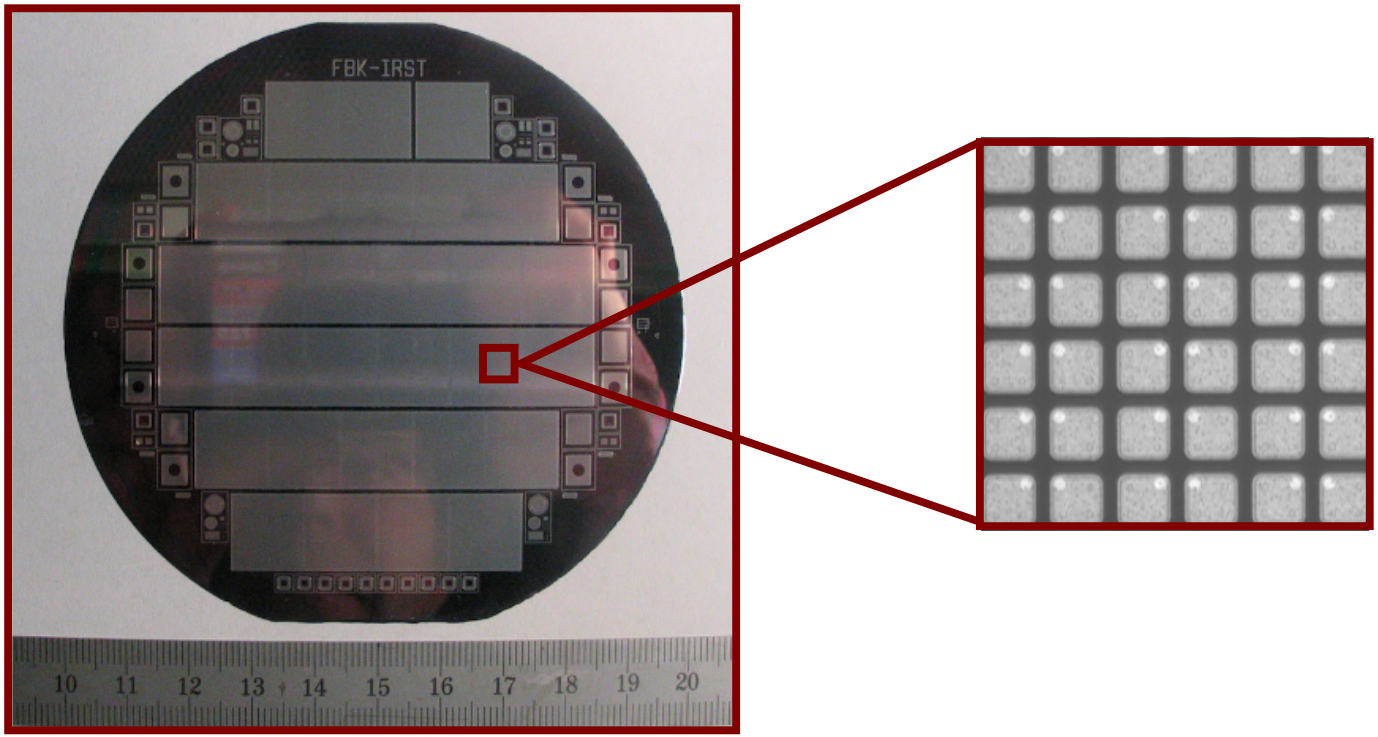




Sensors Characteristics

Pixel part

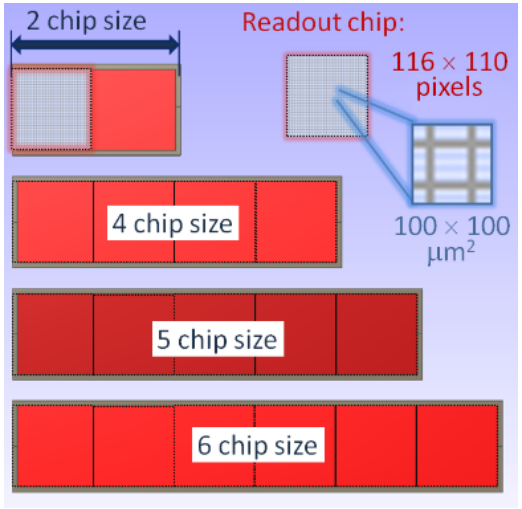
- Epitaxial silicon sensor (FBK, Trento);
- thickness: 100 μm;
- matrix of 100 x 100 μm^2;
- Cz substrate thinned to $\simeq$ 20 μm (IZM, Berlin);
- resistivity: $\simeq$ 1500 Ω· cm;
- bump bonding to electronics.



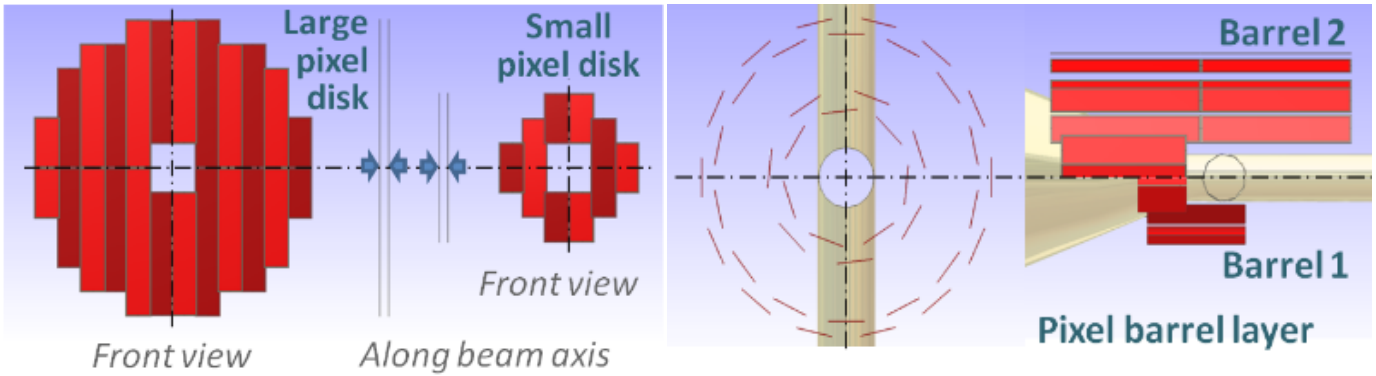
Sensors Arrangement

Pixel part

Four different pixel modules: same width but different length, depending on the readout chip size.



Sensor modules arrangement different for different detector layers.



Readout ASIC: ToPix

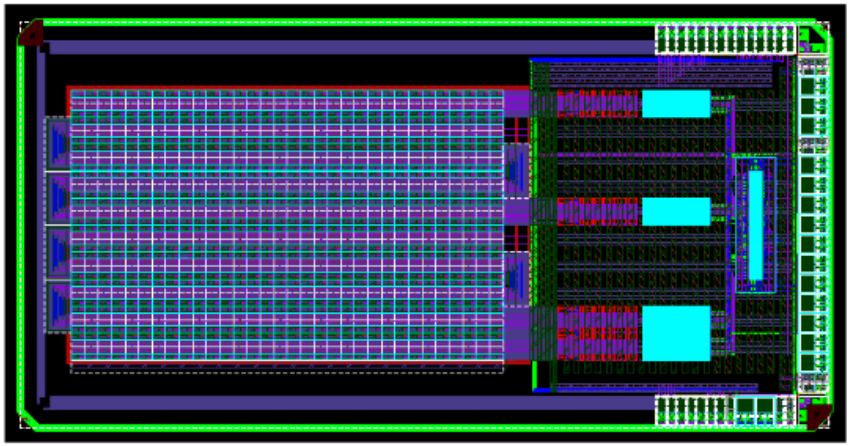
Pixel Part

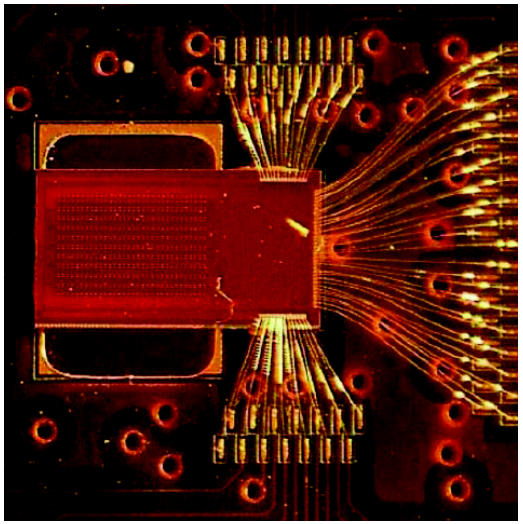
ToPix (Torino Pixel Asic): 130 nm CMOS technology.
Position, time, energy measurement.
Final version will consist of 116 x 110 pixel matrix arranged in 55 double columns.
Current prototype: version 4, reduced size prototype 3 x 6 mm^2.
640 cells with pixel cell divided into 4 double columns.

Self trigger capability	
Pixel size	100 μm x 100 μm
Chip active area	11.4 mm x 11.6 mm
dE/dx measurement	ToT - 12 bits dyn.range
Max input charge	50 fC
Input clock frequency	160 MHz
Time resolution	6.25 ns
Power consumption	$< 800\ mW/cm^2$
Max hit rate	$6.1 \times 10^6/cm^2$
Total ionizing dose	$<$ 100 kGy

Readout ASIC: ToPix

Pixel Part





Performance Measurements

Pixel part

- Reduced size prototype of ToPix extensively tested;
- analog performances satisfy the requirements;
- correct operation at nominal frequency of 160 MHz;
- possible improvement on the data transmission;
- radiaton tolerance suitable to withstand the PANDA foreseen levels.

Pixel Modules

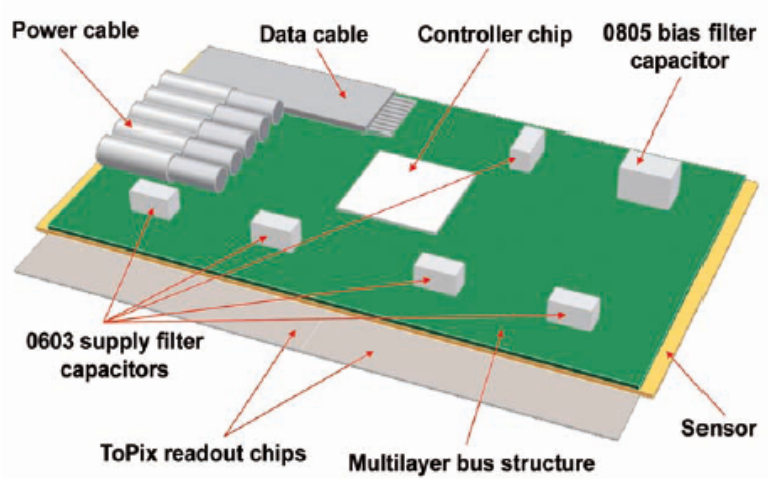
Pixel Part

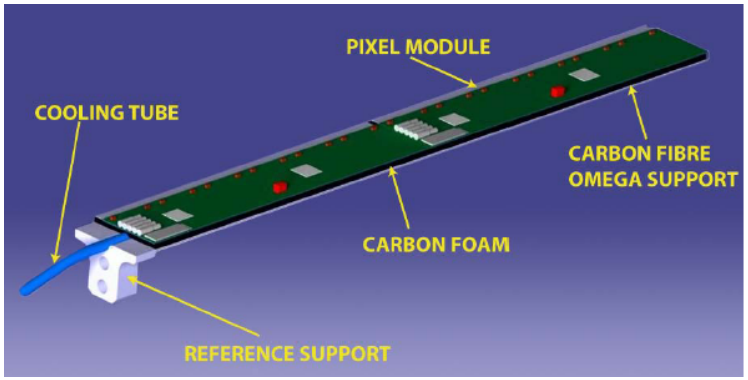
Sensor module:

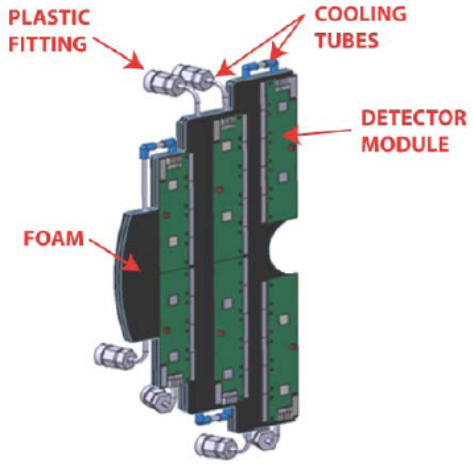
- one sensor;
- 2 to 6 ToPix chips;
- multilayer bus.

Mechanical structure:

- 42 carbon fiber staves on the barrel;
- 12 carbon foam half-disks.



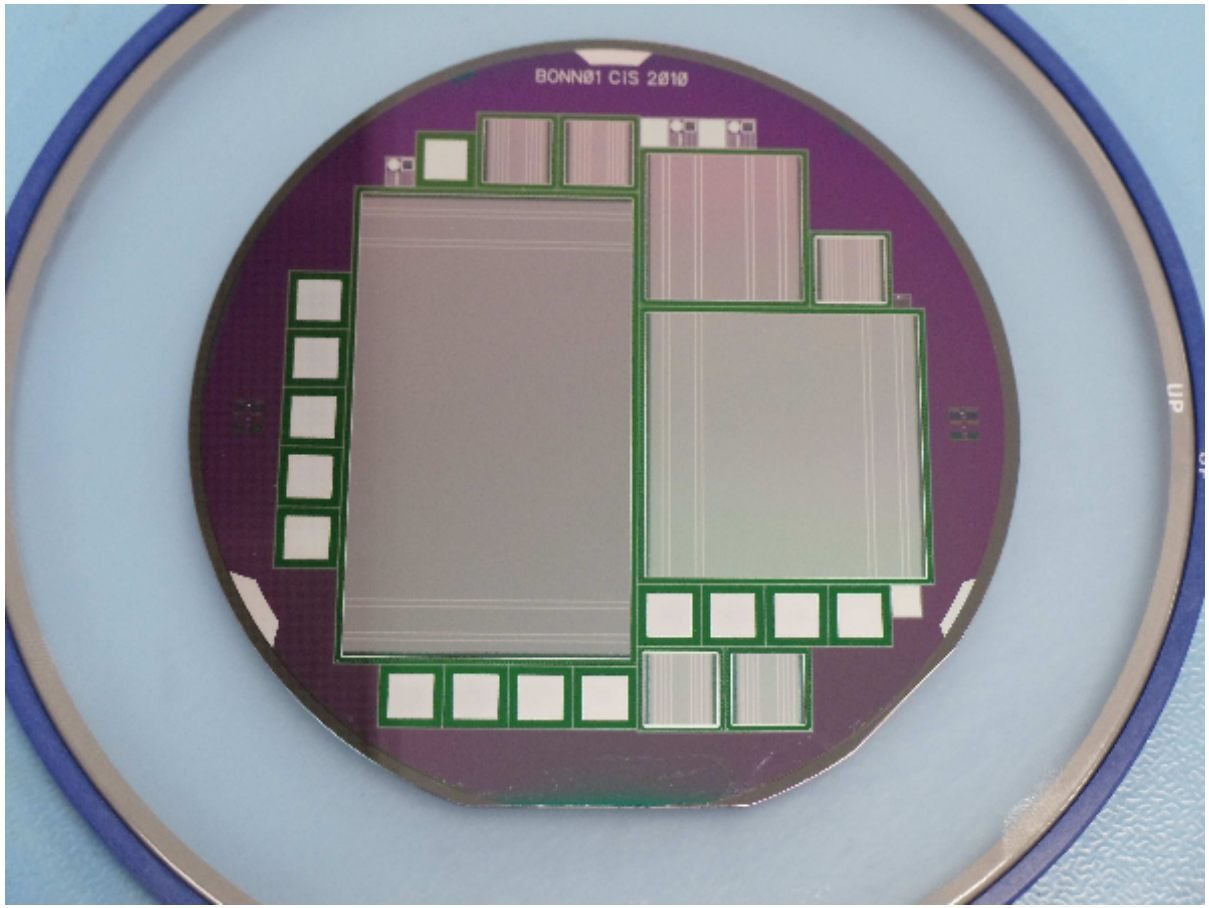




Sensors Characteristics

Strip Part

Two prototype run at CiS GmbH, Erfurt, with different biasing techniques.
Extensive studies on QA carried out.

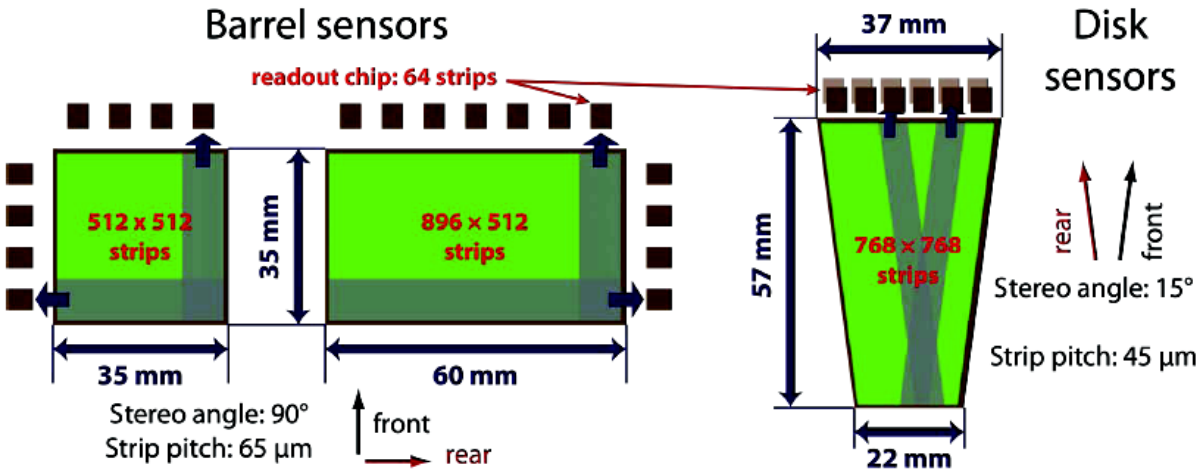


Sensors Arrangement

Strip Part

Three different strip sensors shapes, same thickness of 285 μm:

- squared and rectangular → barrel;
- trapezoidal → disks.



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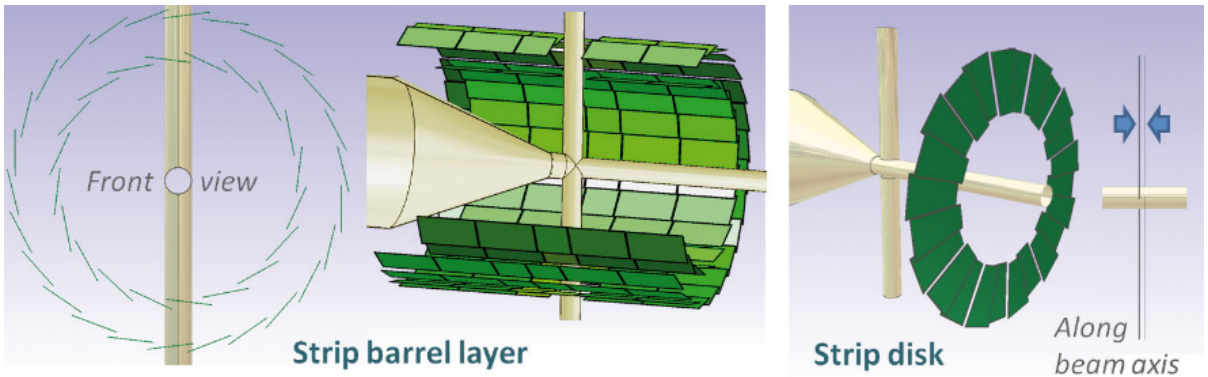


Readout ASIC: PASTA

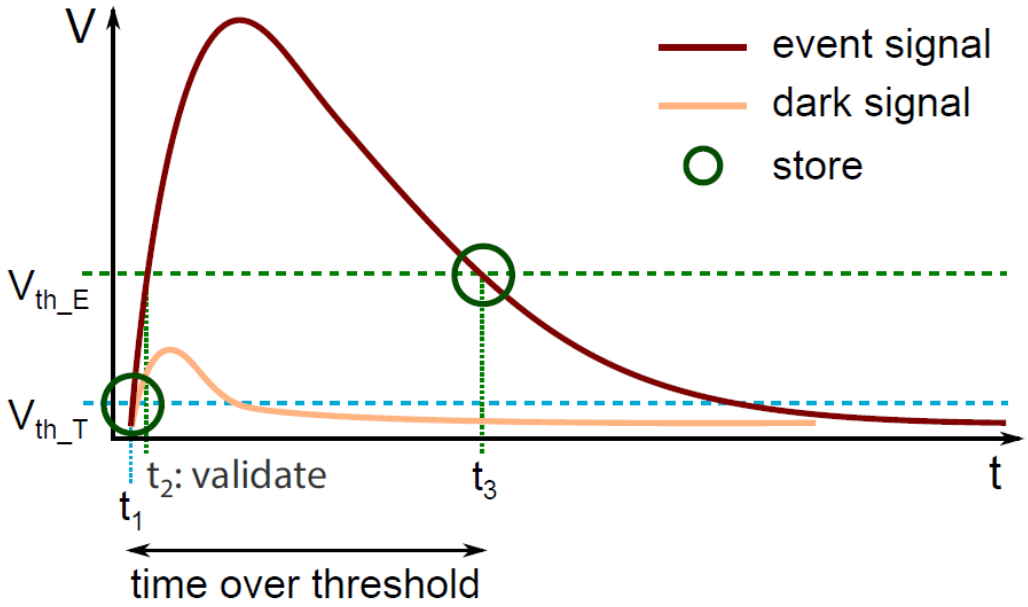
Strip Part

PASTA (Panda Strip ASIC): 110 nm CMOS technology.
Concept based on TOFPET ASIC.

- Developed for medical application for SiPM readout.

Time over threshold measurement based on two leading-edge discriminators.

- Low threshold - time branch: resolve leading edge of pulse (time stamp resolution).
- High threshold - energy branch: reduce jitter on the falling edge.

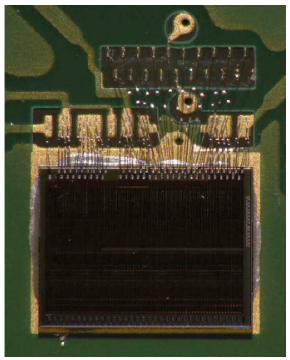


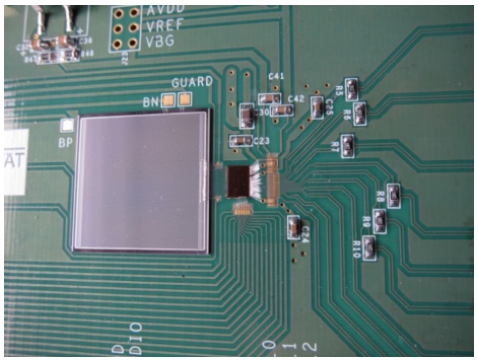
Readout ASIC: PASTA

Strip Part

First version of prototype fabricated with a Multi Project Wafer run.
Currently under evaluation.

Self trigger capability	
Input capacitance/charge	Si Strips: 50 pF / 38 fC
Power consumption	< 4 mW/ch
Channel pitch	63 μm
Radiation tolerance	100 kGy
Efficiency gap	no evt loss
Charge resolution	8 bit dyn. range
Time resolution (coarse)	6.25 ns
Time resolution (fine)	∼ 50 ps





Performance Measurements

Measurement to characterize the chip are currently ongoing:

- in the laboratory;
- under beam (next fall).

- Focus on the coarse information for both time and energy branch.
- No detailed studies on the fine time yet.
- Operation frequency is half of the nominal one (i.e., 80 MHz).

Module Data Concentrator - MDC

Strip Part

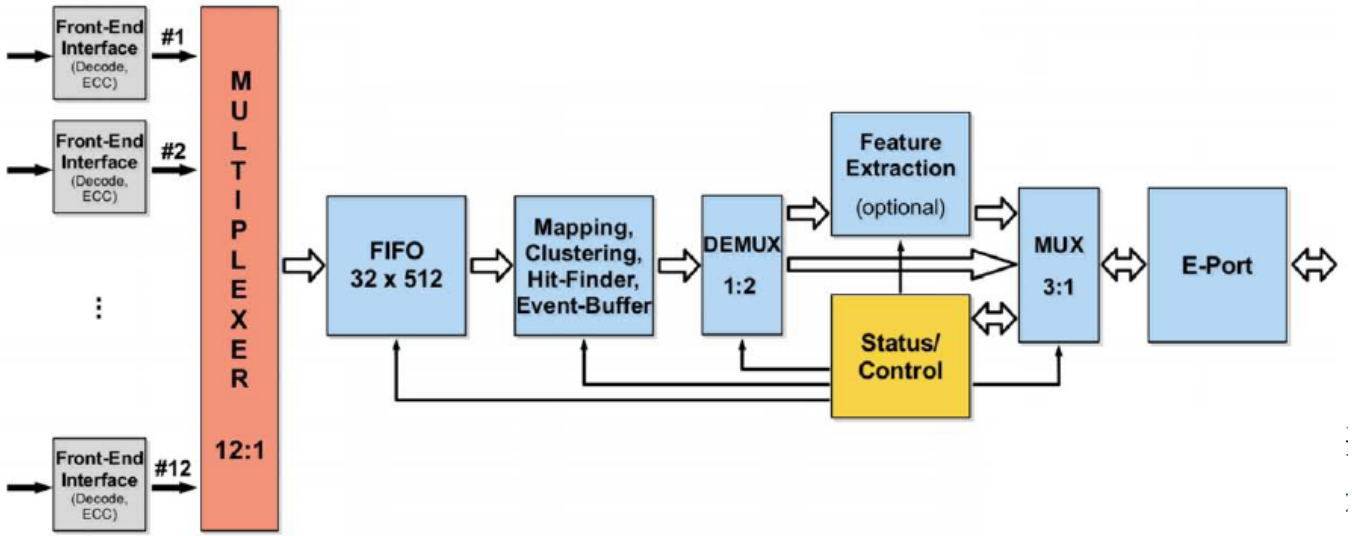
Link between the front-end chips and the MVD DAQ.

Main tasks:

- readout, decoding, multiplexing of front-end of one sensor (up to 12 inputs);
- buffering, pedestal subtraction, clustering (optional);
- slow control and monitoring.

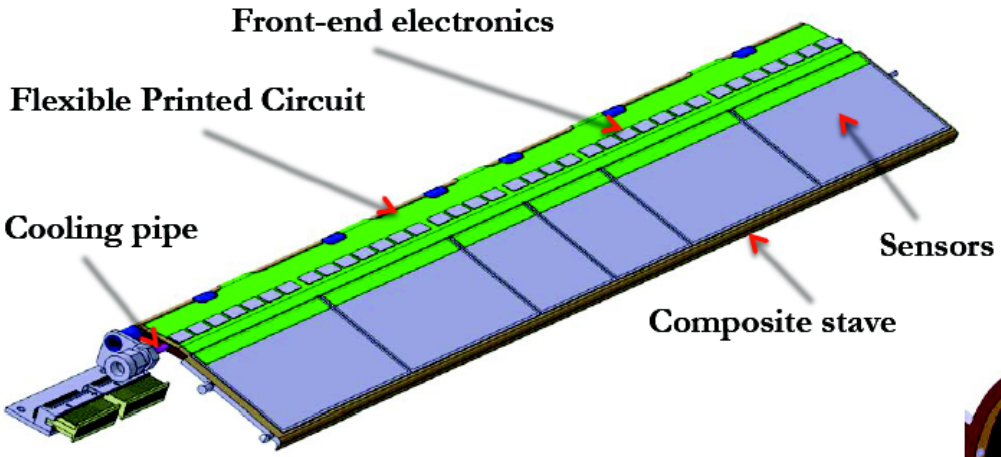
Final implementation on an ASIC.

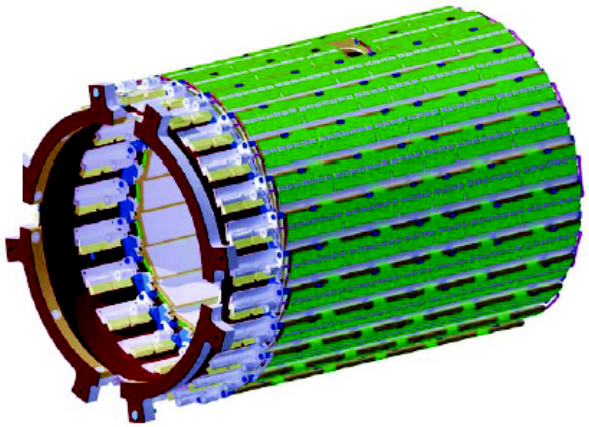
Currently under prototyping on FPGA.

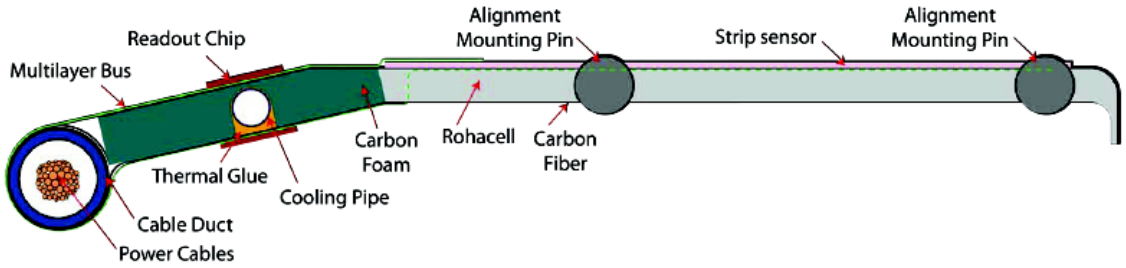


Strip Modules: Barrel

Strip Part



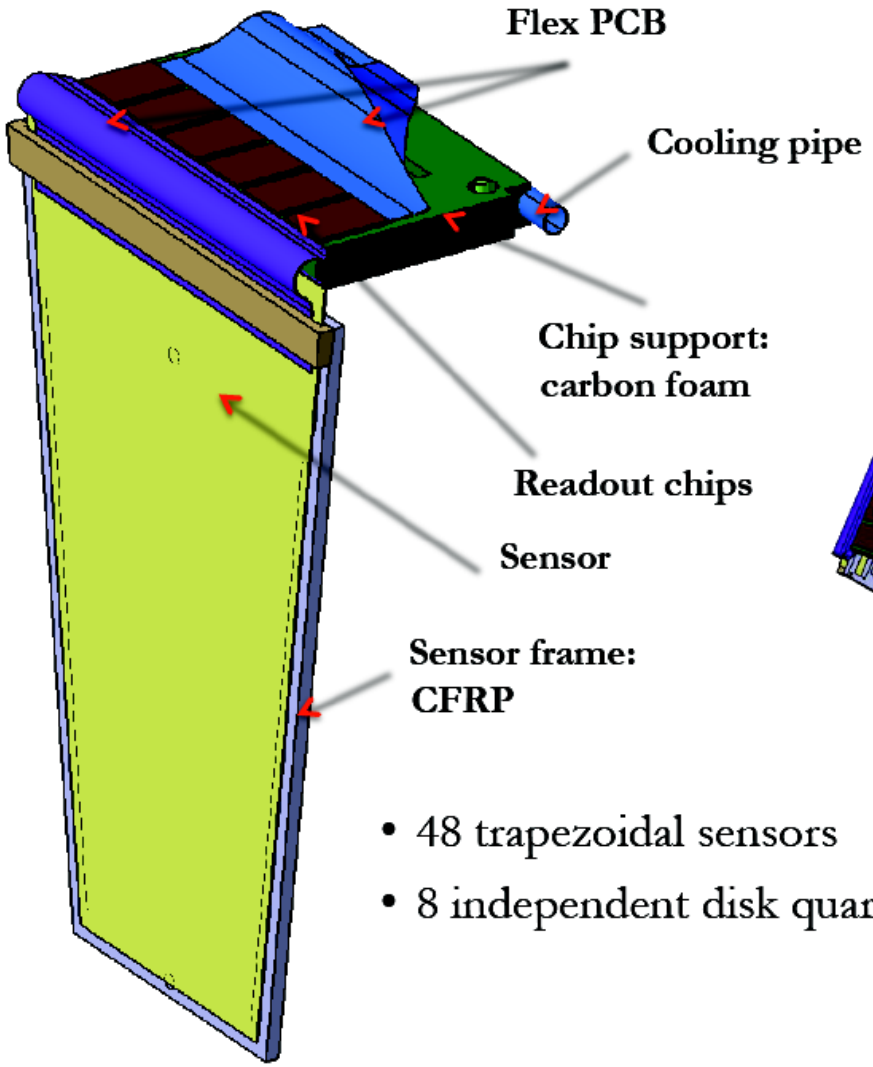


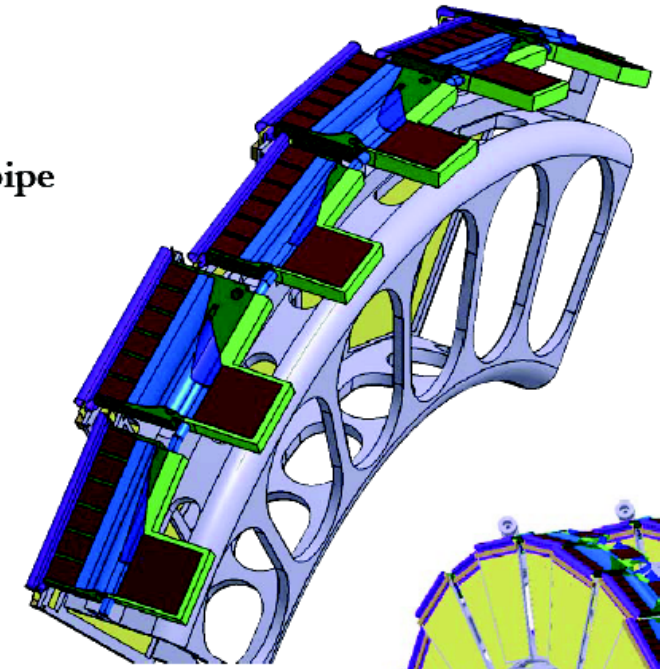


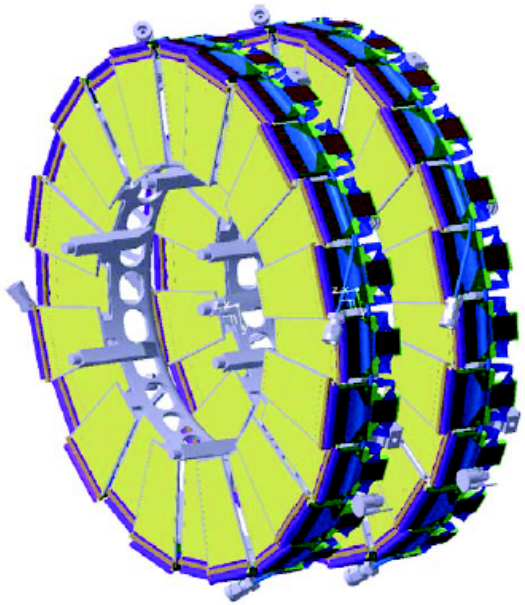
Studies on the cooling system concept prove it works.

Strip Modules: Disks

Strip Part







- 48 trapezoidal sensors
- 8 independent disk quarters on 2 disks

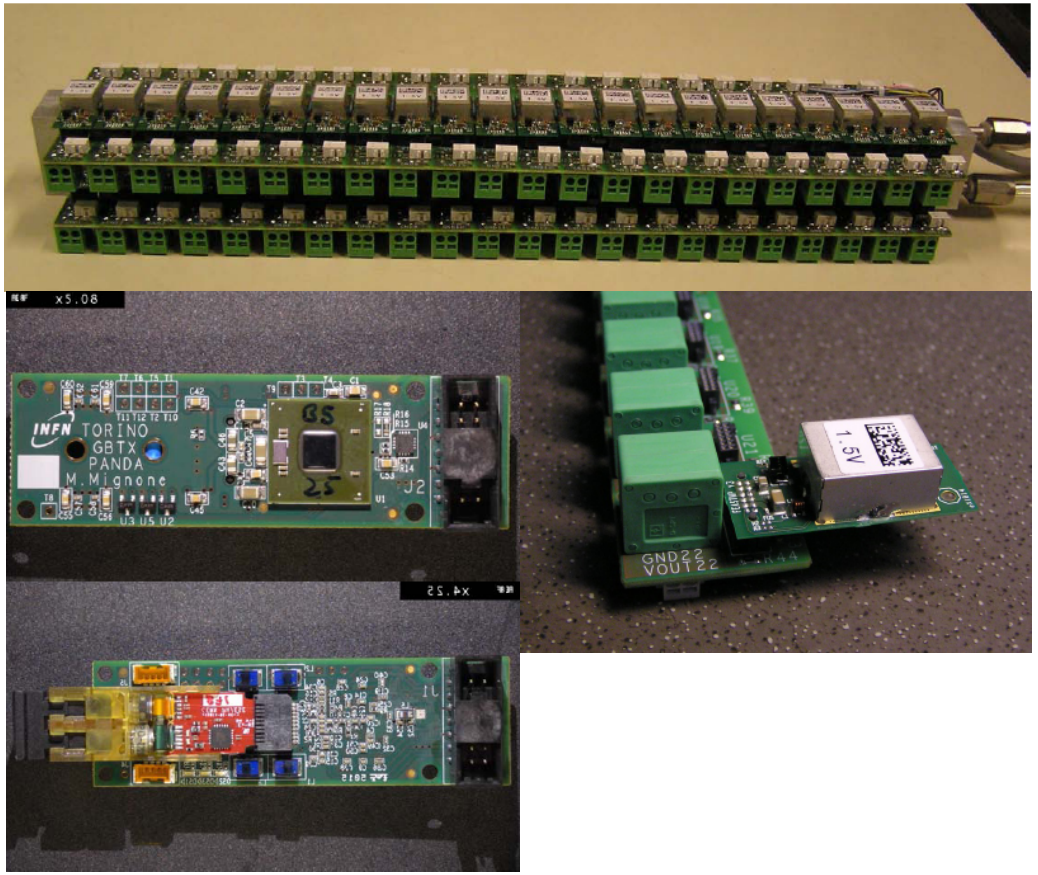
Services

Prototypes

Services are arranged around the beam pipe:

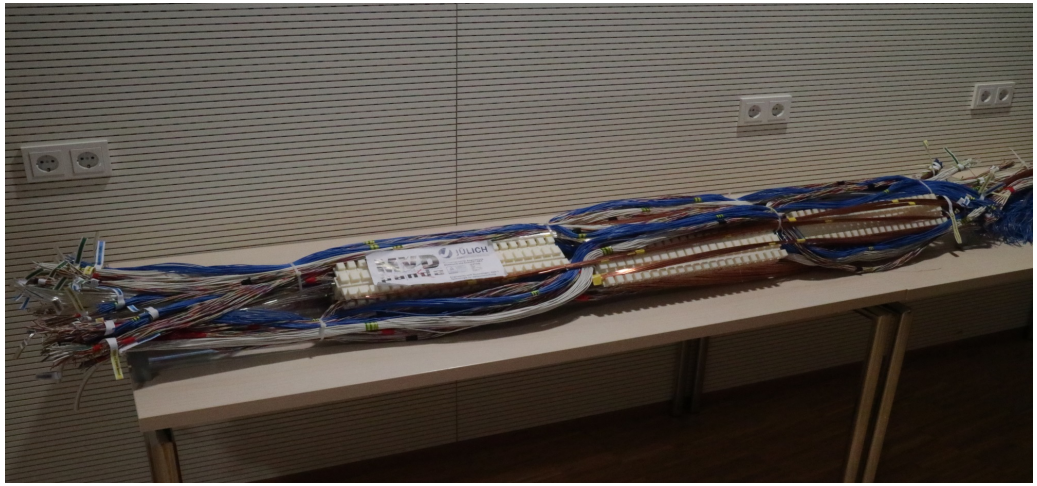
- DC-DC powering operating in magnetic field B = 2 T $\rightarrow\sim$ 2100 DC-DC converters;
- $\sim$ 200 GBT boards for electro-optical conversion of signals.

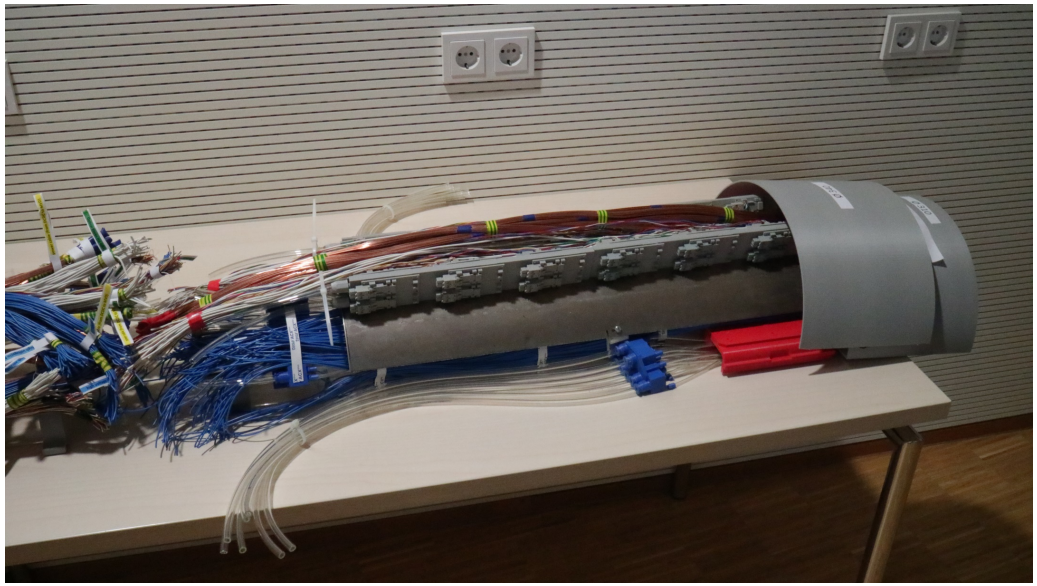
Prototypes currently under test.



Services

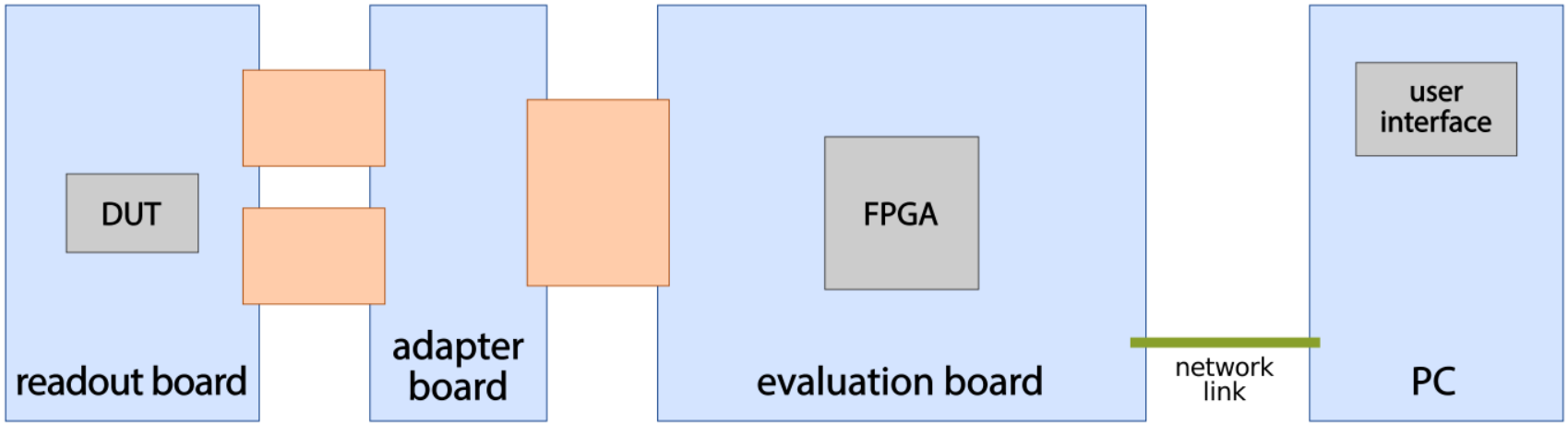
Mock up





JDRS: Jülich Digital Readout System

The basic components



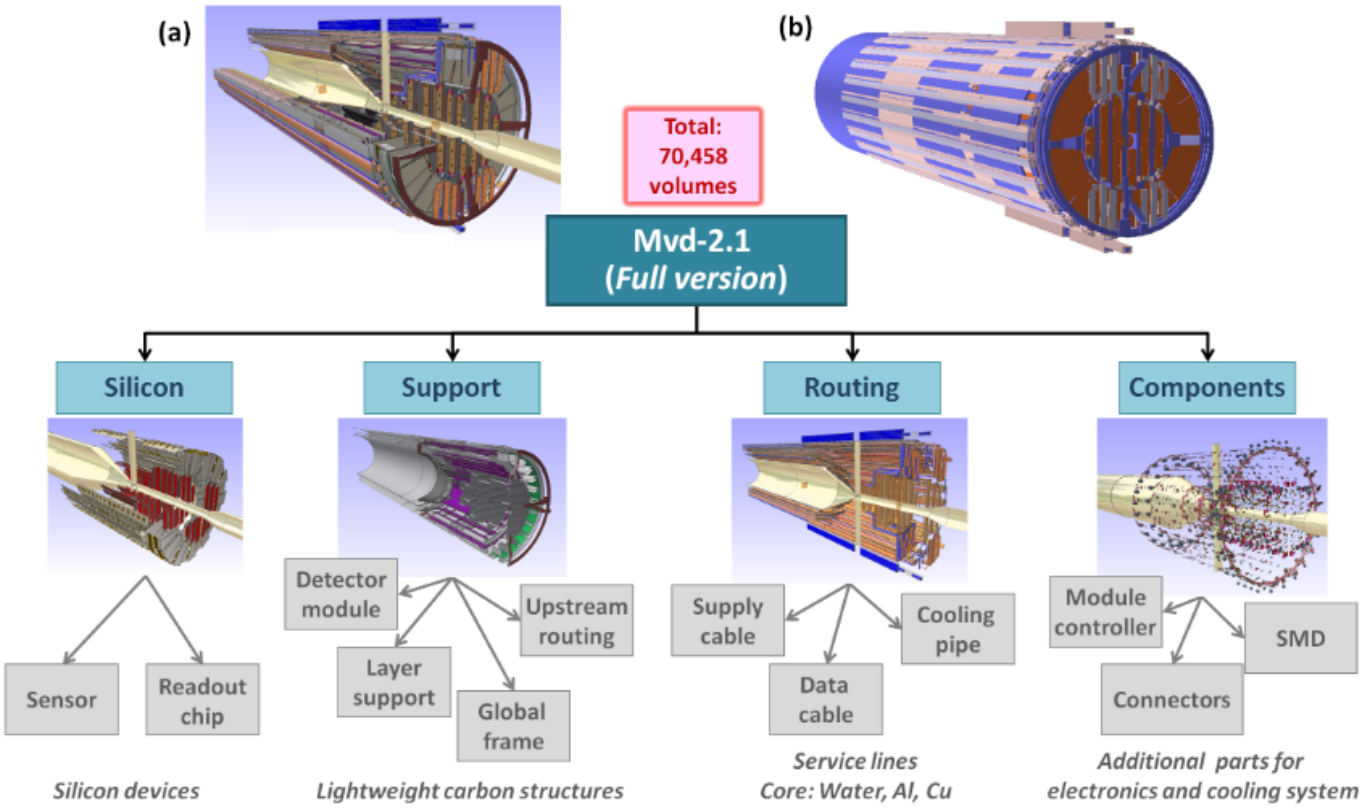
Data conversion and communication with the PC:

- DUT: ToPix, PASTA
- evaluation board: Xilinx ML605 (Virtex-6 FPGA)
- firmware: VHDL

Configuration and data handling:

- PC
- software: C++
- MVD Readout Framework (MRF)
- Qt-based GUI

CAD model



(a) Before conversion from technical CAD to ROOT geometry.
(b) After conversion from technical CAD to ROOT geometry.

Simulations

Extensive simulations to aid design and optimization of the MVD:

- PID and separation power;
- radiation tolerance;
- detector coverage;
- material budget;
- benchmark channels to test analysis tools.

Present Status

- The development of the Pixel part is momentarily partially on hold.
- Waiting for a definitive answer from INFN concerning funds for the pixel projects.
- Technology change needed for the next iteration of the pixels' readout chip, probably 110 nm UMC.
- Since the developers of PASTA are no longer available:
  development of a new strip readout chip in the (near) future in Torino, taking advantage of a new project.

Conclusion

- The development of the MVD is in andvanced stage, but there are still important task to be completed.
- The progresses are currently affected by a severe lack of manpower and difficult situations especially @IKP-FZJ and @INFN Torino.
- The present idea is to concentrate the efforts of the MVD group on the development of the strip barrel part, without excluding the possibility of resuming the pixel activities, if INFN will support with funds.

Backup

Time amplification

i.e. how to get the enhanced resolution.

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5.5.1.2 Time Amplification

The ASIC has an internal counter incremented by the clock to generate time stamps. Just using this counter to time events would lead to a precision based on the clock's period, or 6.25 ns for an input clock of 160 MHz. With the chosen scheme of converting the phase between a trigger and the clock into a proportional voltage drop and then recharge this, a time amplification is gained.

Two factors influence this amplification: a larger capacitance for the second capacitor

$$C_{\mathrm{TDC}} = 4 \cdot C_{\mathrm{TAC}} \tag{5.2}$$

and a lower recharging current

$$I_{\mathrm{TDC}} = {}^{1}/_{32} \cdot I_{\mathrm{TAC}} \,. \tag{5.3}$$

Using the relation for charge in a capacitor and constant currents

$$C \cdot U = Q = I \cdot t$$

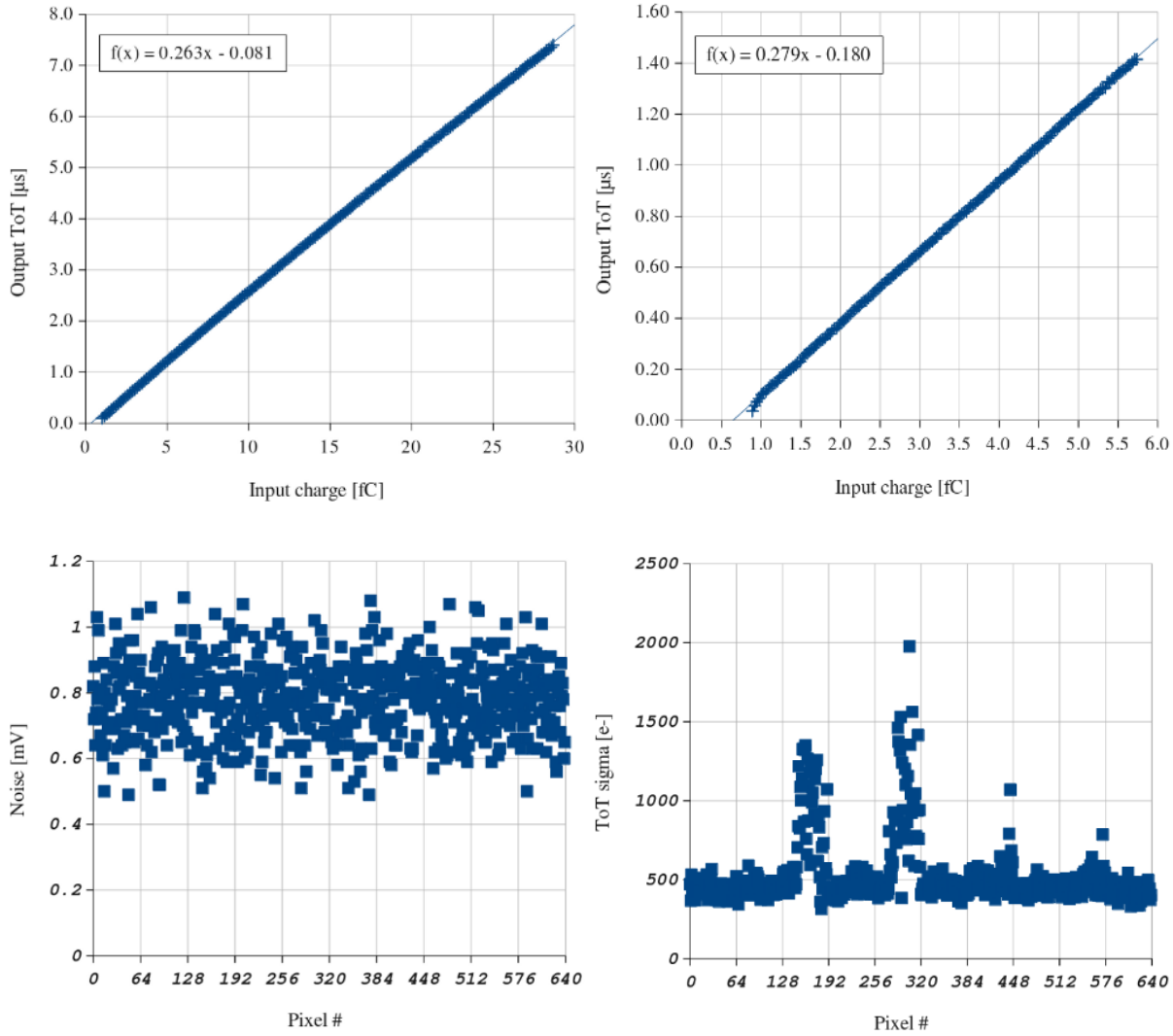
one gets the gain of this method for the time after the process (t_{TDC}) versus the time before (t_{TAC}) by assuming the voltage level is equal after connecting both capacitors:

$$\begin{aligned} \frac{I_{\mathrm{TAC}} \cdot t_{\mathrm{TAC}}}{C_{\mathrm{TAC}}} &= U_{\mathrm{TAC}} = U_{\mathrm{TDC}} = \frac{I_{\mathrm{TDC}} \cdot t_{\mathrm{TDC}}}{C_{\mathrm{TDC}}} \\ \Rightarrow \quad t_{\mathrm{TDC}} &= t_{\mathrm{TAC}} \cdot \frac{I_{\mathrm{TAC}}}{I_{\mathrm{TDC}}} \cdot \frac{C_{\mathrm{TDC}}}{C_{\mathrm{TAC}}} \\ \overset{(5.2)\,\&\,(5.3)}{\Rightarrow} \quad &= t_{\mathrm{TAC}} \cdot 32 \cdot 4 = t_{\mathrm{TAC}} \cdot 128 \,. \end{aligned} \tag{5.4}$$

ToPix Measurements

Pixel Part

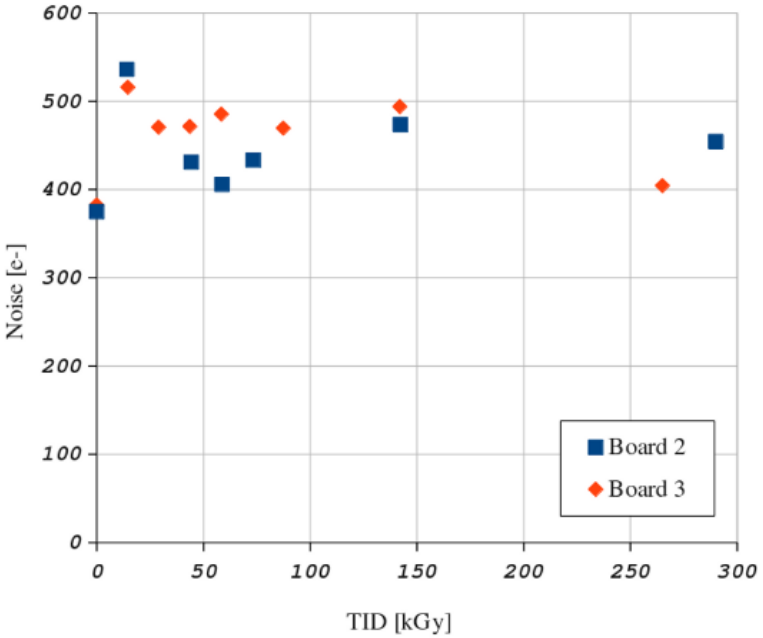
Linearity and noise studies.

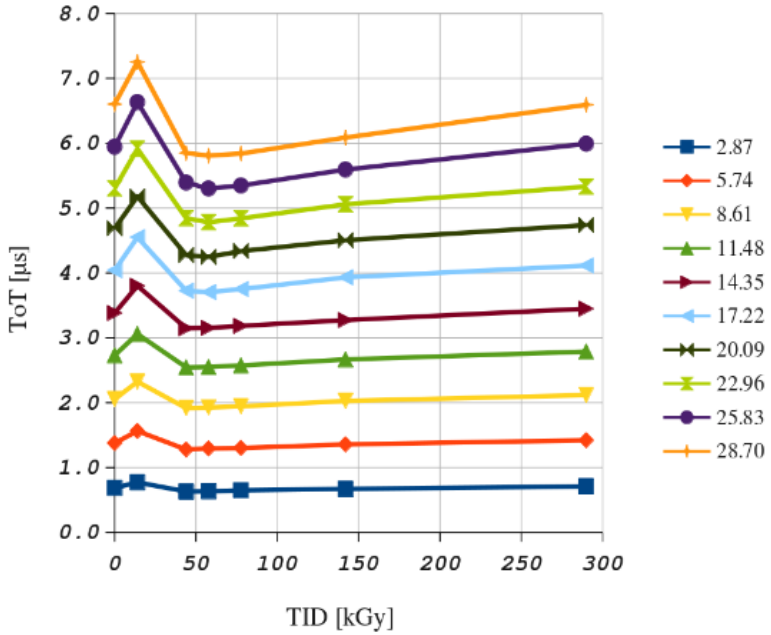


ToPix Measurements

Pixel Part

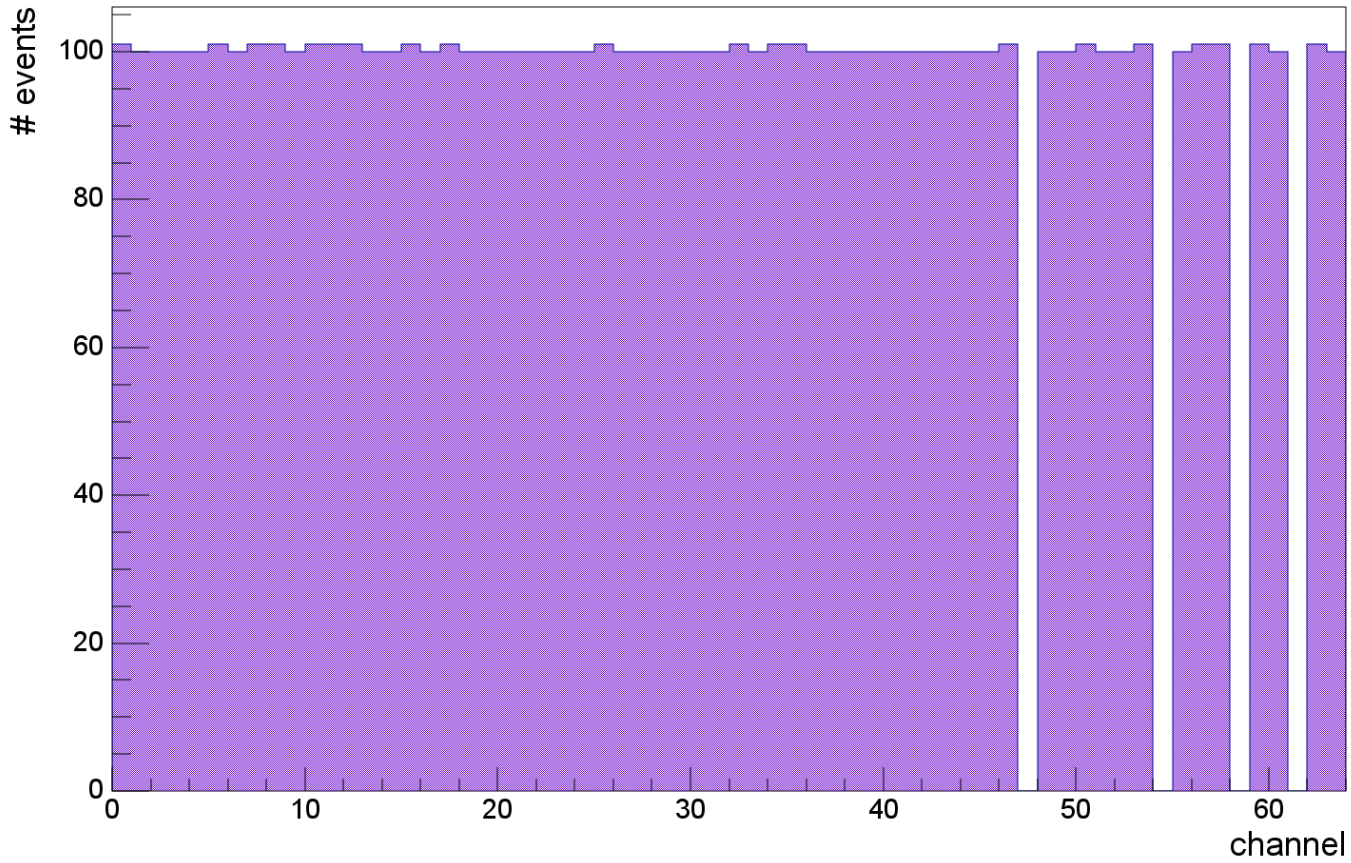
Radiation tolerance studies.





PASTA: Channel Response

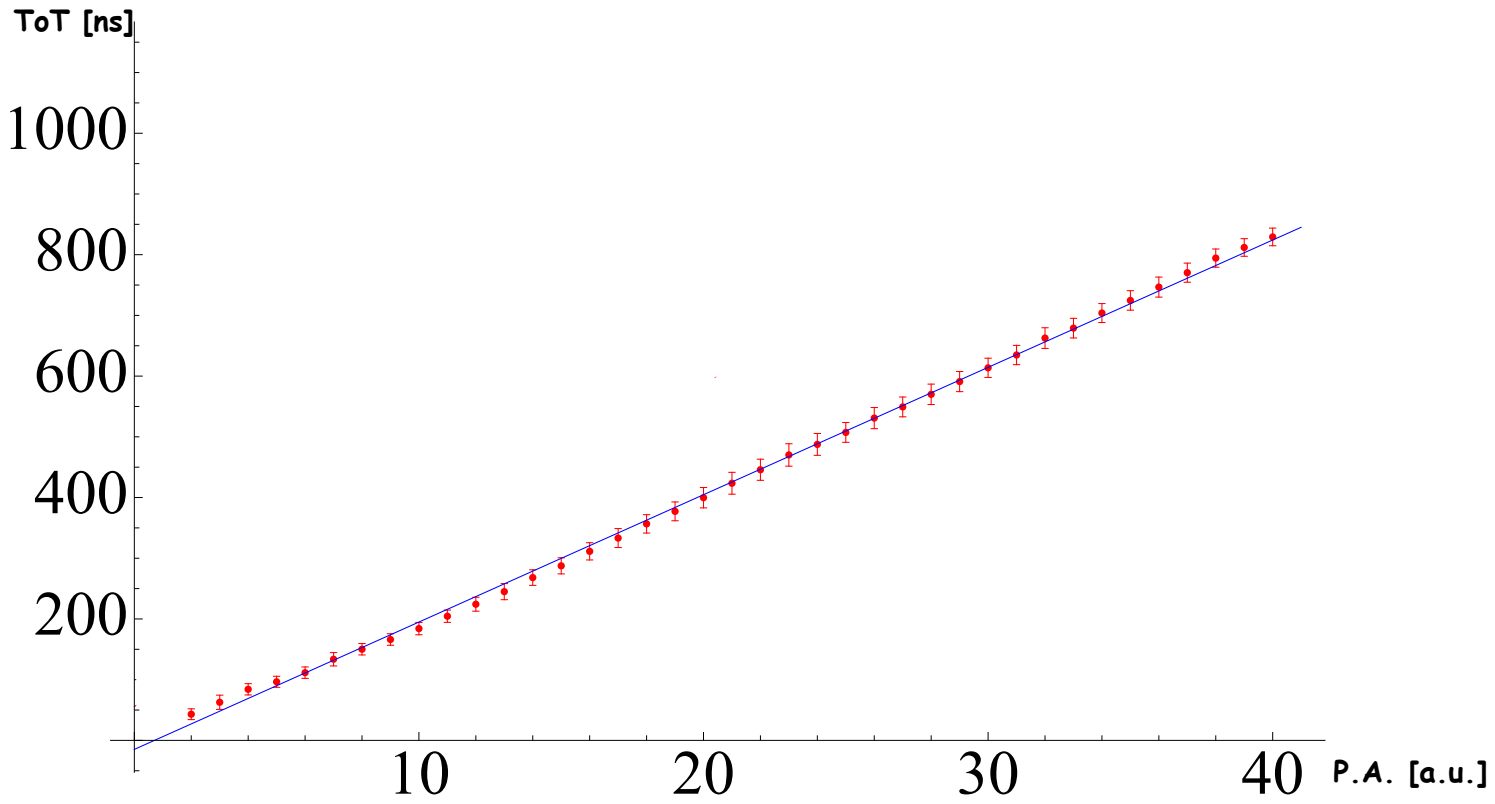
Scan of all the channels for fixed amplitude.



Not all the channels are responsive.

PASTA: ToT Linearity

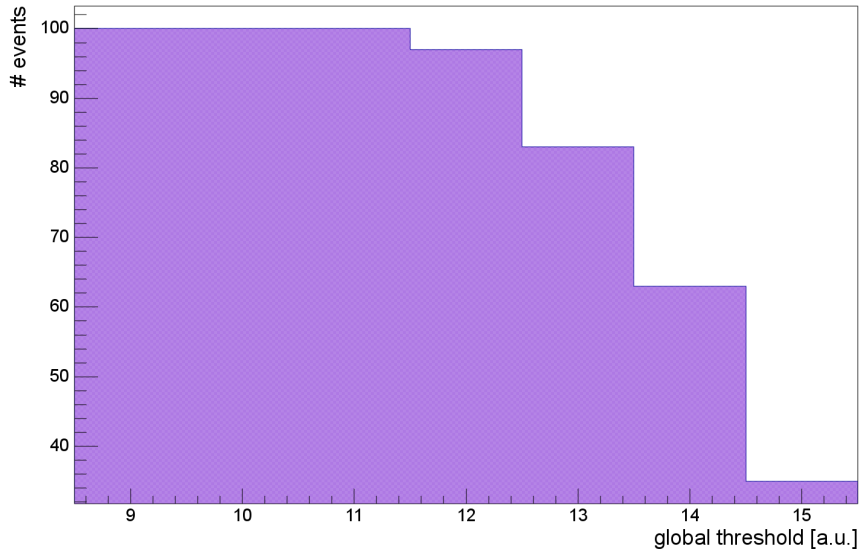
Scan of all the channels within a given amplitude range.
Only coarse information used.
$ToT = t_{coarse_E} - t_{coarse_T}$



PASTA: Threshold determination

Amplitude incoming signal $>$ threshold $\longrightarrow$ signal detected

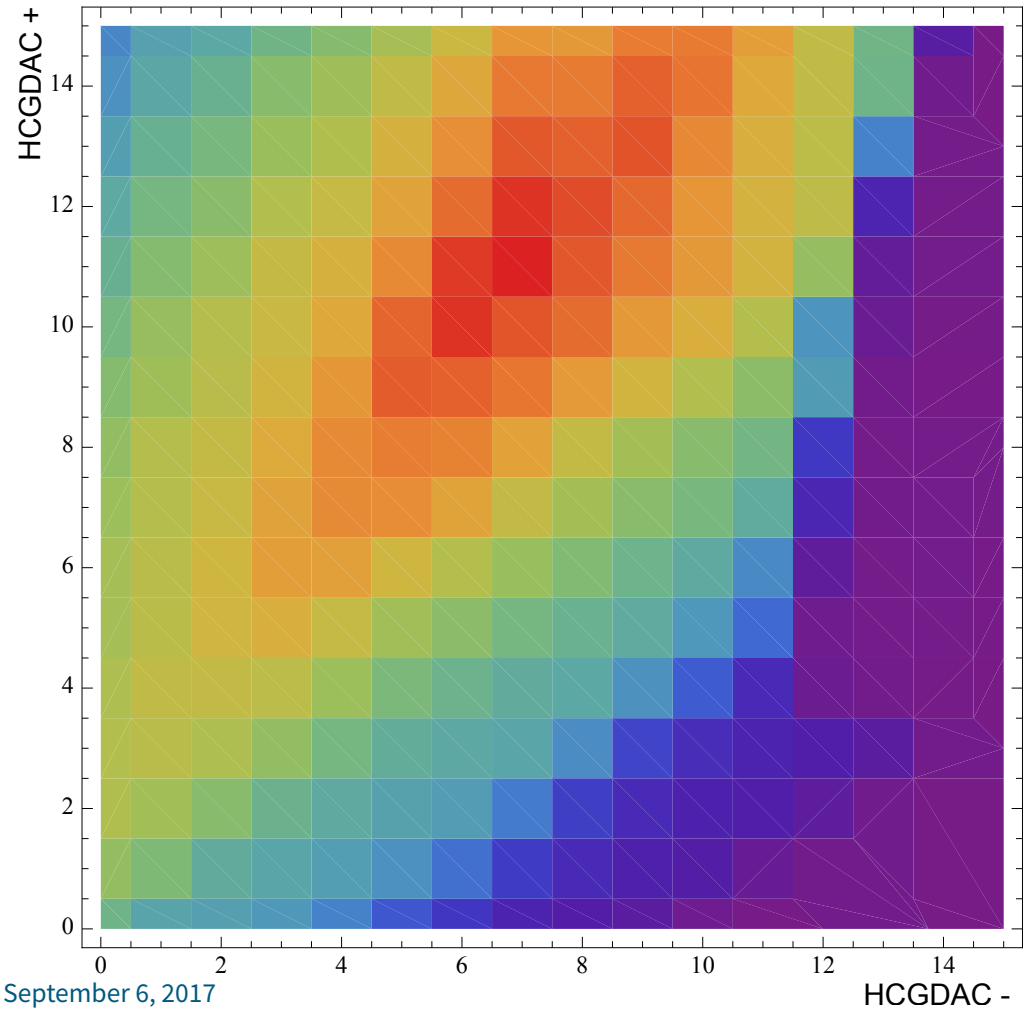
- Global threshold: $\Delta_{th} = HCGDAC_{+} - HCGDAC_{-}$
  $\longrightarrow$ midvalue of an interval with predefined amplitude.
- Local threshold: fine tuning.
- Sweep over Δ_{th} at fixed pulse amplitude $\rightarrow$ expected: S-curve shape.



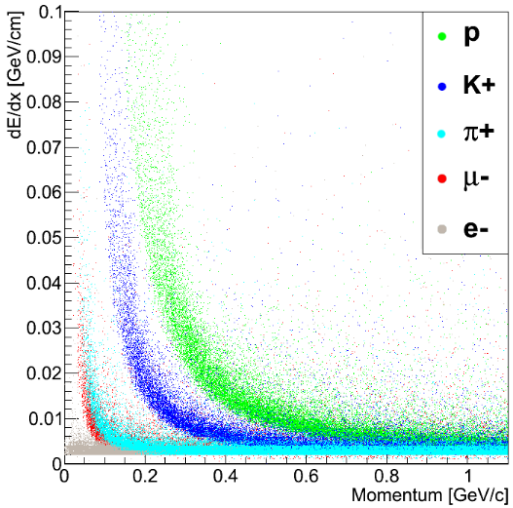
- S-curve structure only for some channels
  $\longrightarrow$ box distribution even for small amplitudes.
- Different optimal values for different channels.

PASTA: Threshold distribution

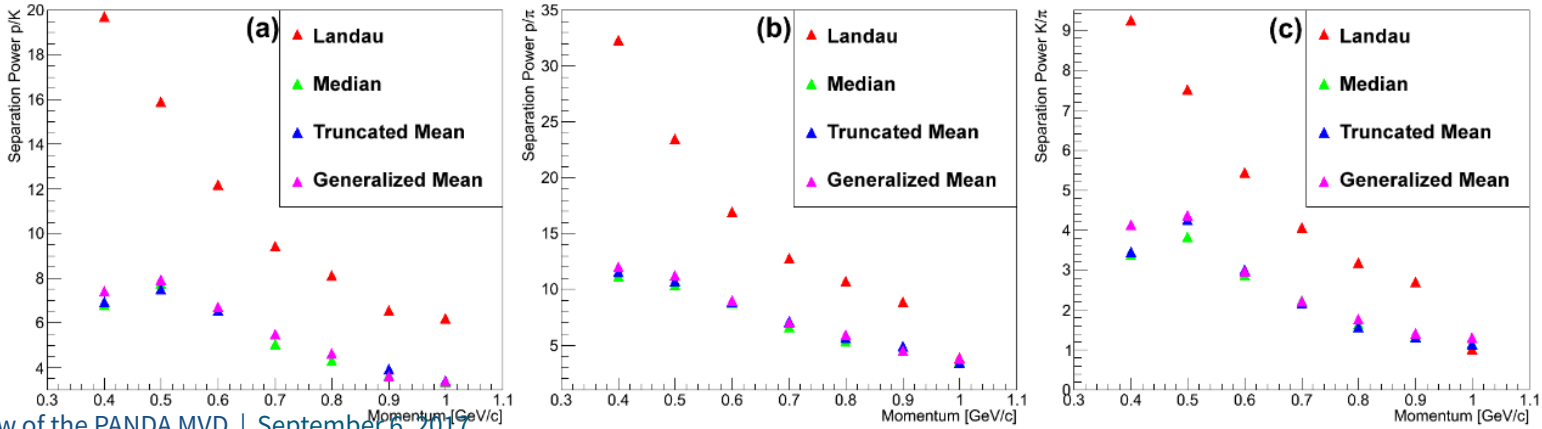
Find the combination of $HCGDAC_+$ and $HCGDAC_-$ to maximize nEv.
Fixed pulse amplitude.



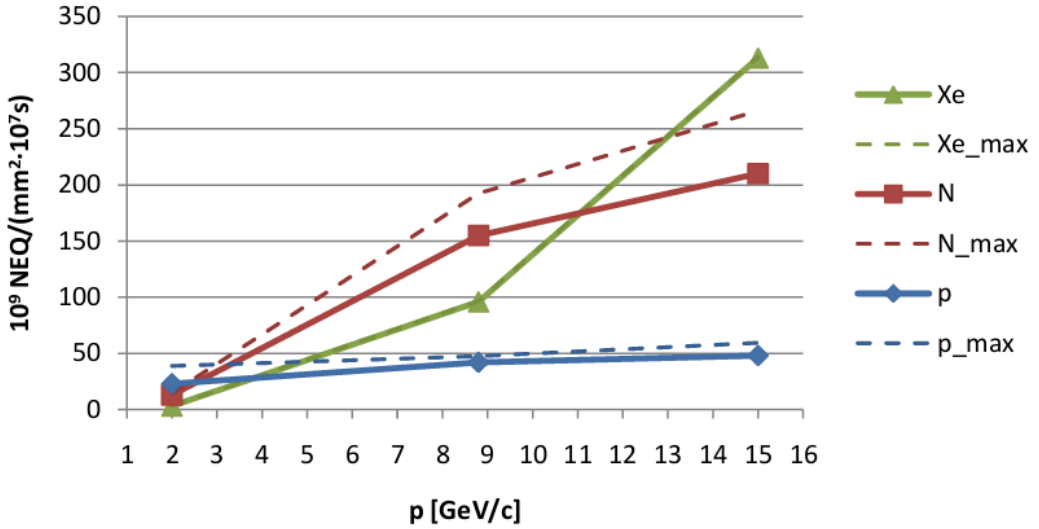
Simulations: PID with MVD



$$SP = \frac{|< dE/dx_{p1} > - < dE/dx_{p2} >|}{\sigma_{p1}/2 + \sigma_{p2}/2}$$



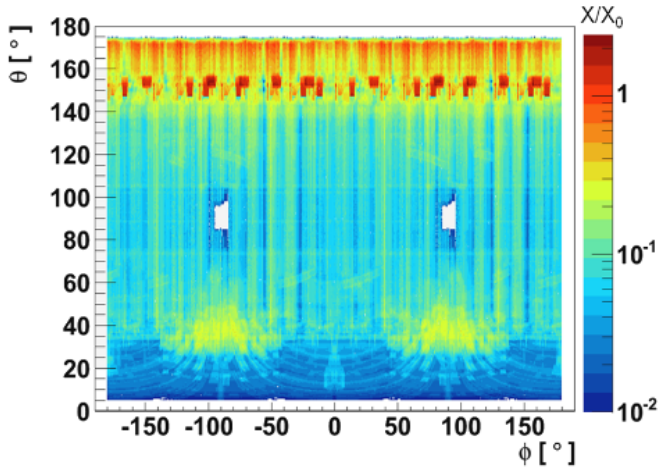
Simulations: Rad-Hard studies

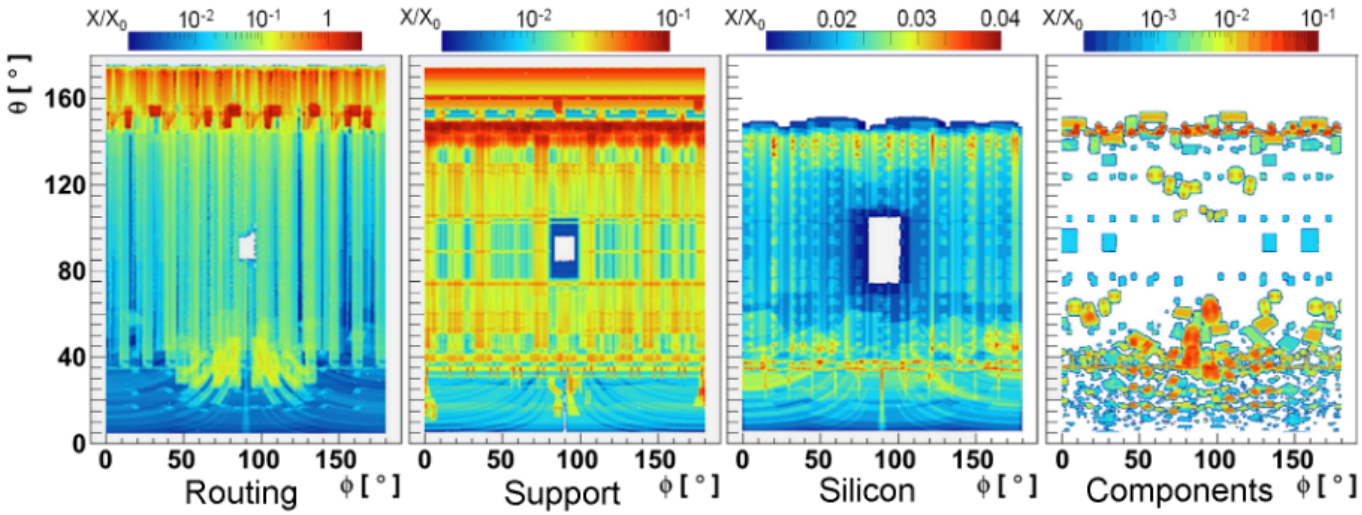


Simulations: Material Budget

Fractional radiation length:

$$X/X_0 = \sum_j \frac{\rho_j \cdot L_j}{X_{0_j}}$$



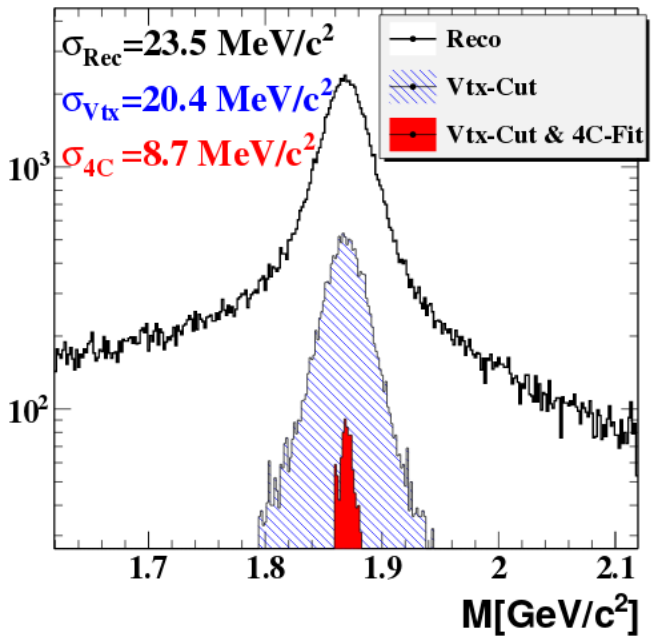


Stronger contribution to material budget: cabling and support.

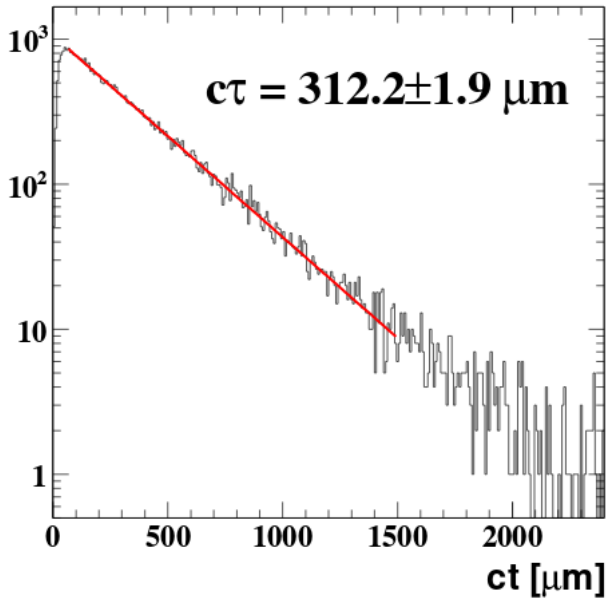
Simulations: Benchmark Channel

$\bar{p} \rightarrow D^+D^- \rightarrow K^-\pi^+\pi^+K^+\pi^-\pi^-$

Invariant mass



Decay length



PDG value: $c\tau = 311.8\ \mu m$