# Update of BWEC Activities

Oliver Noll

$\bar{\text{P}}$ANDA-Collaboration Meeting 17/3

September 2017

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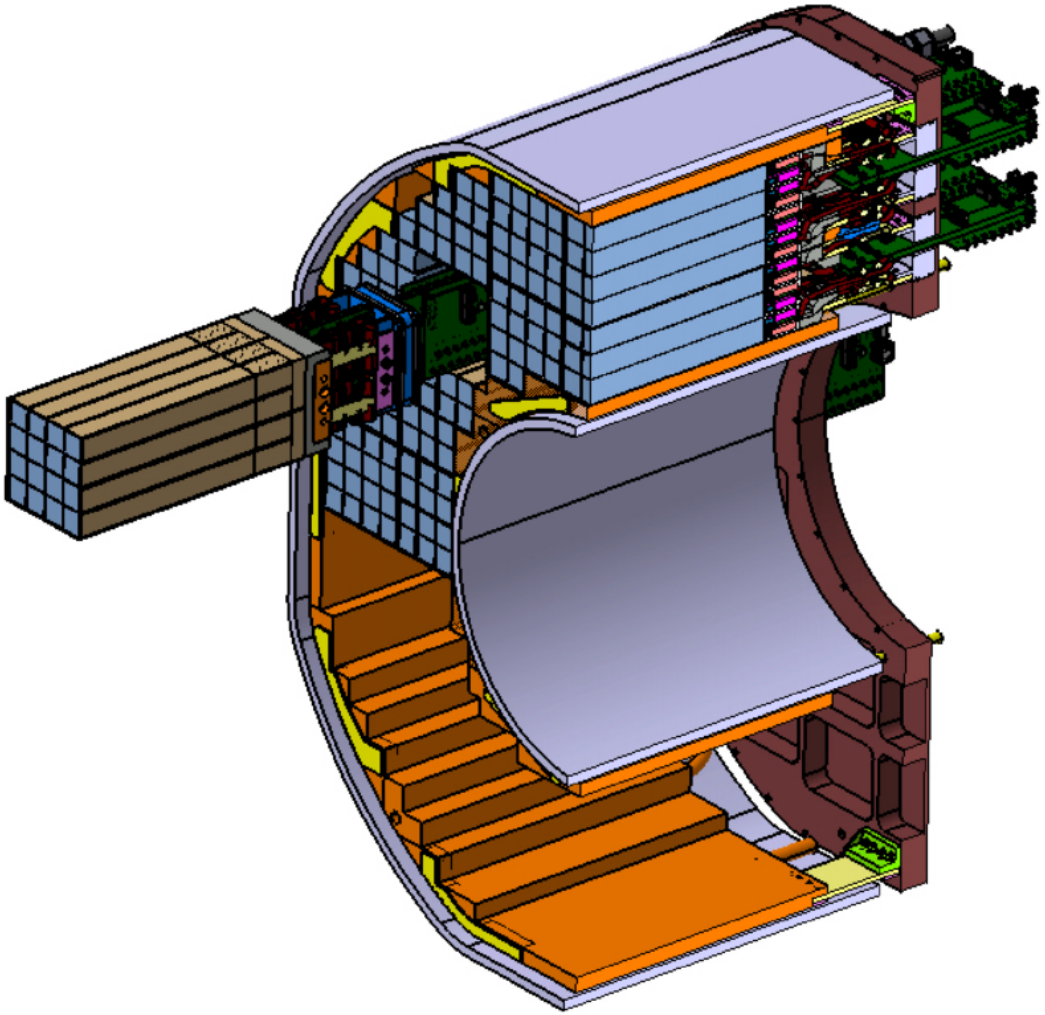
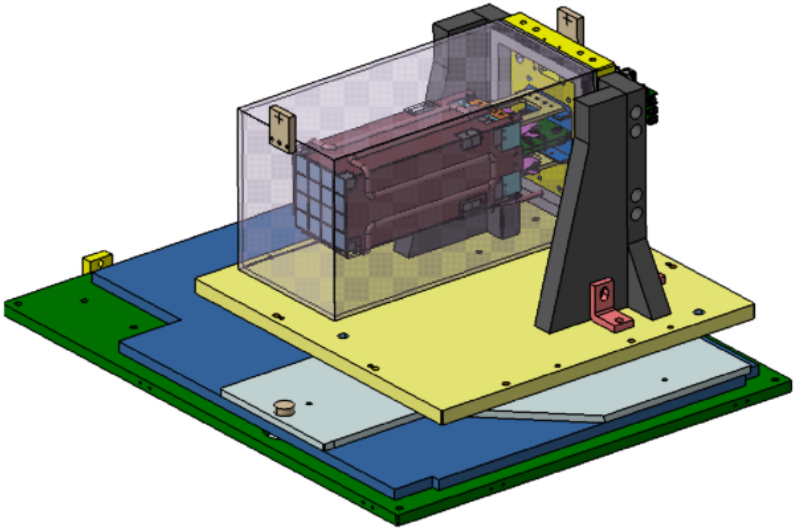
# BWEC News

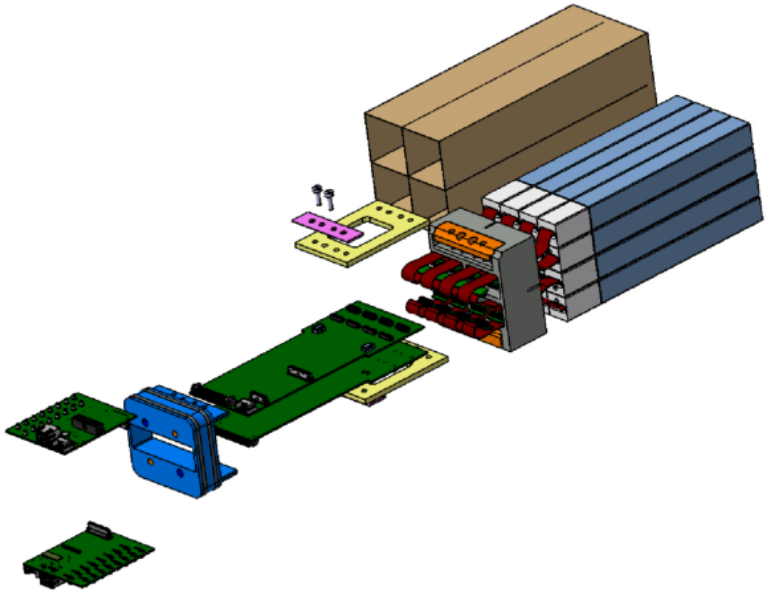


# PROTO16-2

## PROTO16-2

- Test of latest BWEC subunit design
- New parts are in production
- New front end electronics is currently being tested

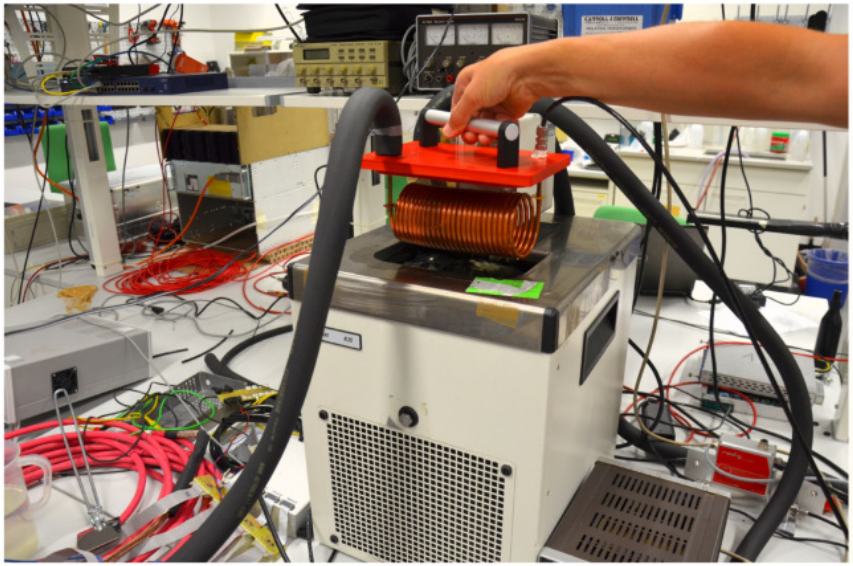


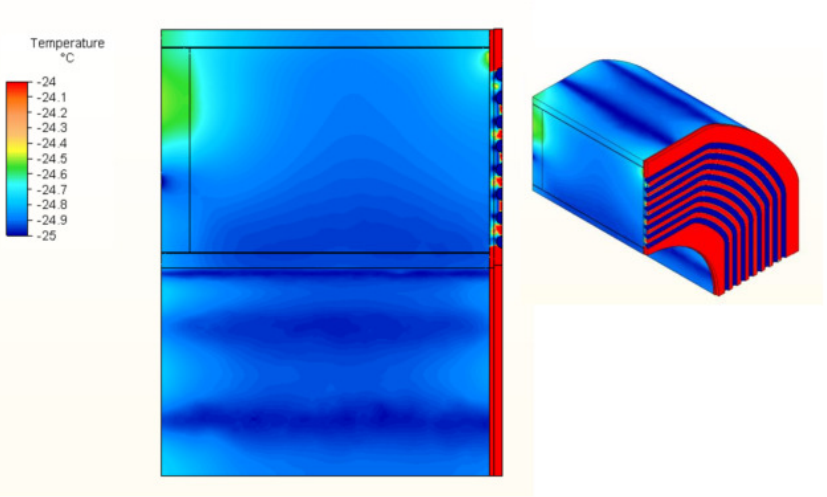


# Cooling Tests

## Cooling Tests (see contribution from David)

- FEM simulations are done
- Tests with PROTO16-1
- Nitrogen cooling
- Front cooling

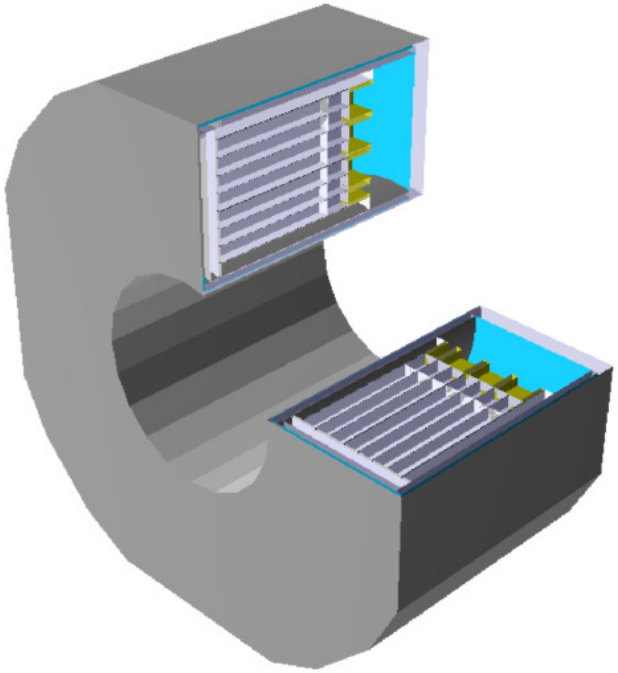


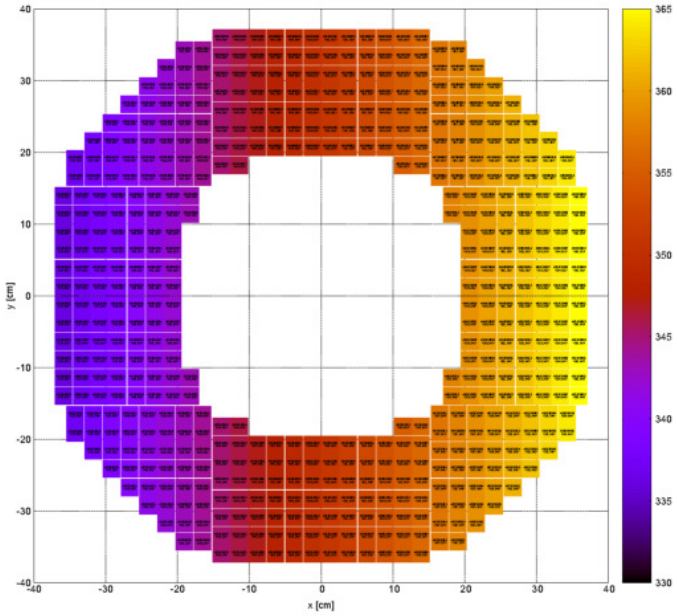


# P̄ANDA ROOT Implementation

## P̄ANDA ROOT (computing session contribution from Luigi)

- Implementation of BWEC is done
- Also dead materials
- Now crystal numbering is done

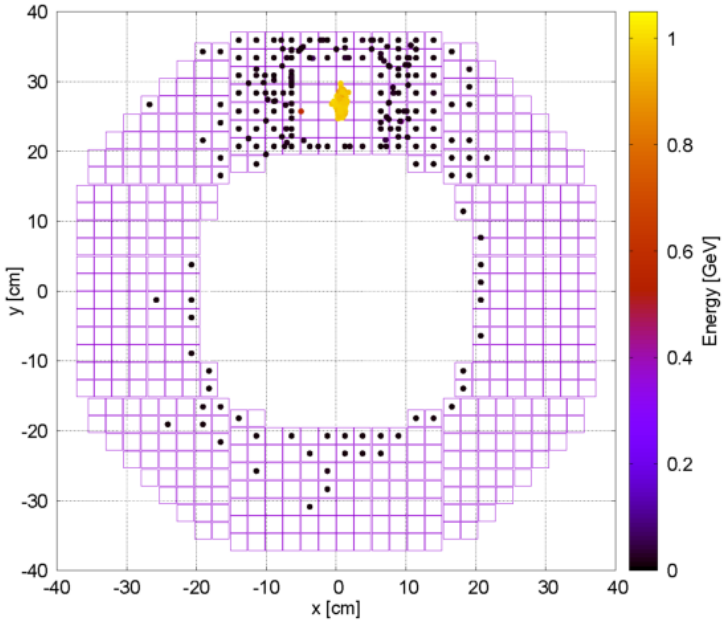


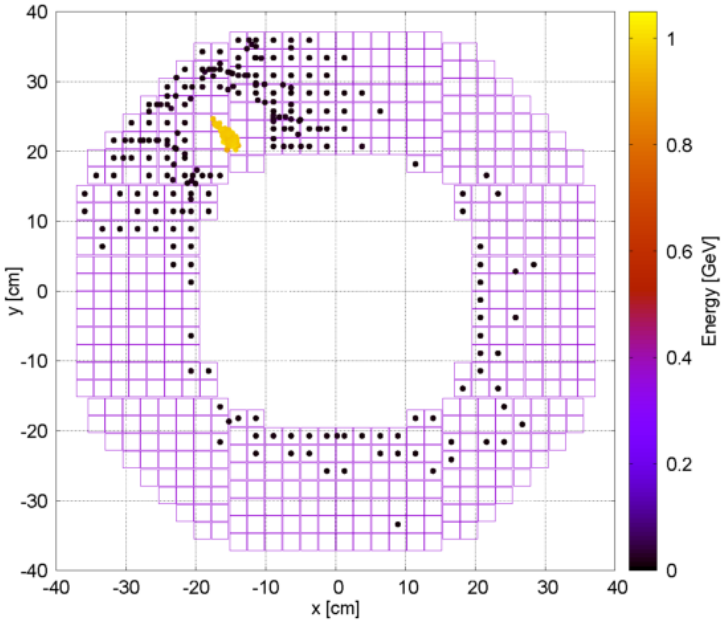


# P̄ANDA ROOT Implementation

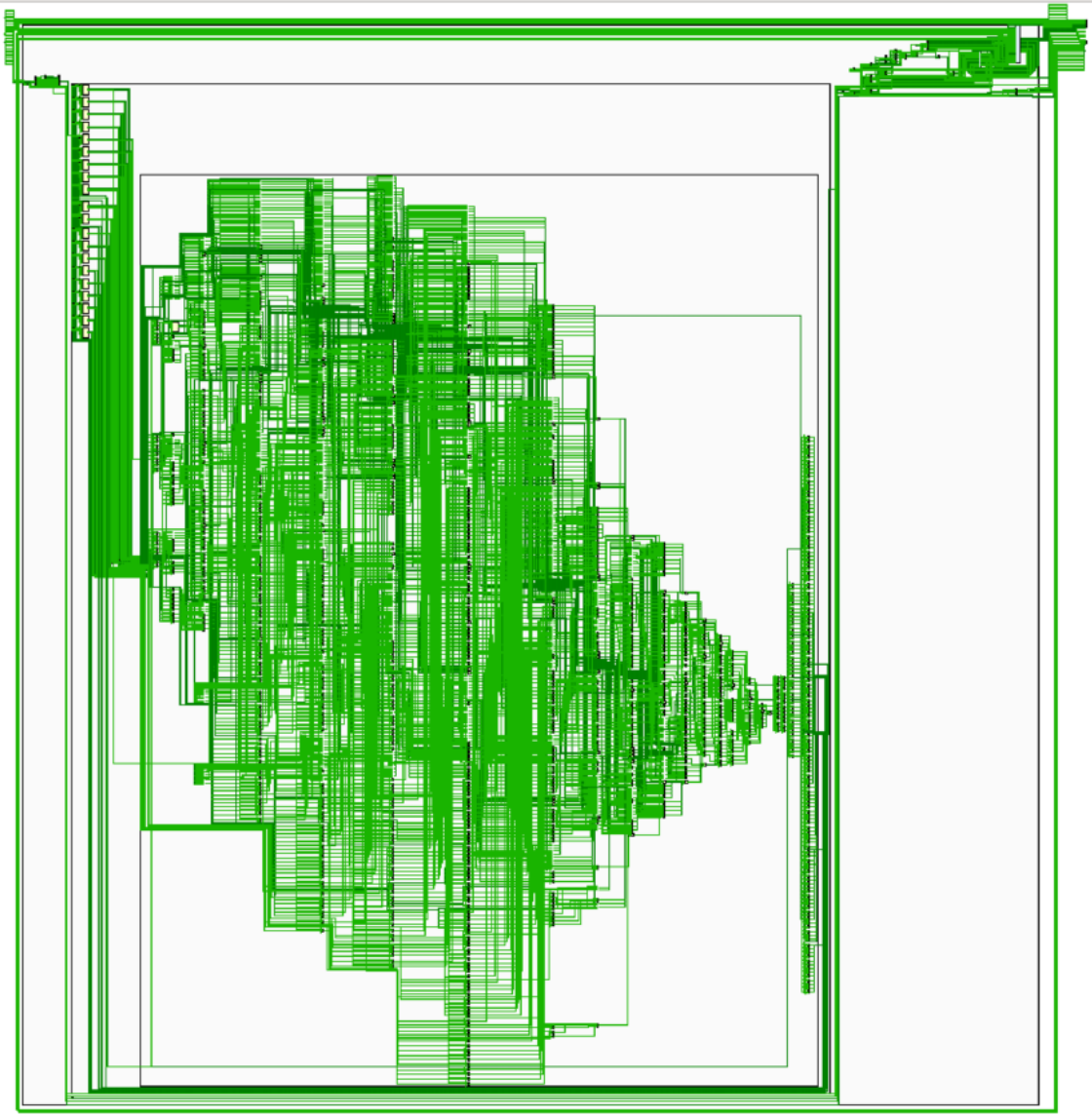
## P̄ANDA ROOT (computing session contribution from Luigi)

- Cluster reconstruction works

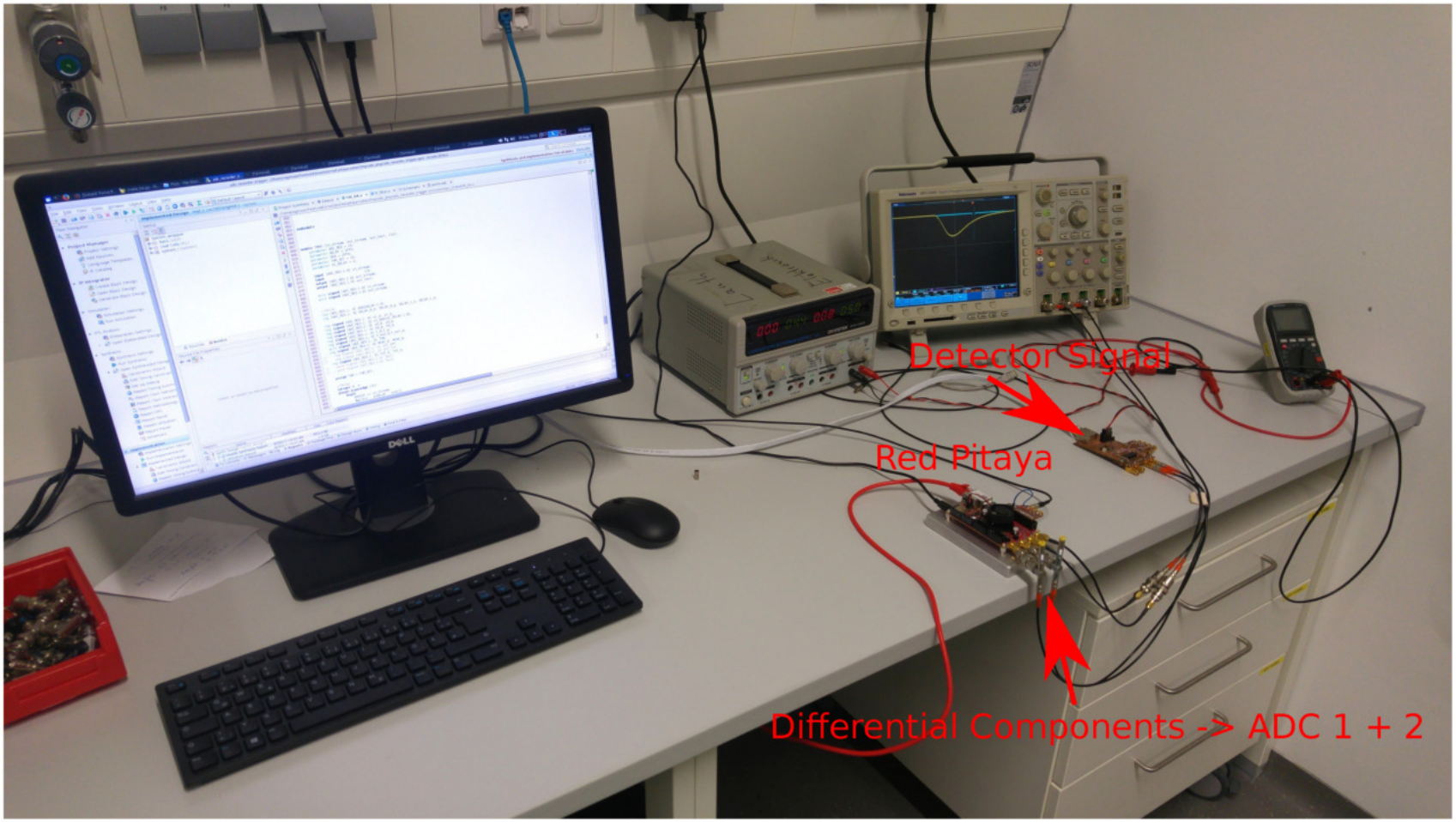


# APFEL ASIC Feature Extraction (FE)



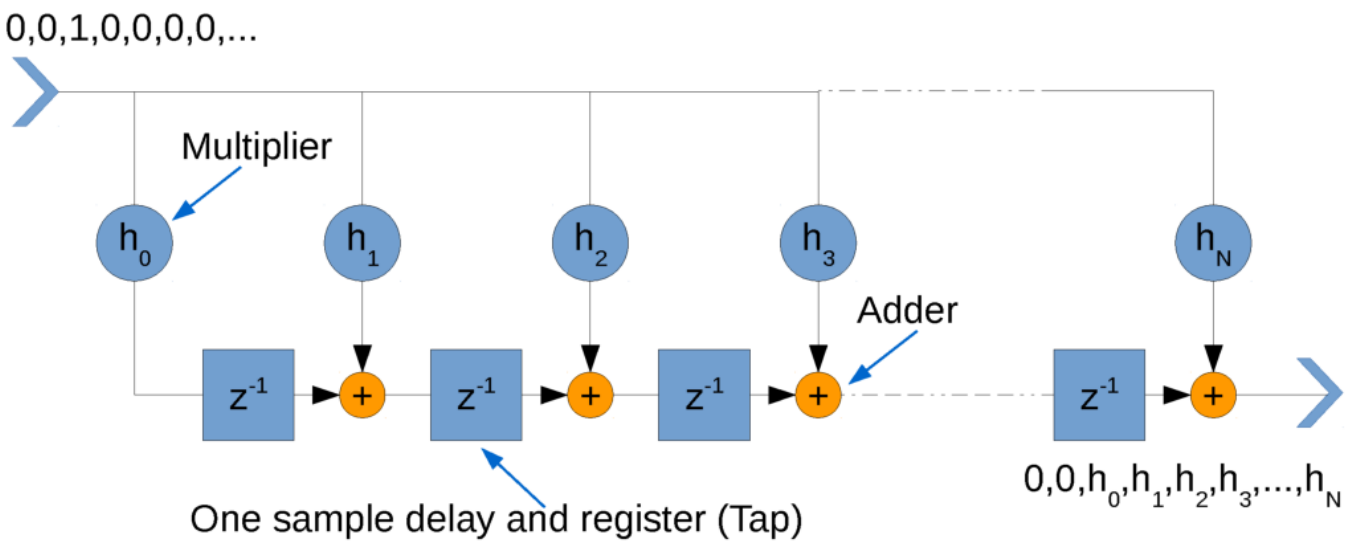
# FE - Setup (FPGA)



# FE - Smoothing via Finite Impulse Response (FIR) Filter

## Idea

- Transfer function which suppresses undesired signal frequencies
- $H(z) = \sum_{j=0}^{N} h(j) \cdot z^{-j}$ (Z-transformation of impulse response)
  - $h(j)$ : filter coefficients
  - $z = e^{i\omega}$ with $\omega = 2\pi f / f_s$ ($f_s$ : sampling rate)
- Each output value is weighted sum of most recent input values
- $\mathbf{out}[n] = h_0\mathbf{in}[n] + h_1\mathbf{in}[n-1] + ... + h_N\mathbf{in}[n-N]$



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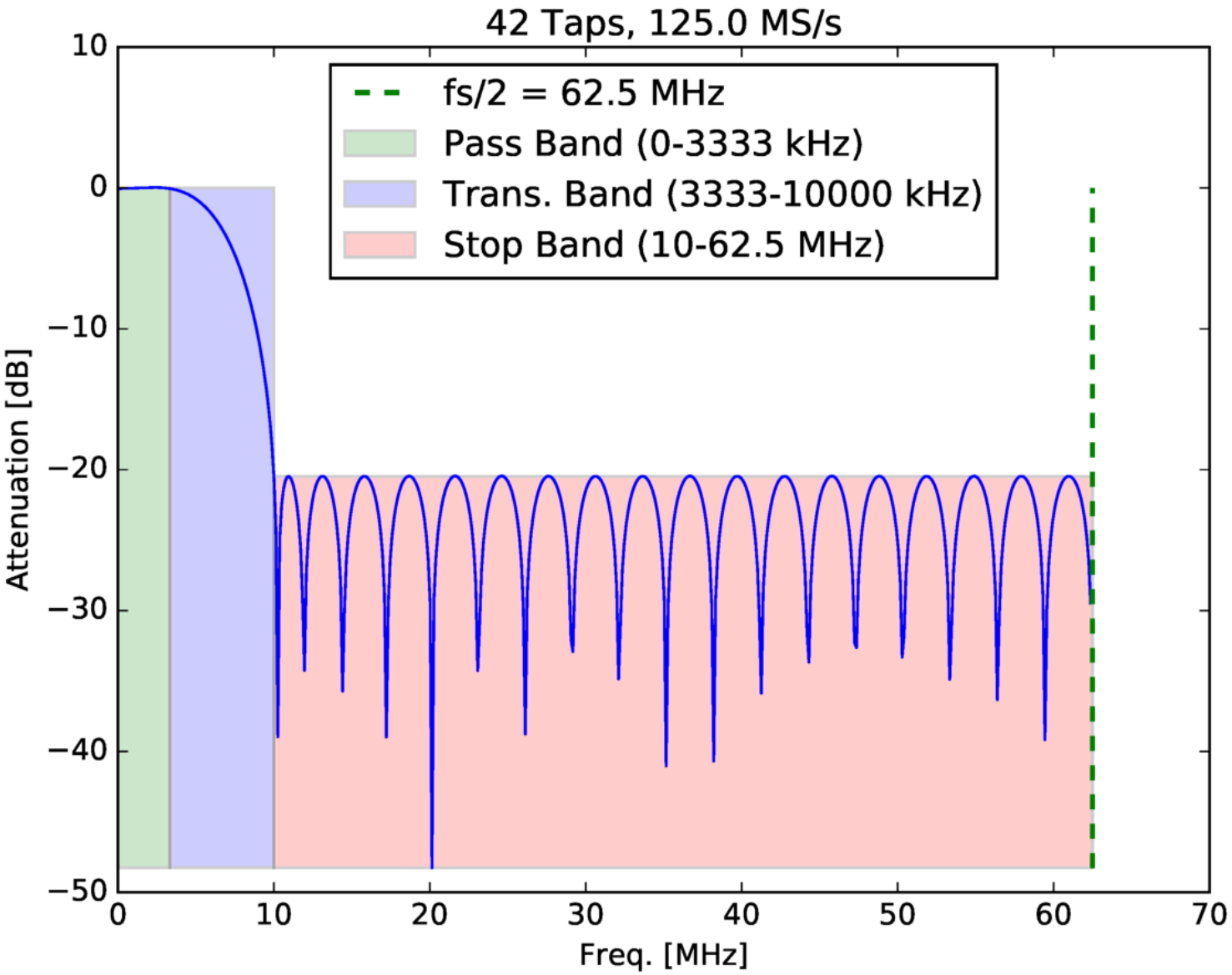

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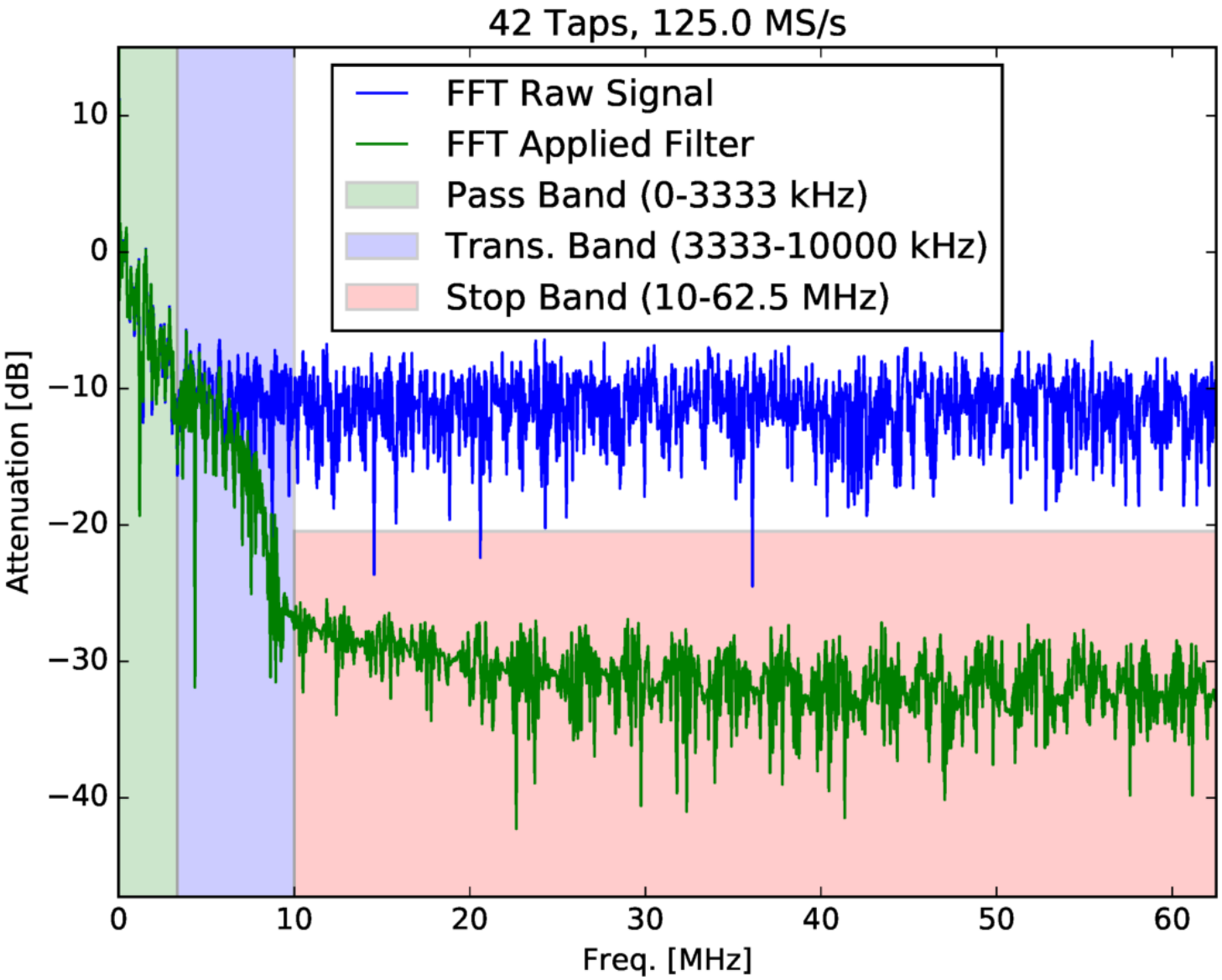

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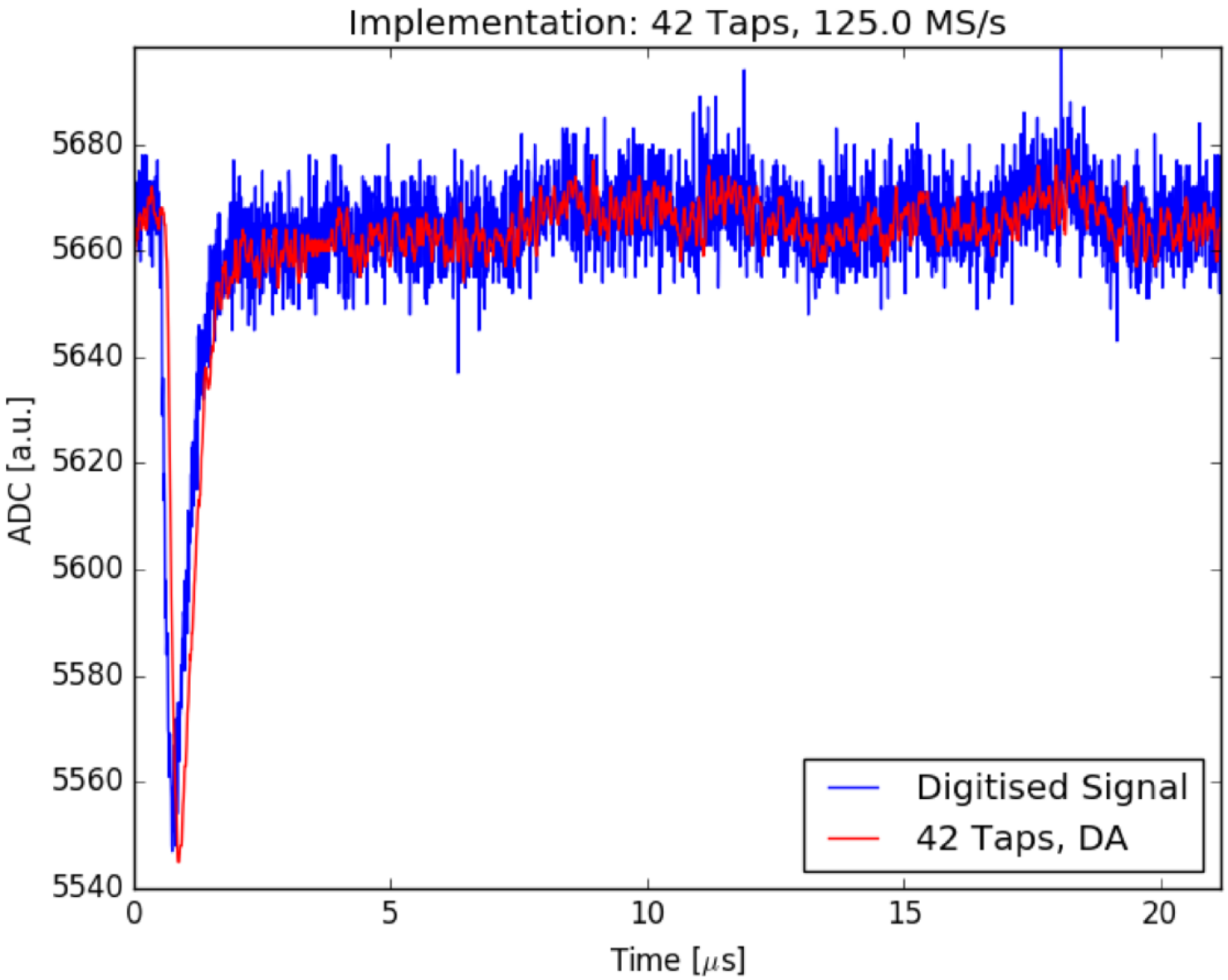


# FE - Smoothing via Finite Impulse Response (FIR) Filter

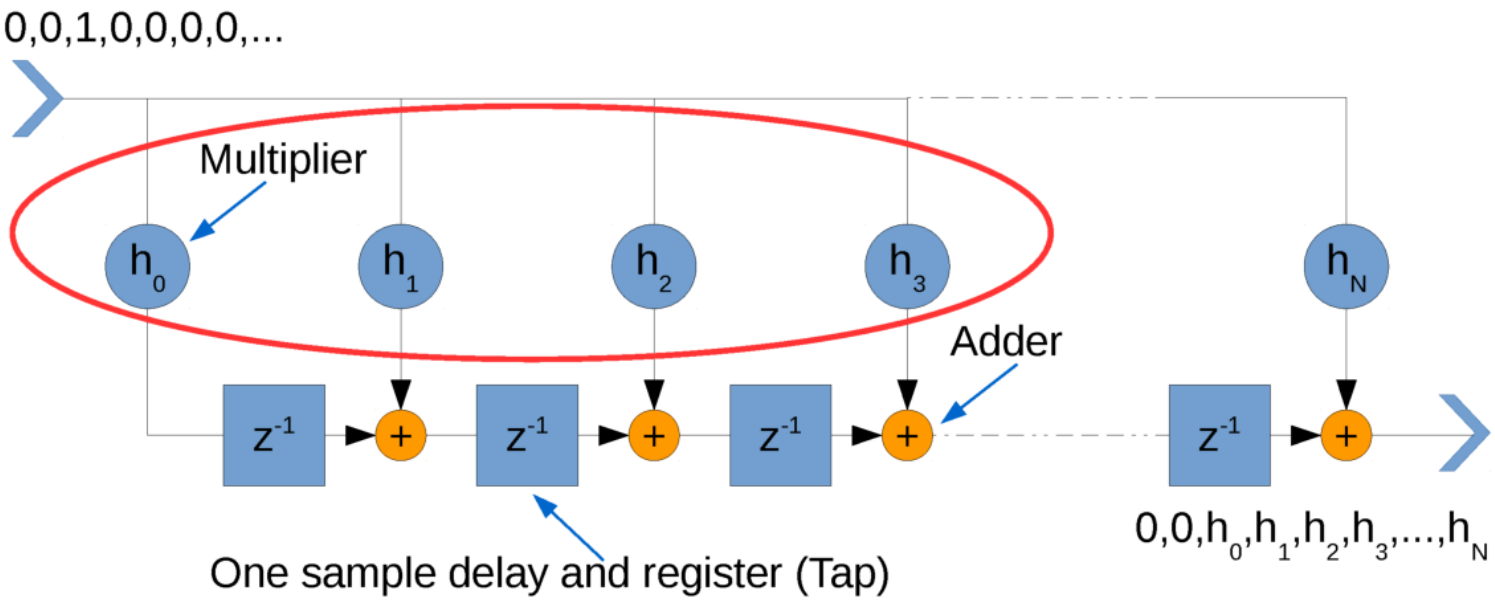
## Benefits

- Reliable smoothing procedure (stable, no self-excitation)
- No pulse washout (pulse slope)
- Perfect adaption on Signal (bandpass)

## Drawback

- FIR filtering eats FPGA recourses

# FE - Smoothing via Finite Impulse Response (FIR) Filter




## Implementation

- Efficient synthesis with Digital Signal Processing slices (DSP)
- ∼70 DSP slices per channel, 600 DSP slices on XC7K160T
- Need of resource saving implementation

# FE - FIR with Distributed Arithmetic (DA)

Idea (simplified):

$$y = \sum_{k=1}^{K} h_k \cdot x_k$$

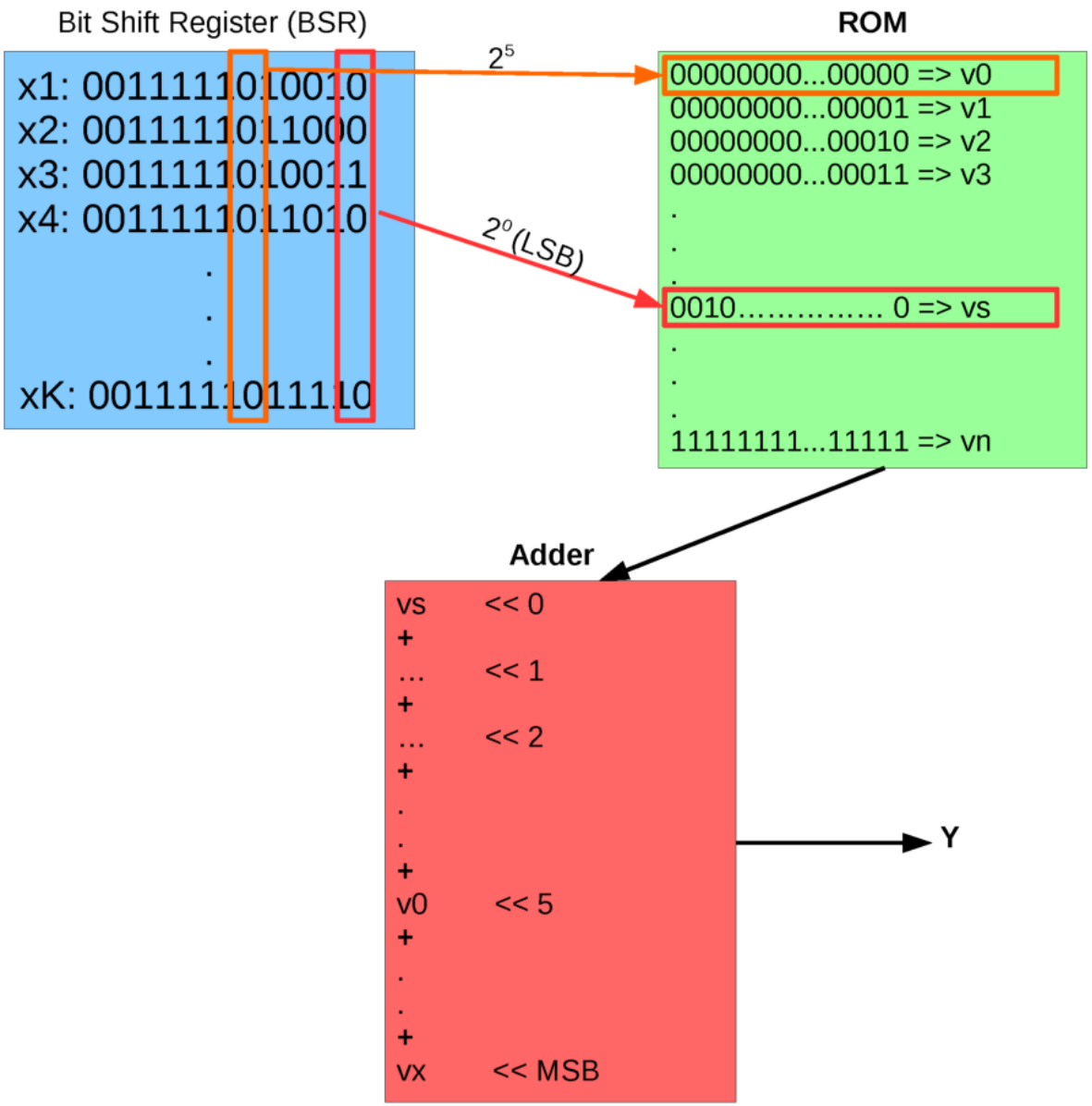
$$x_k = \sum_{n=0}^{N} b_{kn} 2^n$$

$$\dots$$

$$y = \sum_{n=0}^{N} \left[ \sum_{k=1}^{K} h_k \cdot b_{kn} \right] 2^n$$

Precalculated and stored in ROM

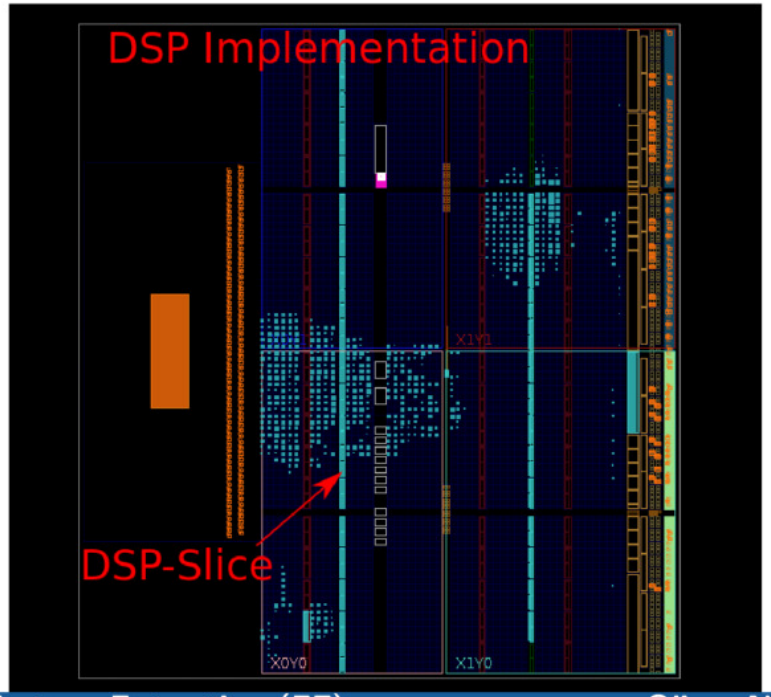
# FE - FIR with Distributed Arithmetic (DA)

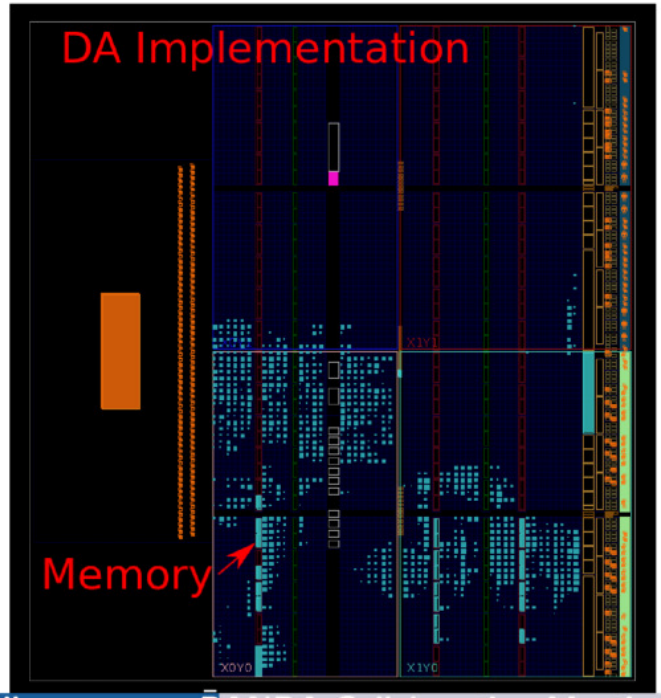


# FE - FIR with Distributed Arithmetic (DA)

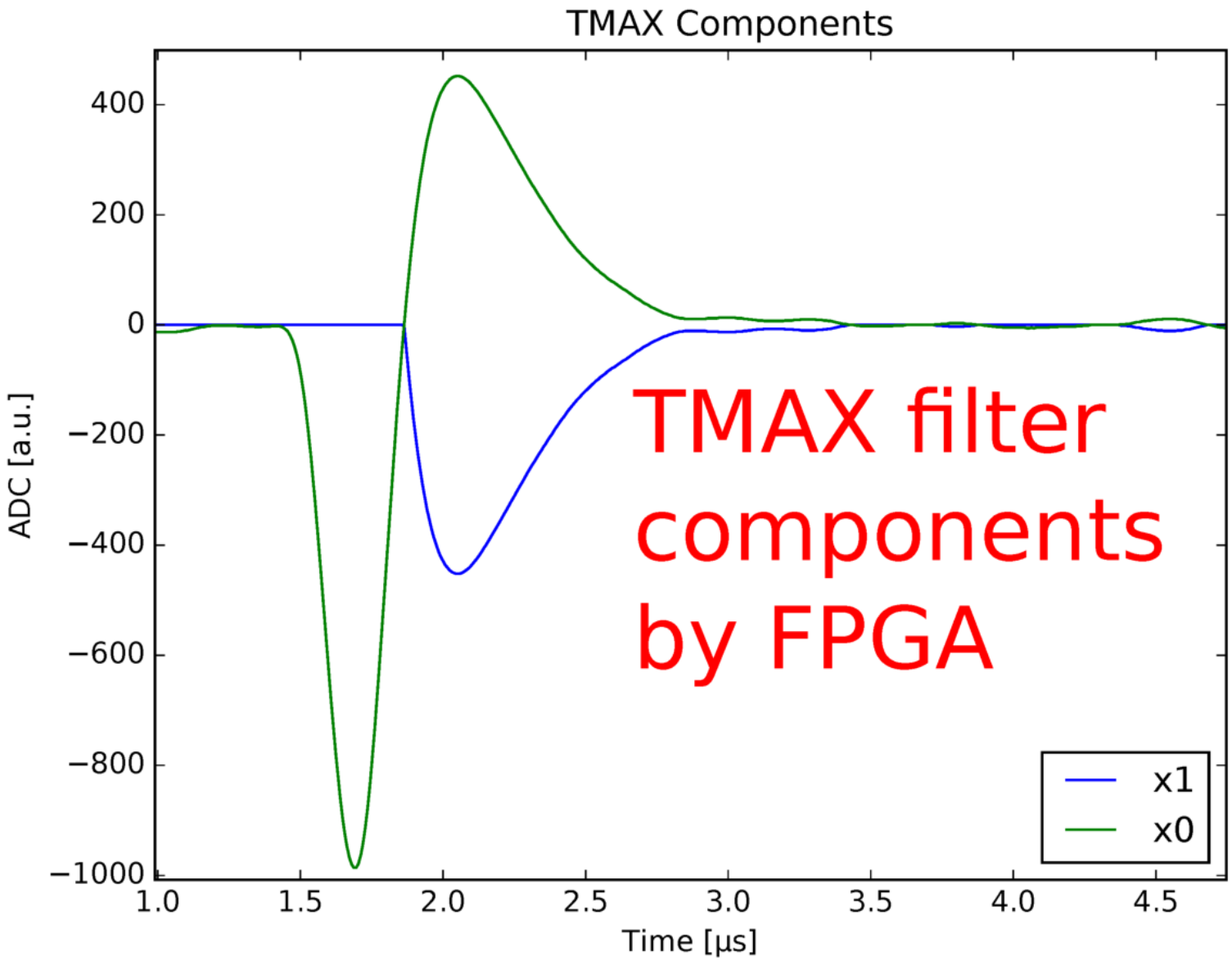
## DA Implementation

- No DSP slices needed
- No multiplications
- Hardware description way more complicated
- Hardware description generator script



# Time Measurement and Amplitude Extraction (TMAX)



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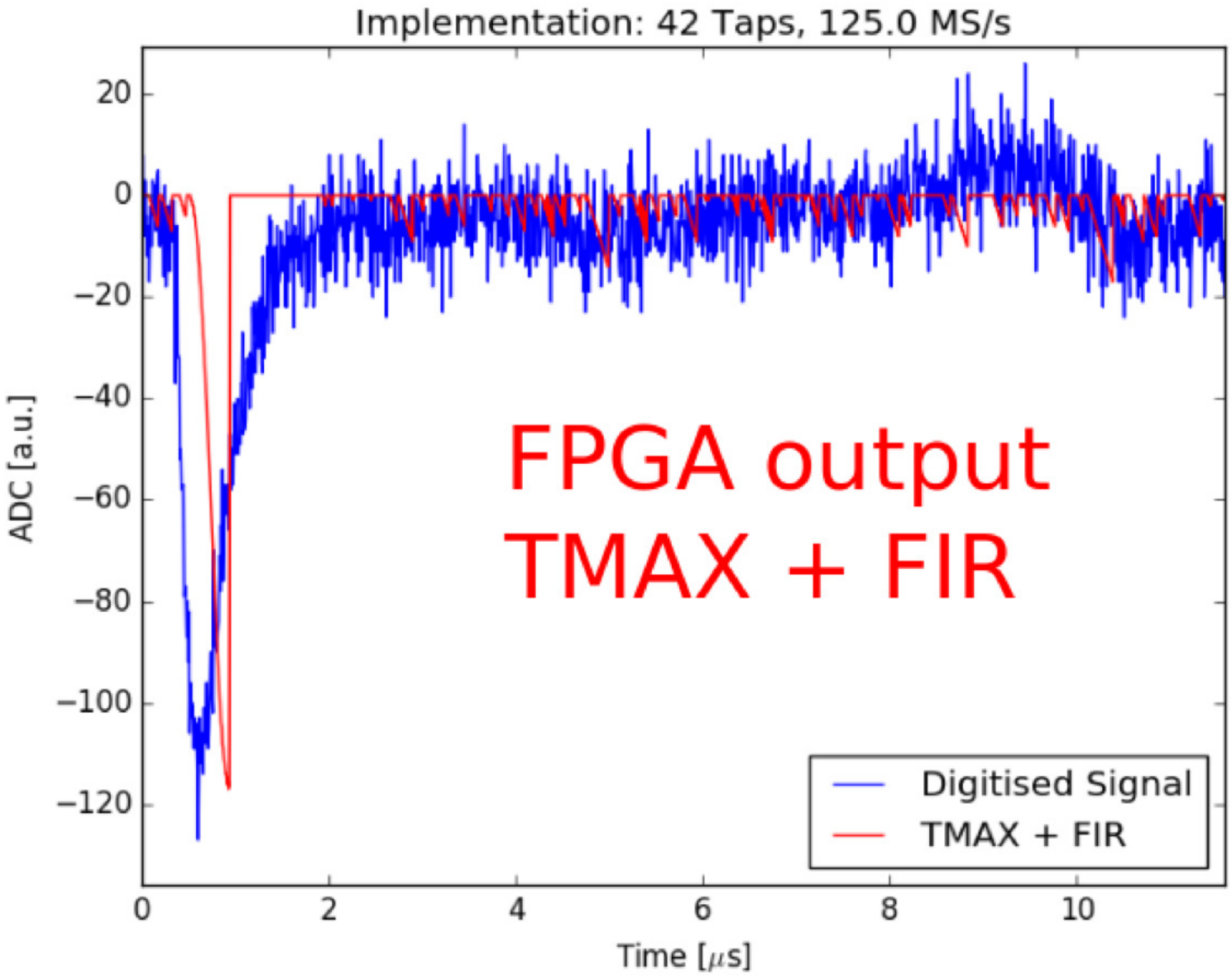

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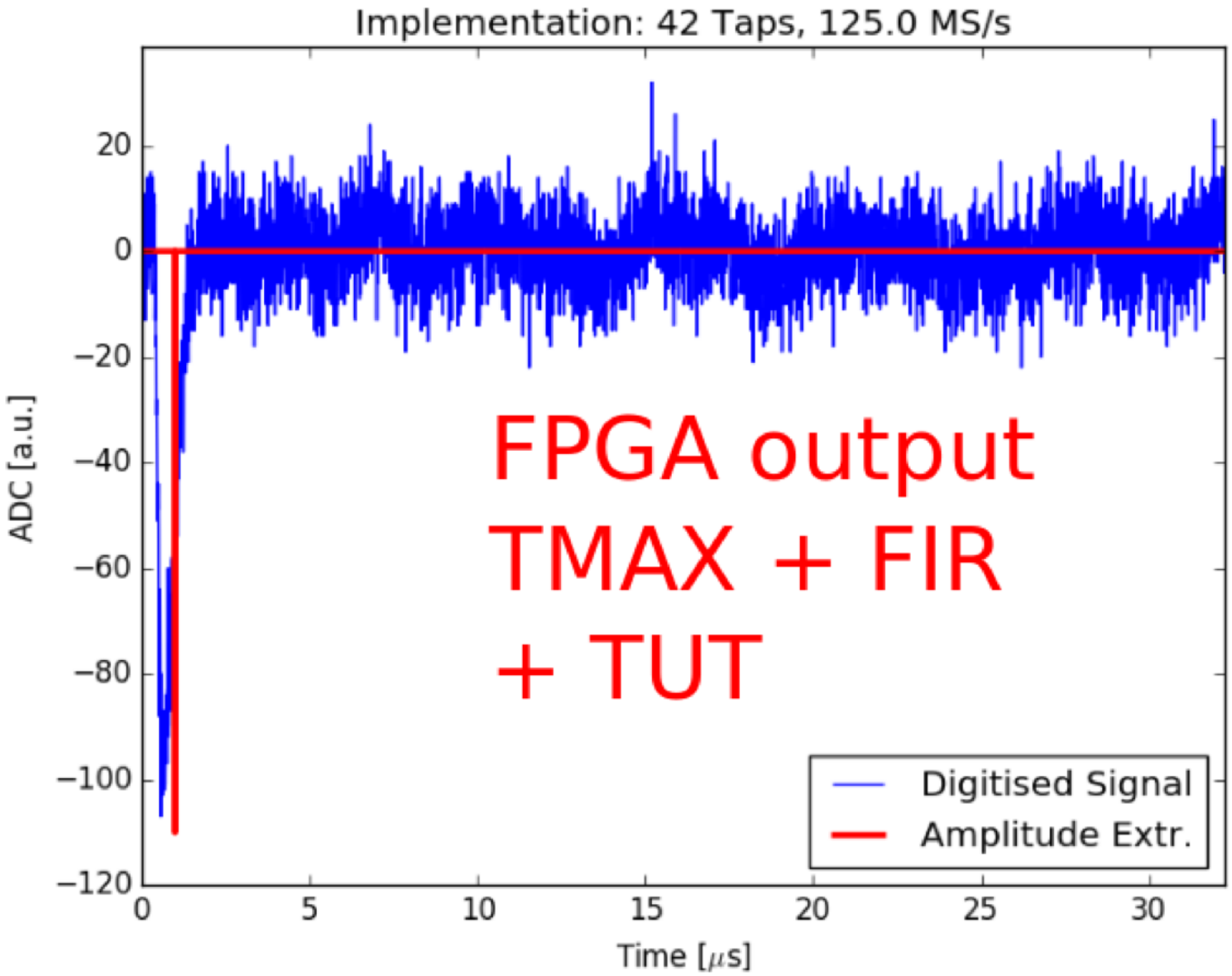


# FPGA Utilisation for FIR+TMAX

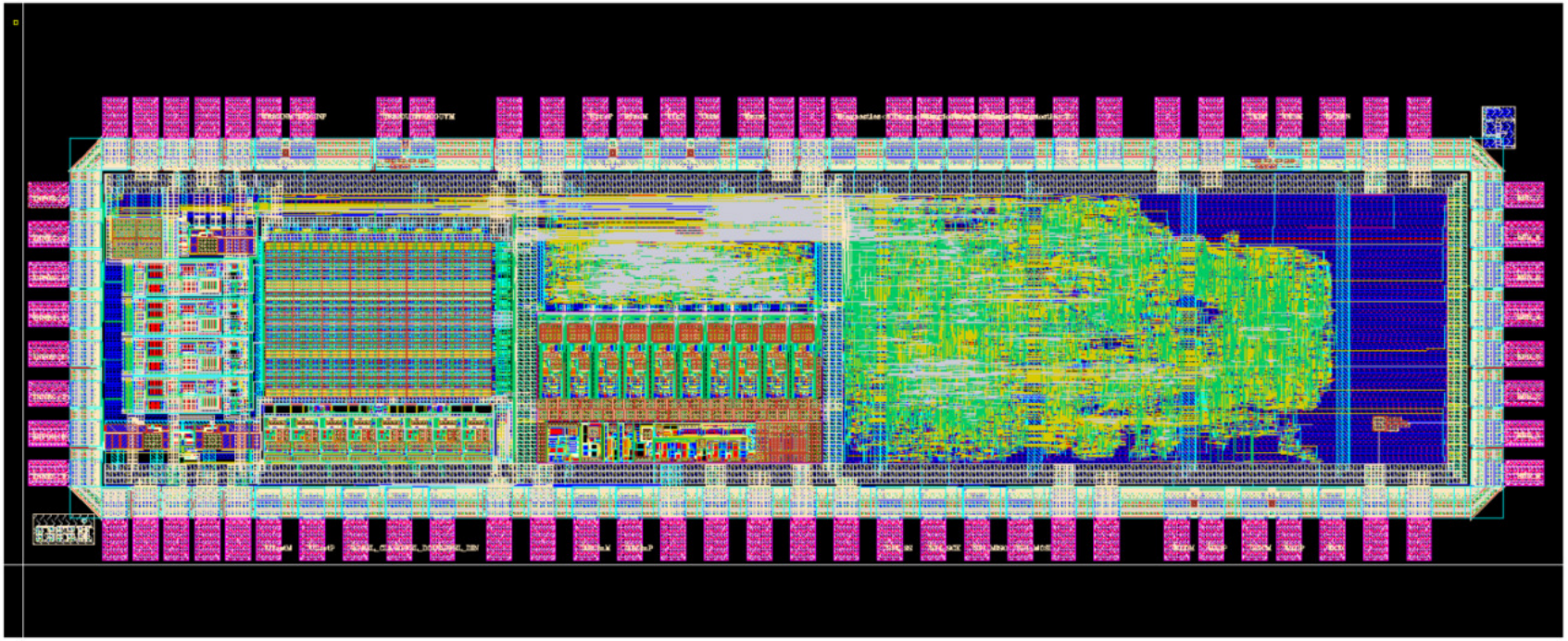
## Utilisation

- DSP on XC7K160T $\Rightarrow$ $\sim$9 channels
- Distributed Arithmetic on XC7K160T $\Rightarrow$ $\sim$30 channels

## Improvements

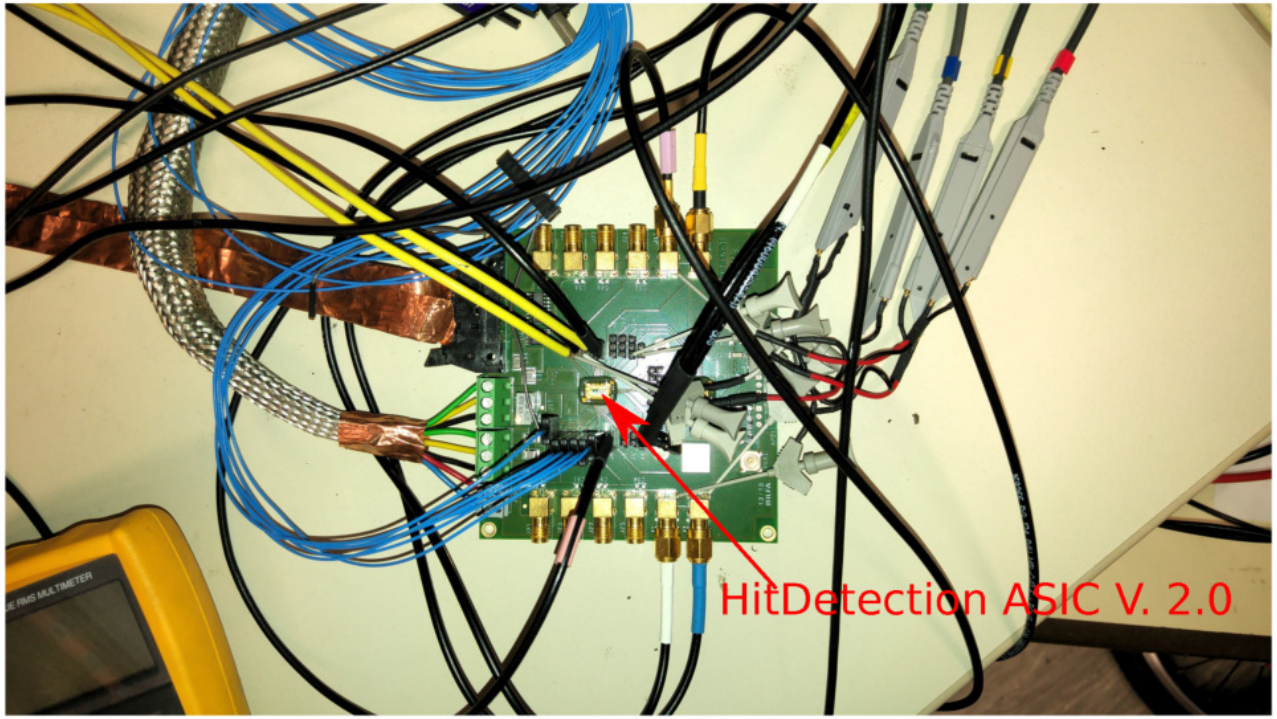
- Using inverse symmetries of FIR coefficients to reduce ROM
- Reducing number of FIR coefficients
- $>$32 channel on XC7K160T

# HitDetection ASIC Benchmark Tests



- H. Deppe, H. Flemming, P. Grasemann, O. Noll, P. Wieczorek

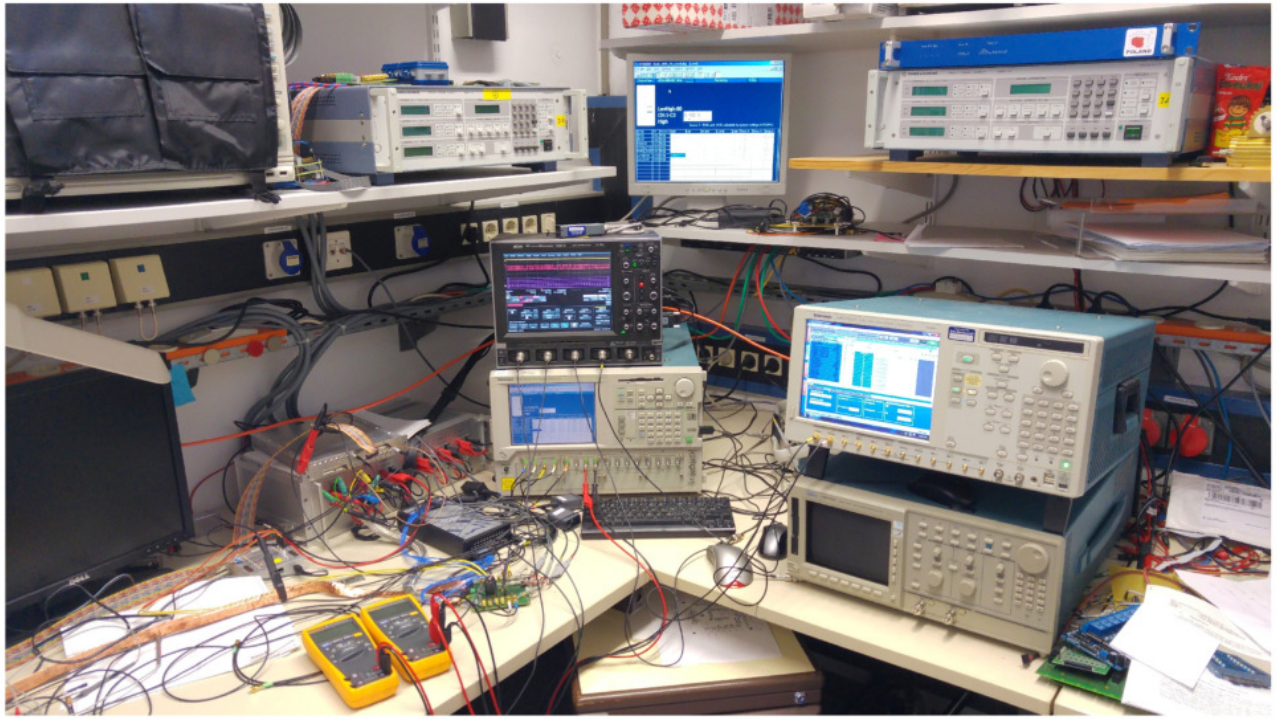
# HitDetection ASIC




## HitDetection ASIC

- 12 bit pipeline ADC
- Analog buffer for fast sampling rates
- Integrated hit detection
- Goes well together with APFEL ASIC

# HitDetection ASIC



## Measuring Program

- Linearity
- Signal noise ratio (effective number of bits)
- Threshold scans (hit detection)
- Tests with APFEL ASIC pulses (also with Mainz prototype)

# HitDetection ASIC

## Results

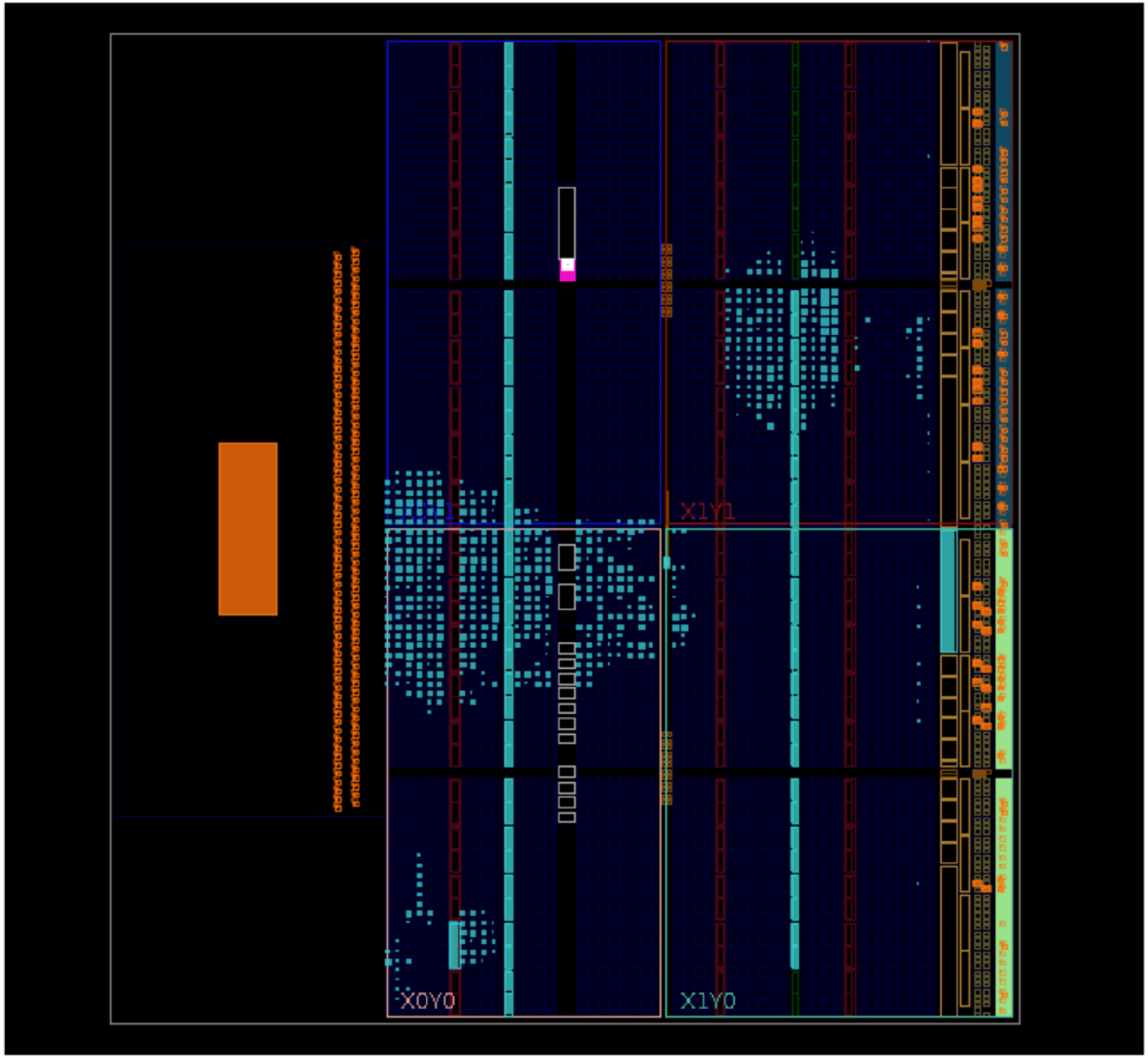
- Data taking and analysis are ongoing
- First promising results
- Will be shown at next $\bar{\text{P}}$ANDA meeting at the latest

# Summary and Outlook

- BWEC
  - Final design will be tested with PROTO16-2
  - PROTO16-2 is in production
  - Cooling tests with PROTO16-1
  - Implementation of BWEC in $\bar{\text{P}}$ANDA ROOT
- Feature Extraction
  - Resources saving implementation of filter
  - Time extraction needs to be updated
  - First tests with Uppsala ADC are currently being prepared
- HitDetection ASIC
  - First tests are done
  - Results will soon be shown

# Backup

# FE - Smoothing via Finite Impulse Response (FIR) Filter



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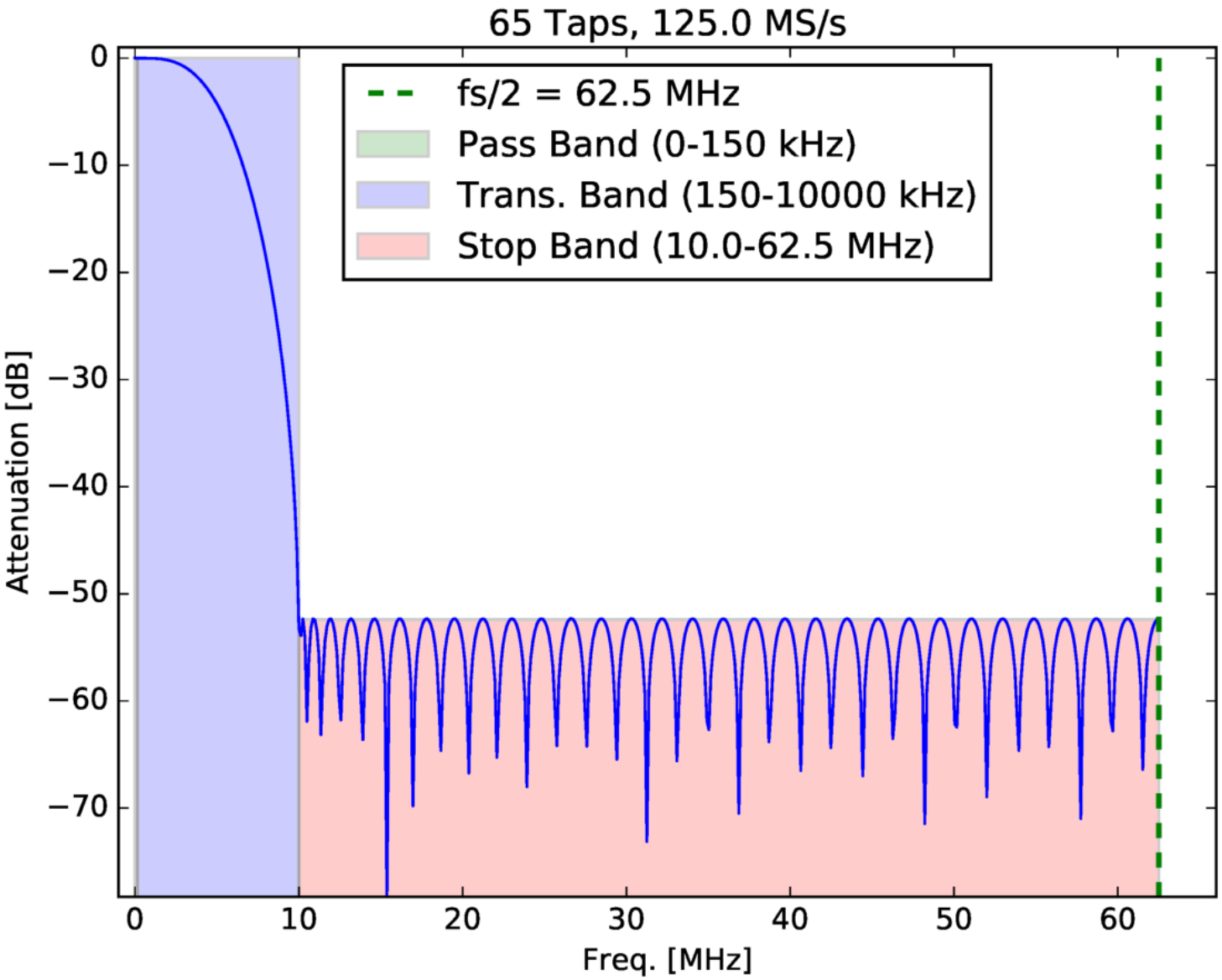

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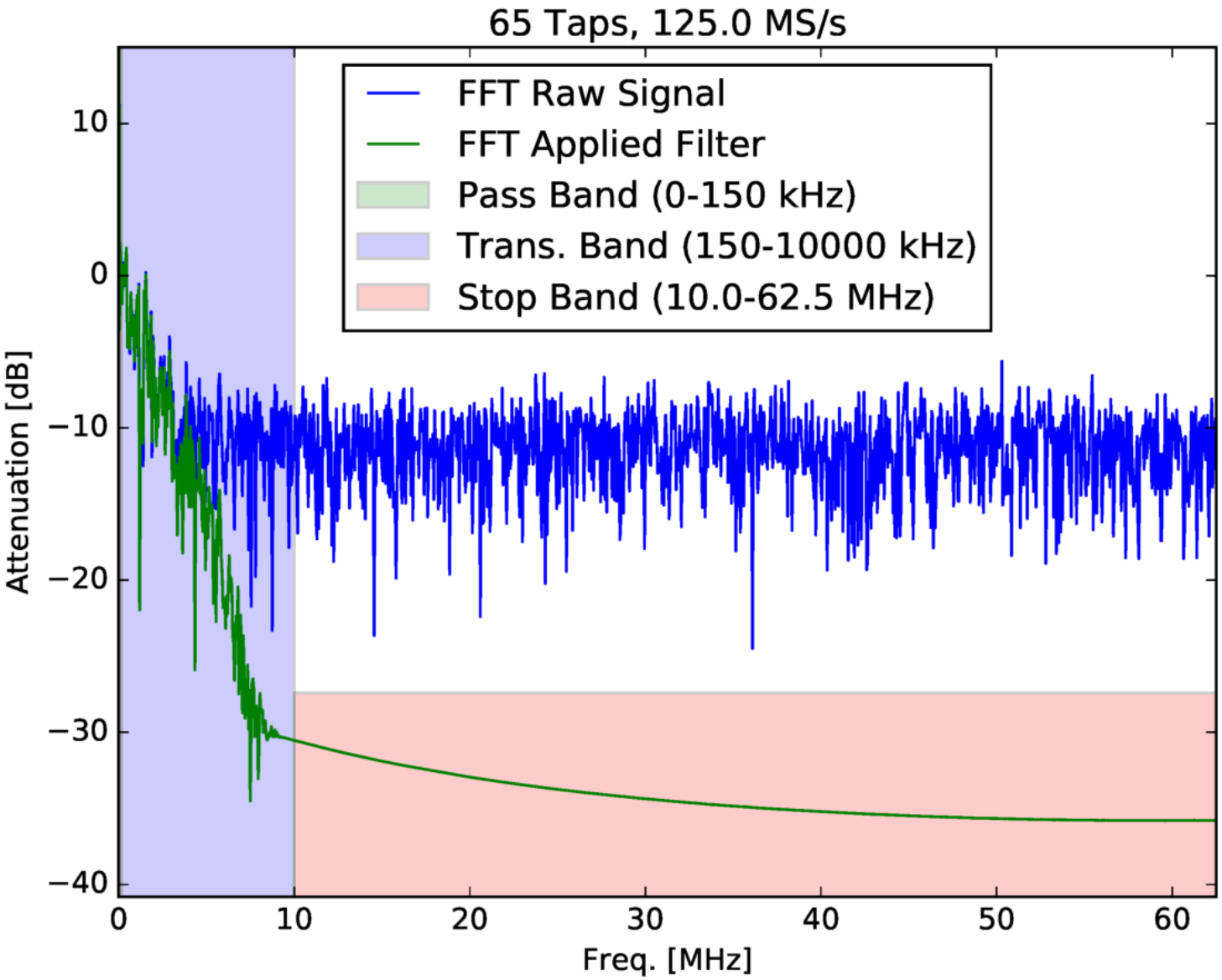

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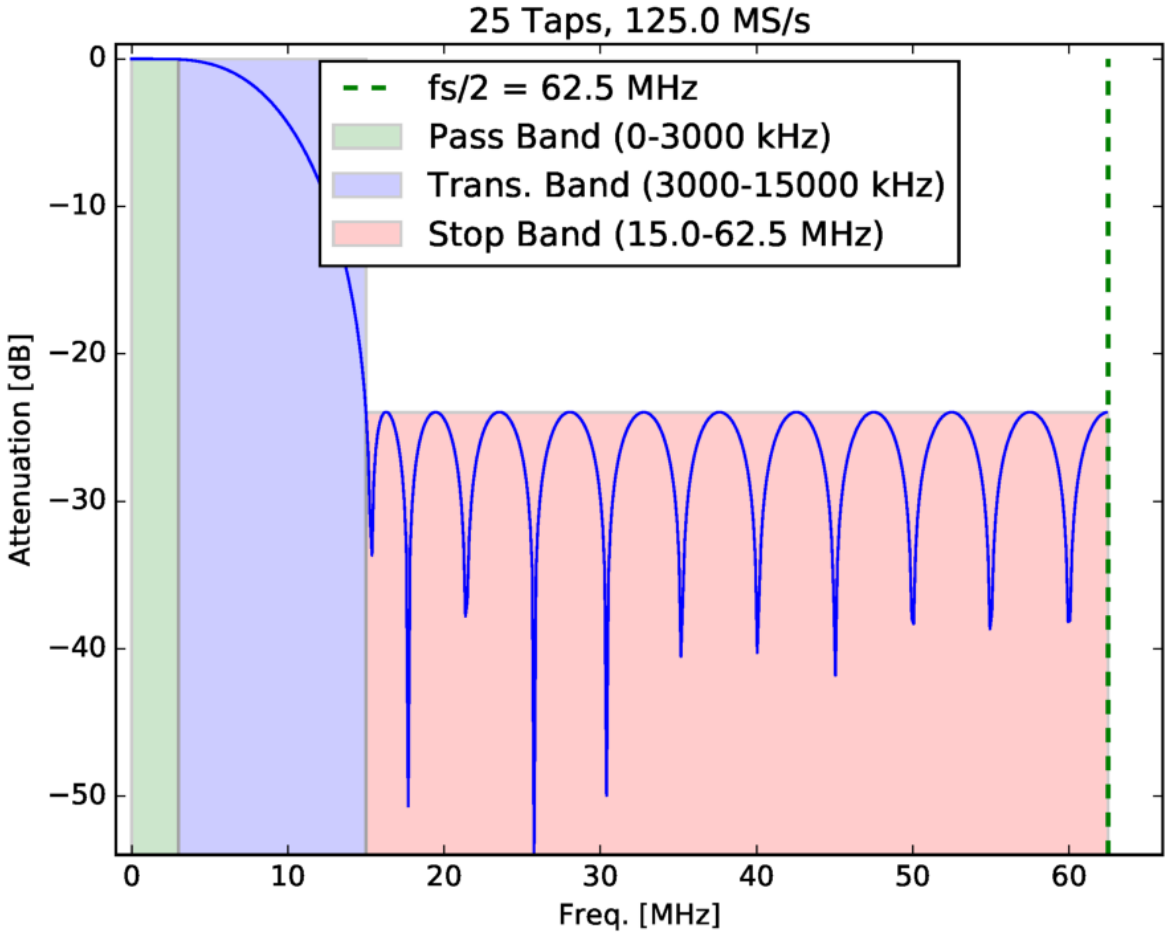

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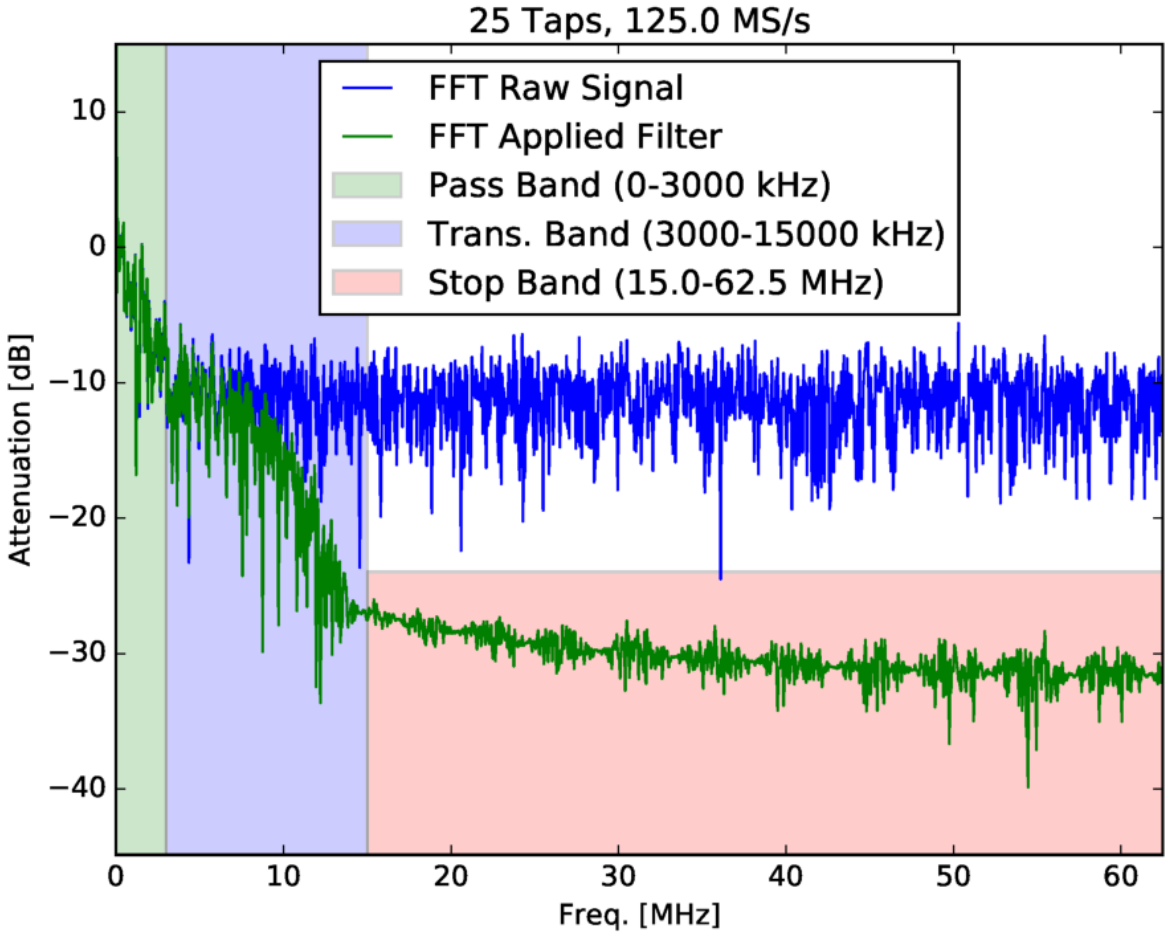

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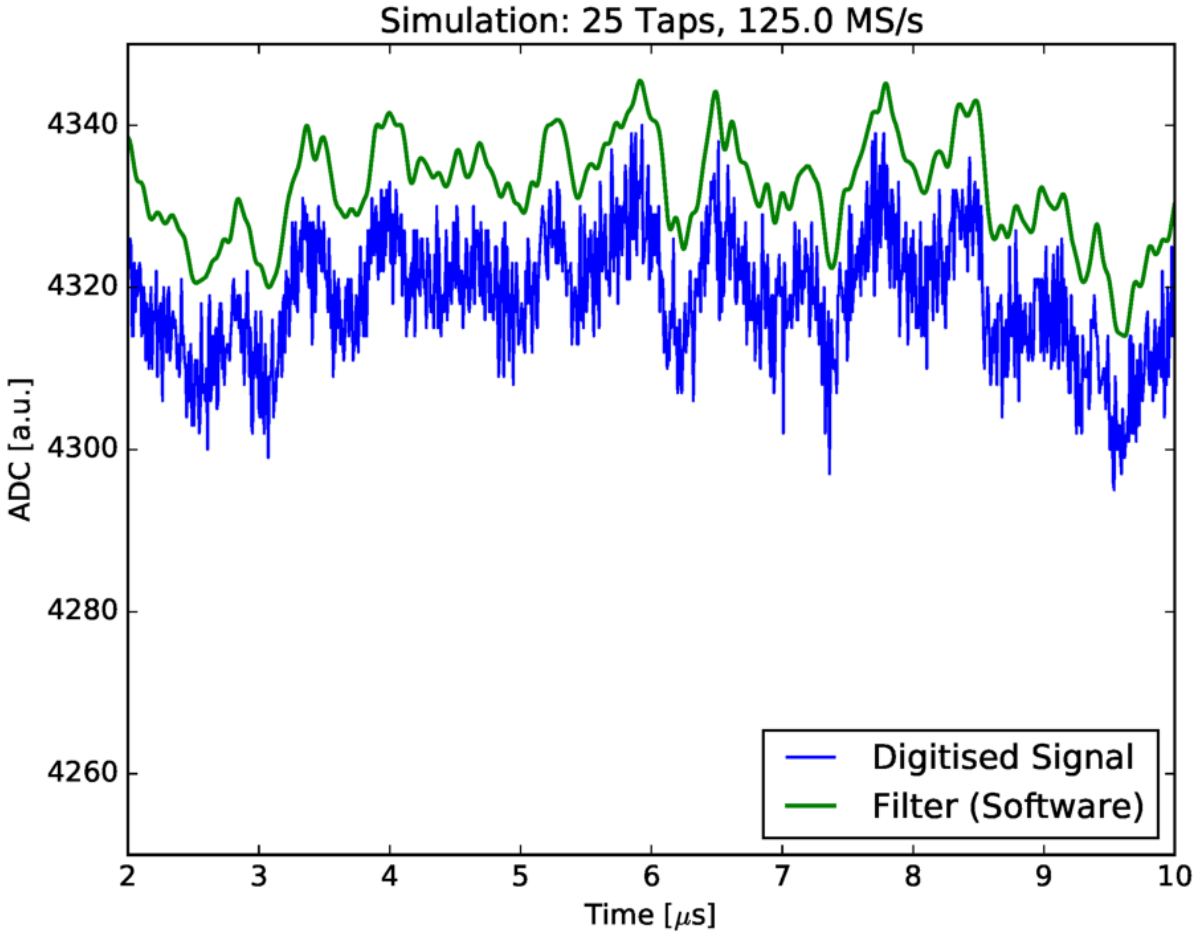

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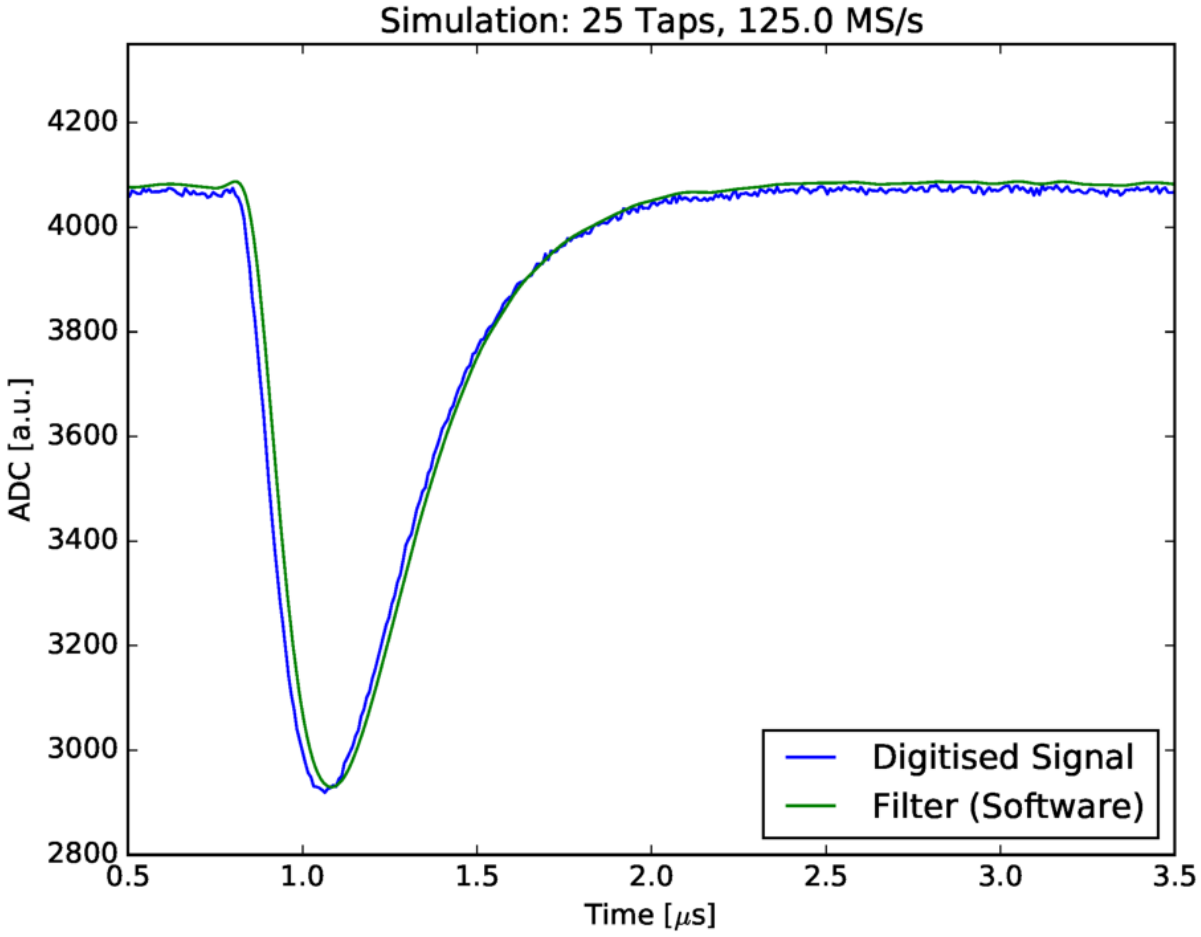
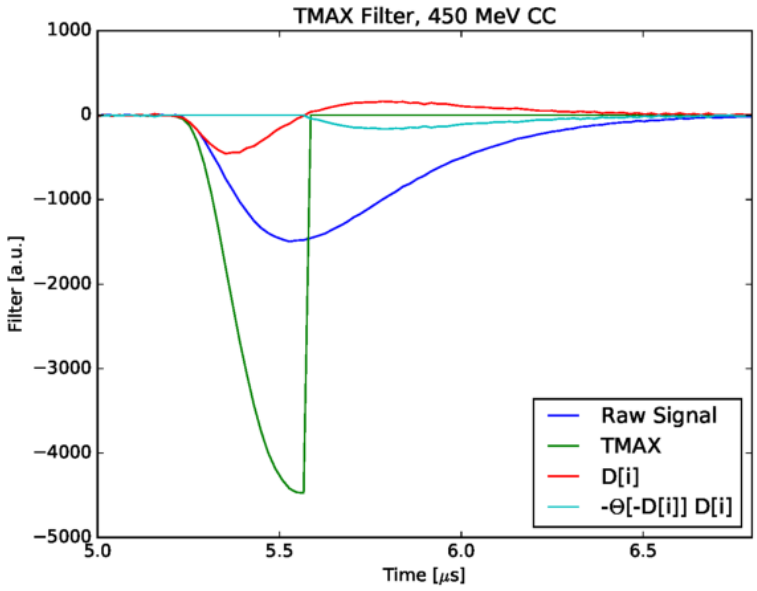
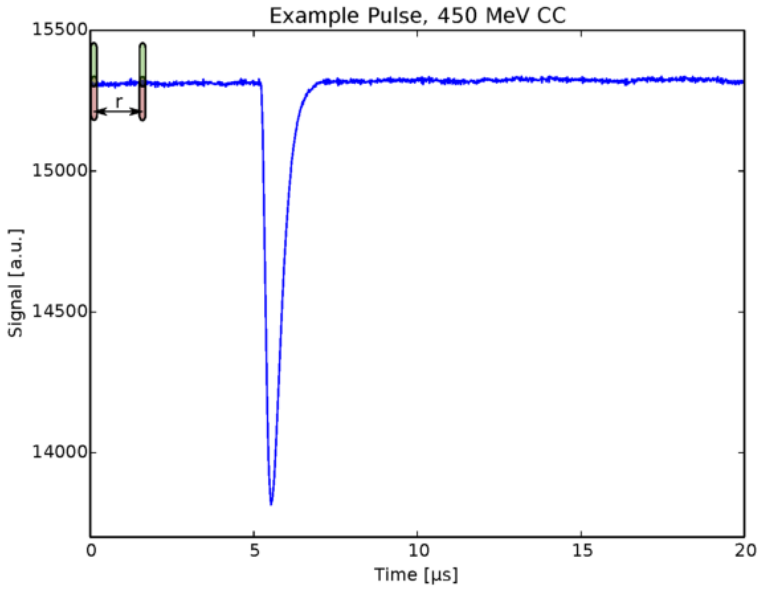


# TMAX Filter




**Derivative:**

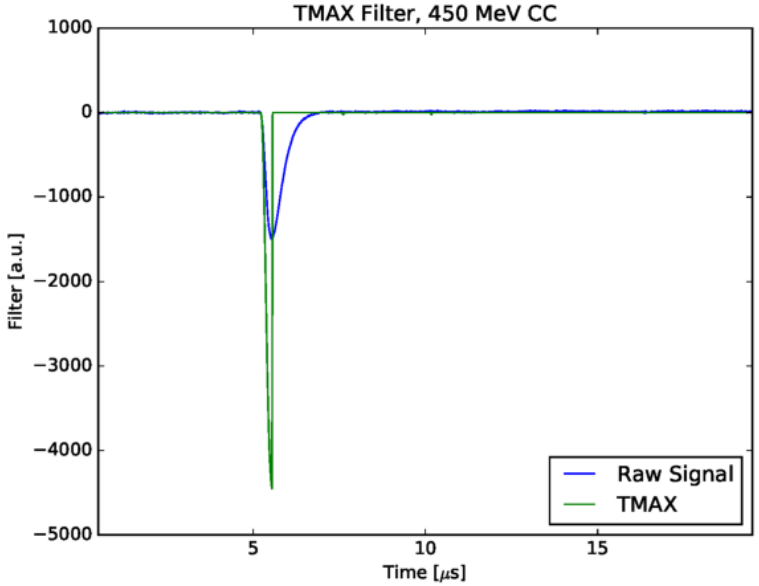
$$D[i] = T[i + r] - T[i]$$

**Heaviside function Θ:**

$$x \mapsto \begin{cases} 0: & x < 0 \\ 1: & x \geq 0 \end{cases}$$

**TMAX:**

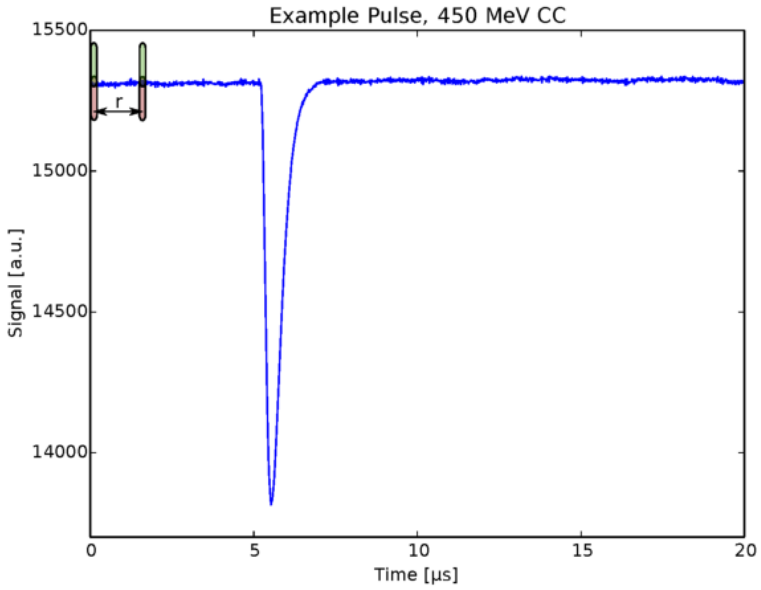
$$F_{TMAX} = \sum_{i=0}^{N} D[i] - \Theta[-D[i]] \cdot D[i]$$



# TMAX Filter

## TMAX Filter

- Sensitive on rising edge
- Cancels out falling edge
- No overshoot
- Short dead time

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