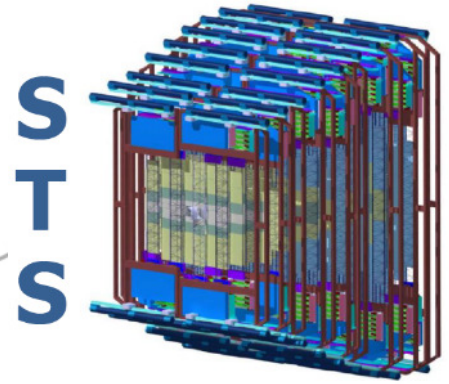
Microstrip and Gas Electron Multiplier Readout ASIC for Physics Experiment at FAIR

AKADEMIA GÓRNICZO-HUTNICZA IM. STANISŁAWA STASZICA W KRAKOWIE
AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

kasinski@agh.edu.pl

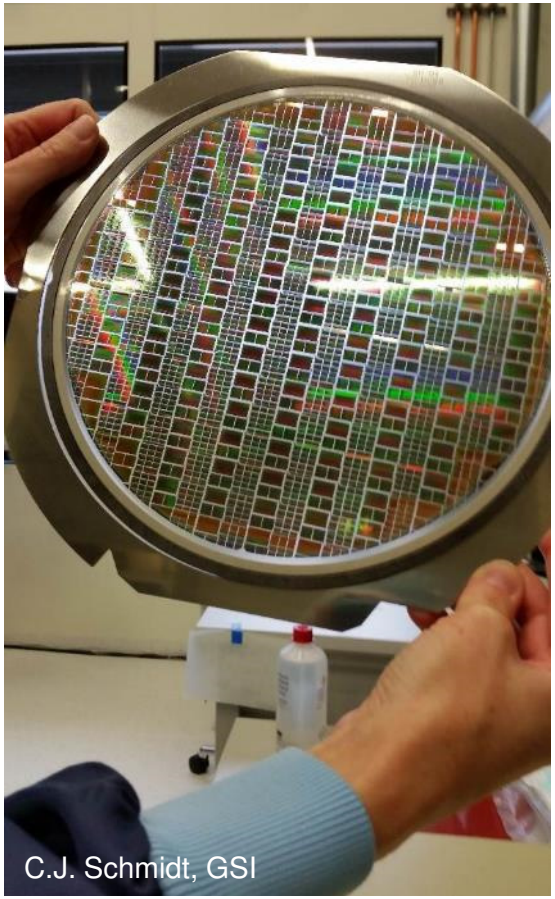
Krzysztof KASINSKI,
Weronika ZUBRZYCKA,
Robert SZCZYGIEŁ

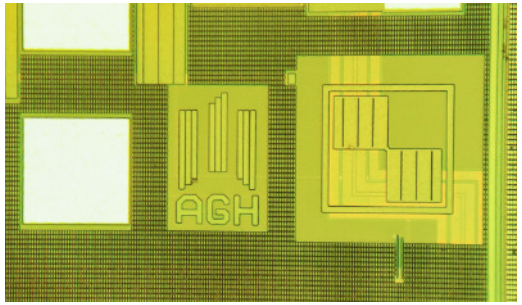


2017 IWORID, Kraków, Poland

Outline

- Introduction – CBM Experiment, STS & MUCH detectors
- STS/MUCH-XYTER2 ASIC
  - Front-End, Data flow, Protocol & Interface
  - Test system
- Measurement results
- Summary



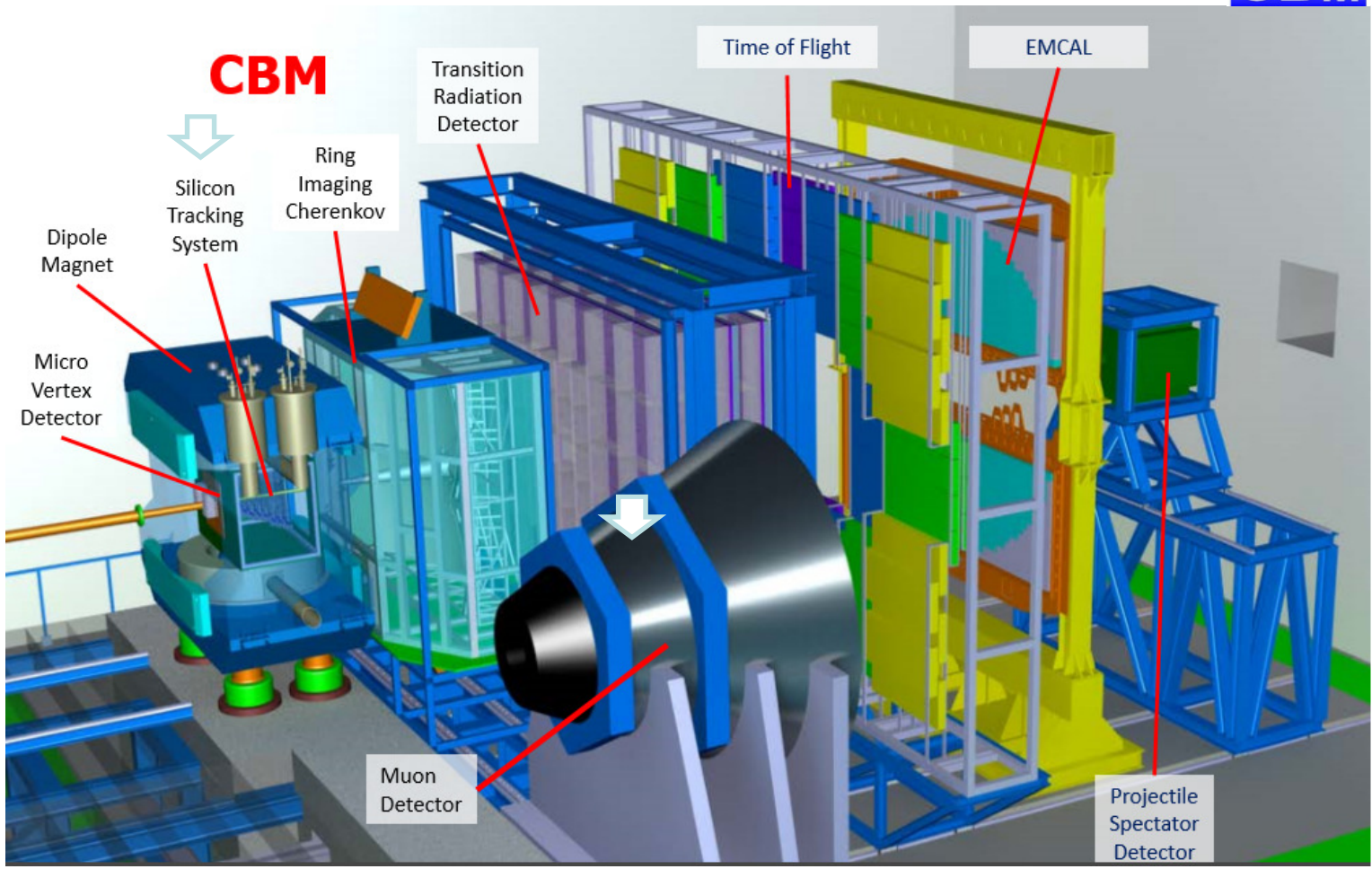


Compressed Baryonic Matter Experiment

Goal: exploration of the QCD phase diagram in the region of very high baryon densities

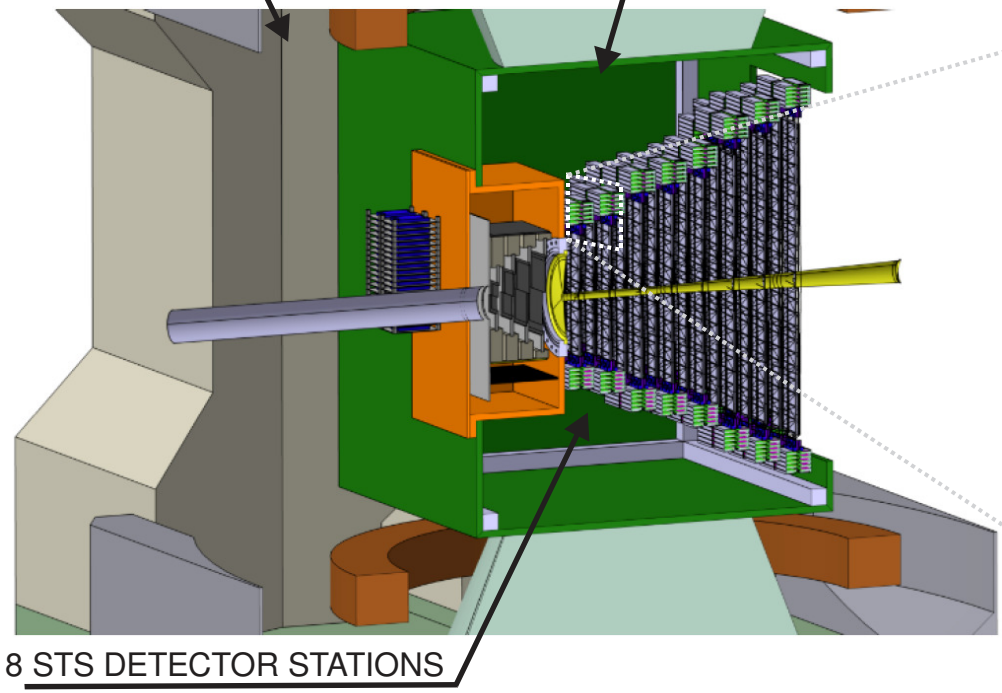
- up to 10 MHz interactions
- **self-triggering** front-end chip
- radiation doses

STS: track reconstruction and momentum determination of charged particles in 1T field, 8 detector stations (30cm – 100 cm from target)

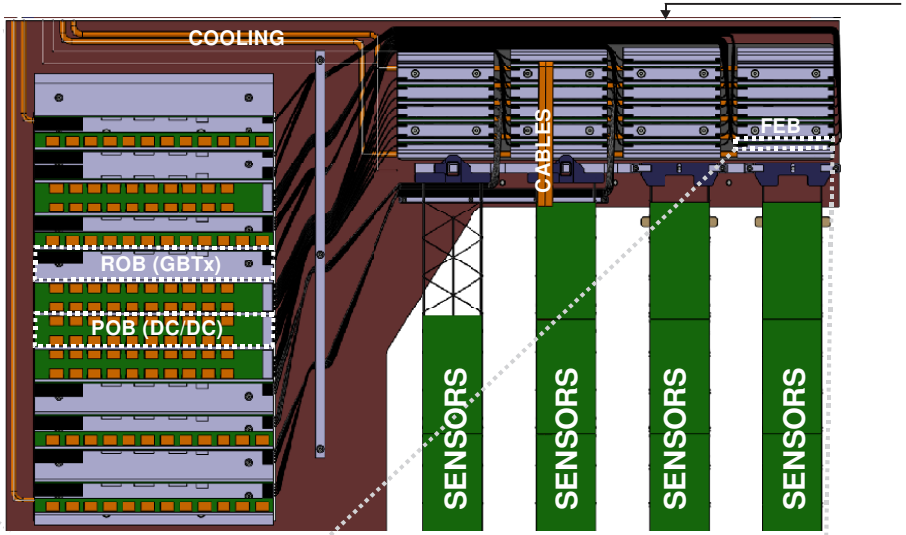


FAIR Facility for Antiproton and Ion Research

STS system - overview

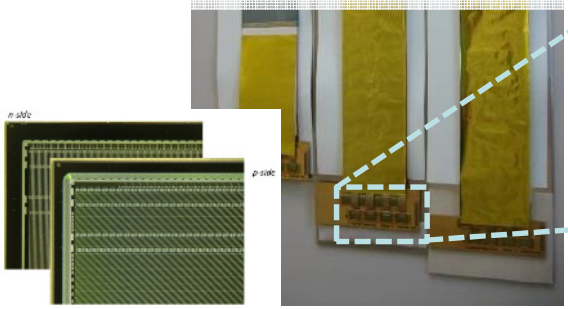


CORNER OF THE SINGLE STATION

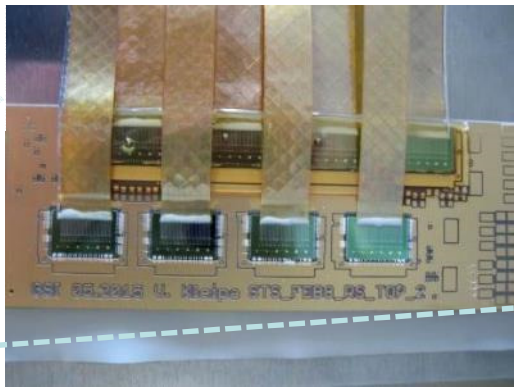


readout electronics located at the perimeter of the detector stations on FEB boards (8 chips/board).

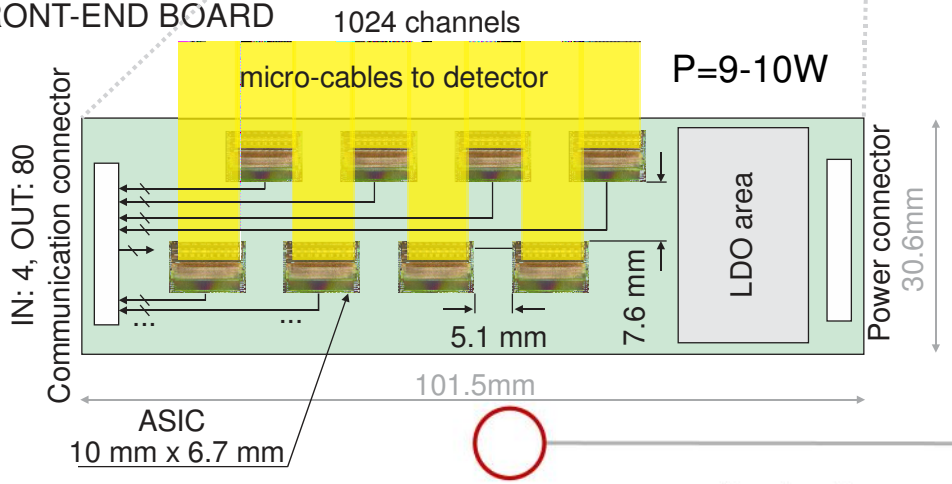
double–sided, micro-strip, 1024 channels per side, 7.5°stereo angle, **58 μm pitch**, lengths 20 - 120 mm, 300 μm thickness,



mock-up demonstrator

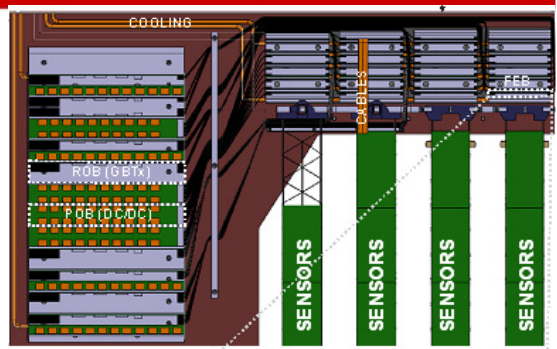


FRONT-END BOARD

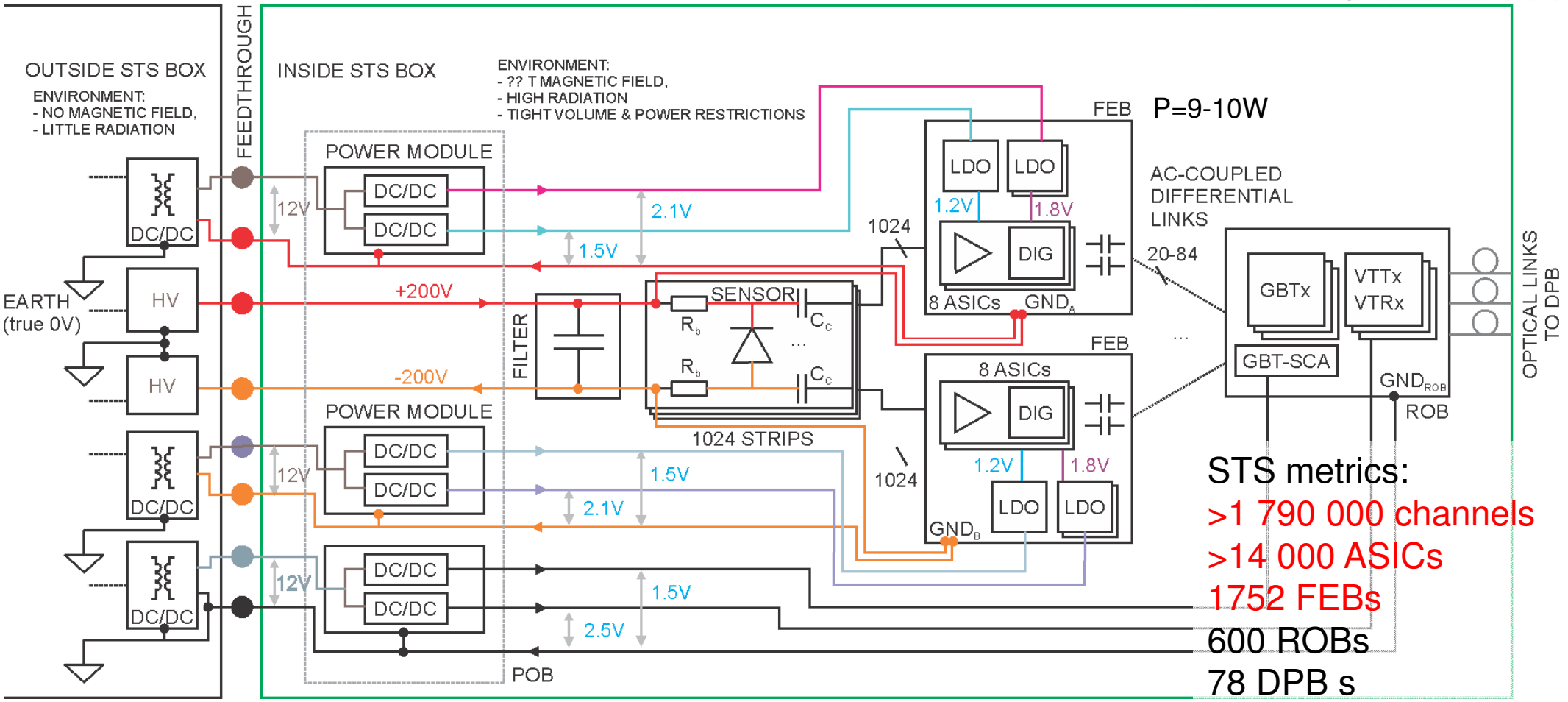


J. Heuser, et al., *GSI Report 2013-4 Technical Design Report for the CBM Silicon Tracking System (STS)*, GSI, Darmstadt, 2013.

STS Power & Readout



LOW-VOLTAGE and HIGH-VOLTAGE POWERING SCHEME (SINGLE SENSOR)

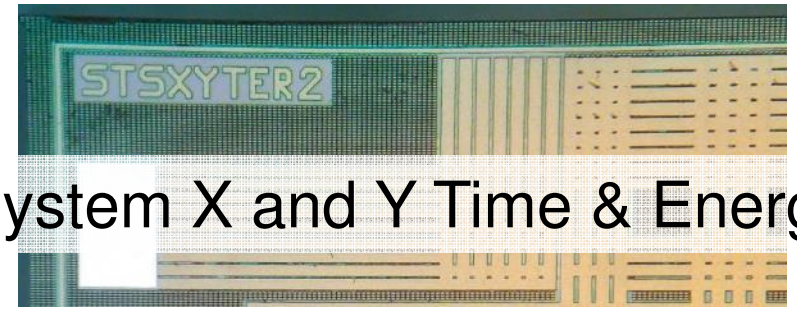


J. Lehnert ; W. F. J. Müller ; C. J. Schmidt;
The GBT-based readout concept for the silicon tracking system of the CBM experiment. Proc. SPIE 9662, 96622S.

K. Kasinski, P. Koczon, S. Ayet, S. Loechner, C. J. Schmidt;
System-level Considerations of the Front-End Readout ASIC in the CBM Experiment from the Power Supply Perspective. Journal of Instrumentation 2017.

STS-XYTER2

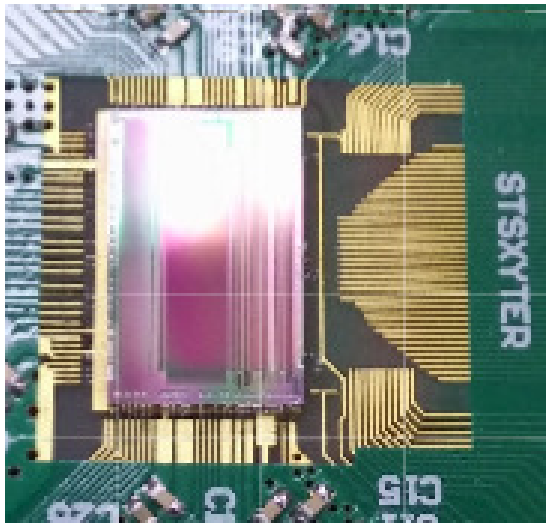
Silicon Tracking System X and Y Time & Energy Readout

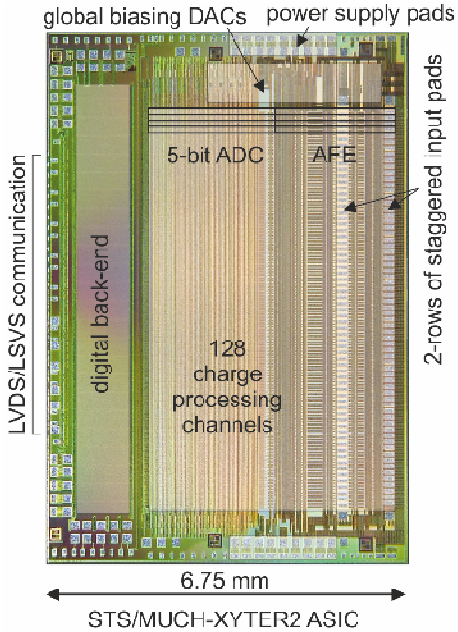


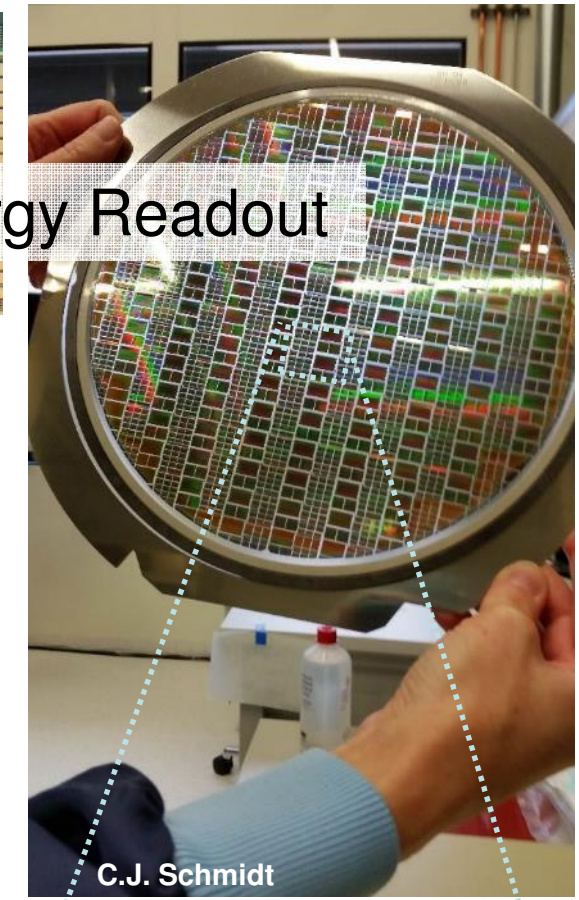
UMC 180 nm CMOS Engineering Run 2016 shared between other CBM chips
Thinning & stealth laser dicing
10 mm x 6.8 mm die size, 288 pads
128 channels + 2 diagnostic channels, Power: 1.1 – 1.3 W/chip
4420 bits of AFE configuration
54400 gates (after triplication), 12600 flops

Evolution of the STS-XYTER prototype

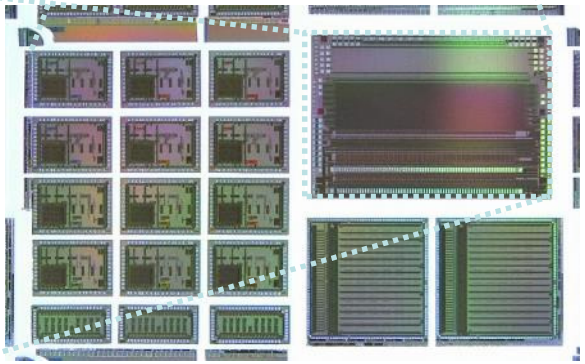
- New CSA & reset circuits
- Enhanced layout & schematics
- New back-end
- Dedicated protocol

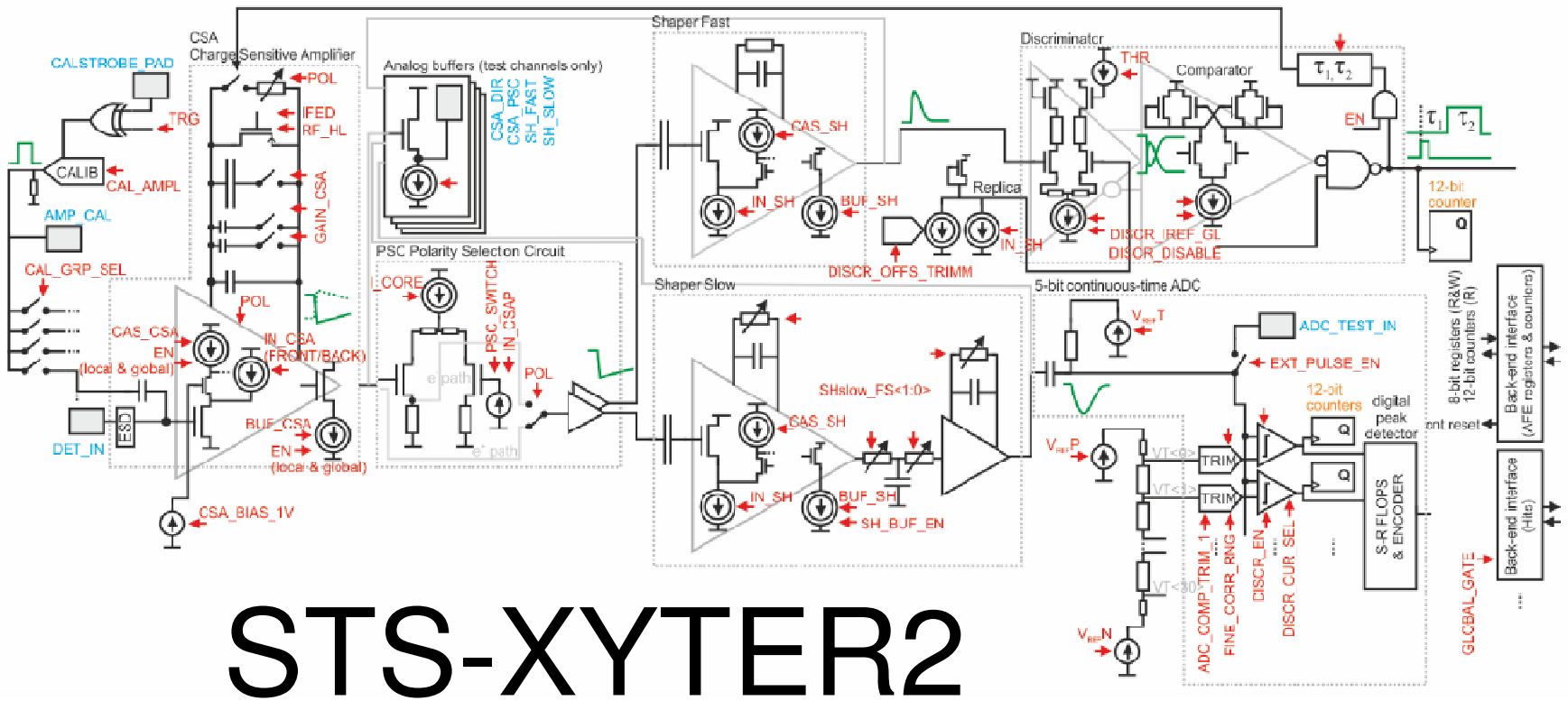






Engineering run wafer after dicing



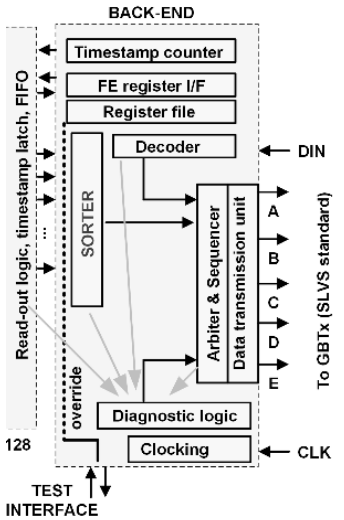


STS-XYTER2

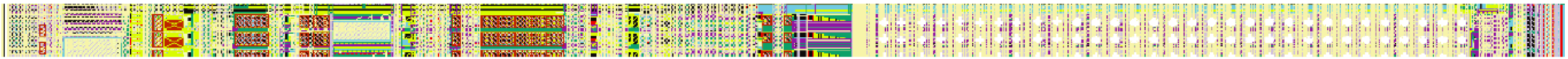
128 channels
time (3.125 ns) & amplitude digitization (5-bit)

0-12 fC electrons & holes (STS)
gain switching & trimming
250 khit/s rate (pulsed reset)
80-280 ns shaping time (slow path)
time-walk corrected offline
continuous-time ADC + peak det.
P=8.5-10 mW/channel (incl. logic)

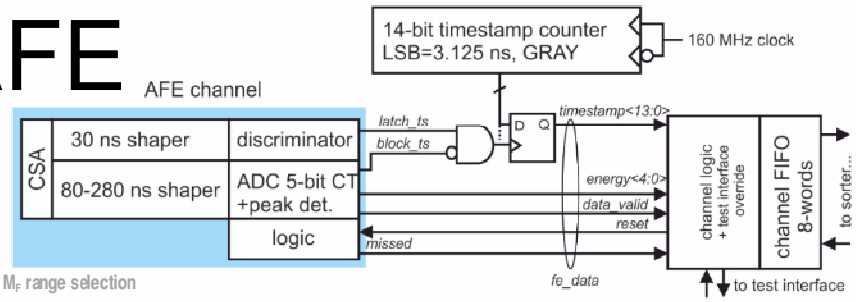
Back-end:
- control via synthesized reg & AFE DICE cells
- 9.41 – 47 Mhit/s/ASIC data BW
- throttling, diagnostic features
- link loopback (multi-level)
- 64-bit e-fuse for traceability

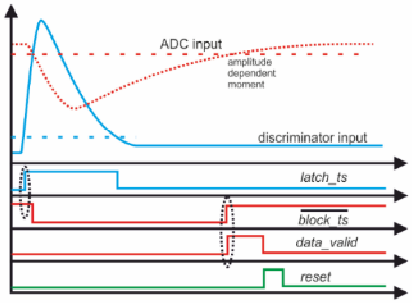


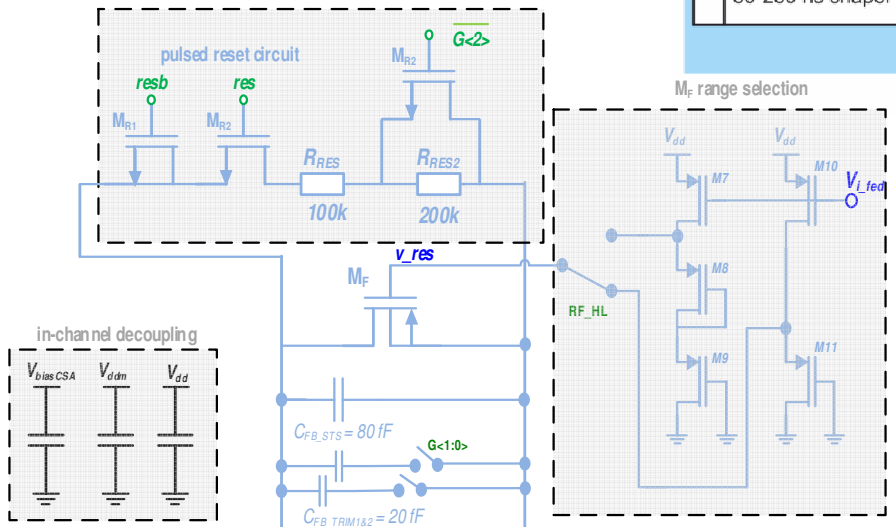
AFE Channel Layout

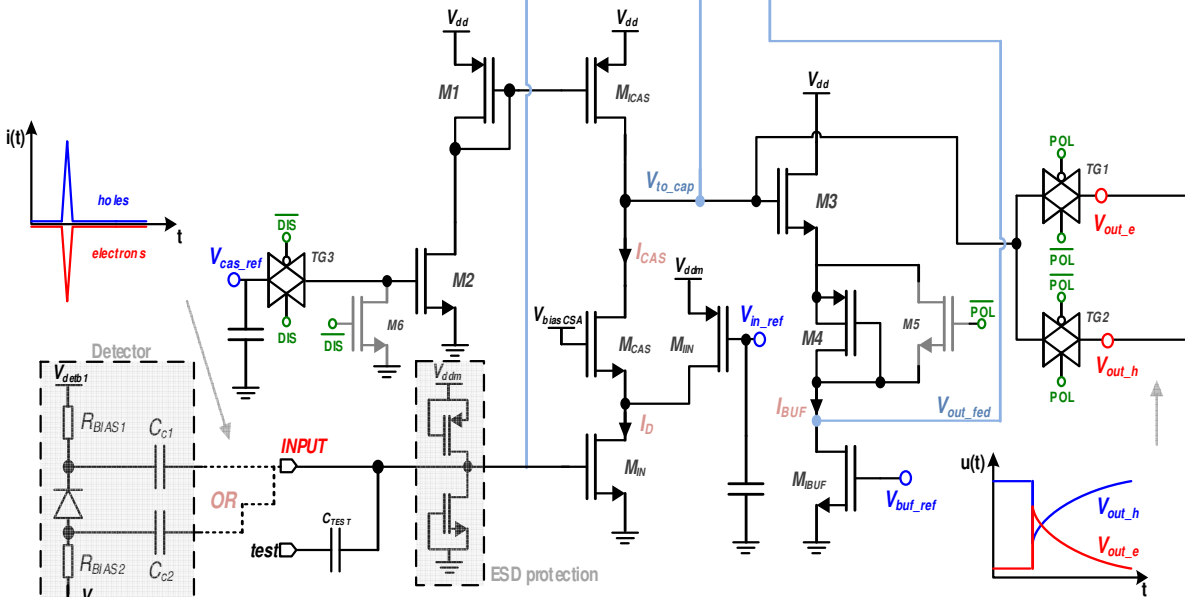


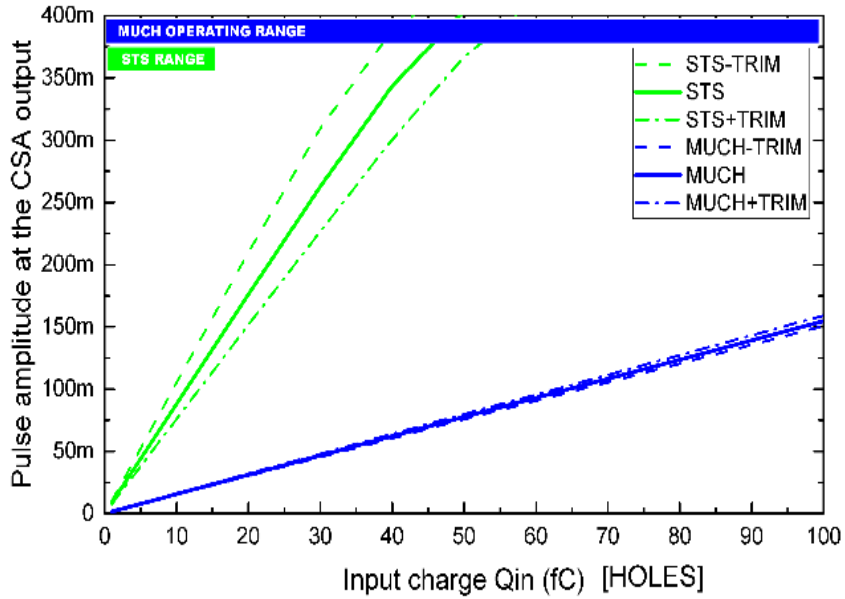
Short blink on AFE

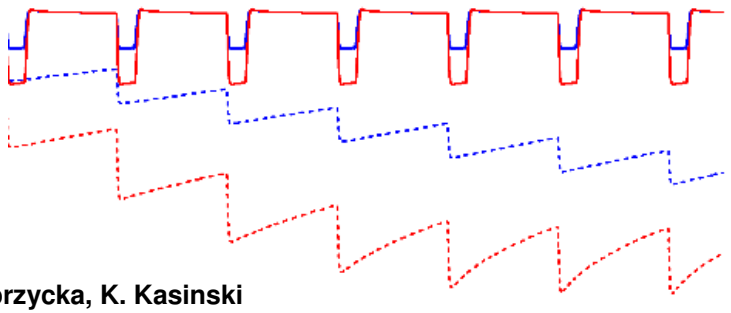










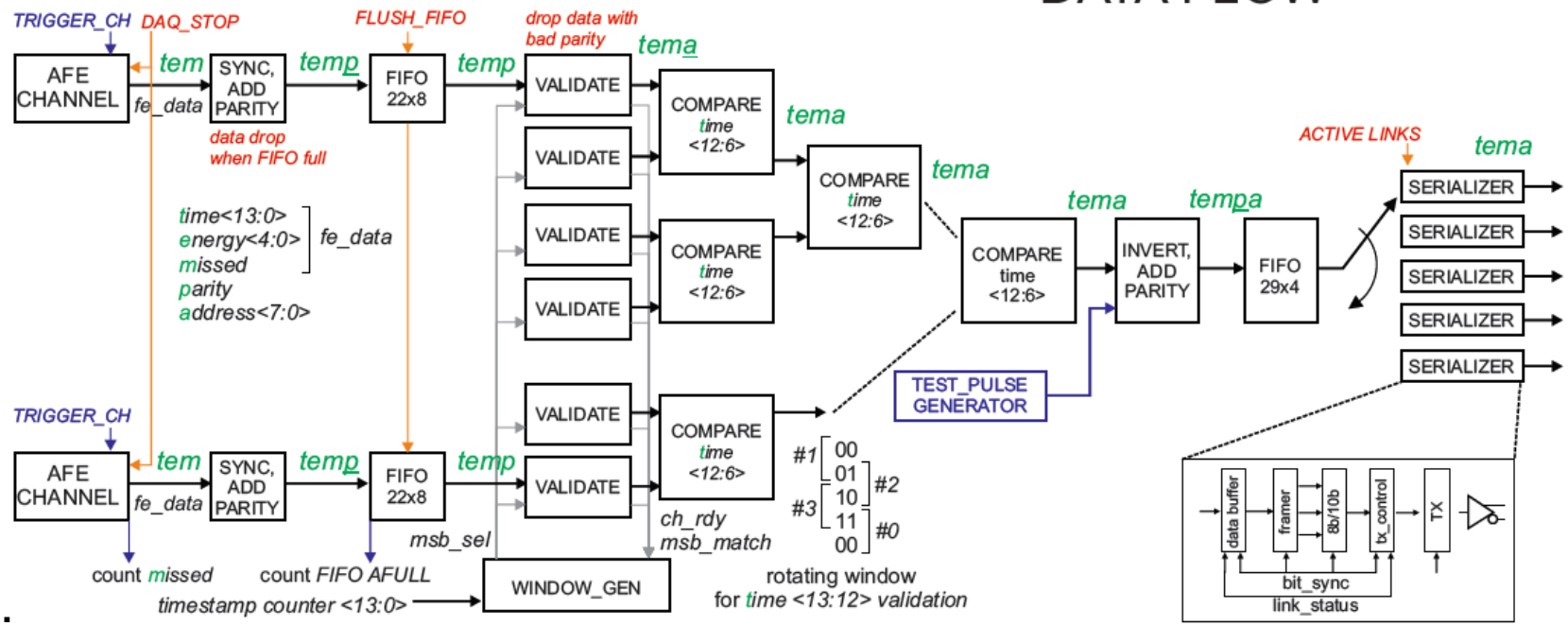


W. Zubrzycka, K. Kasinski
Fast reset of the (...) readout chain in the presence of leakage current
Monday, Poster Session

Temp: -20 – 80 °C P_{CSA} = 2.7 – 5.1 mW

Data flow

AFE > Channel FIFO > Sorter > 5 output serializers

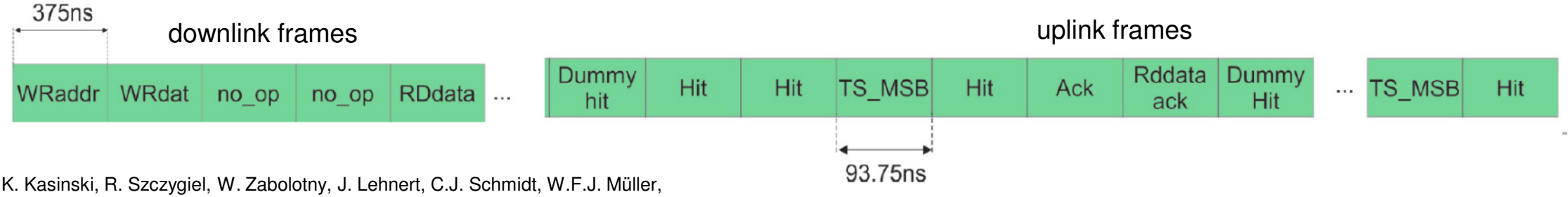


Diagnostic / throttling features:

- test hit generator (multi level, separate generator (rate & content control), channel triggering)
- counting of: event missed, channel FIFO almost full
- channel masking & data drop & FIFOs

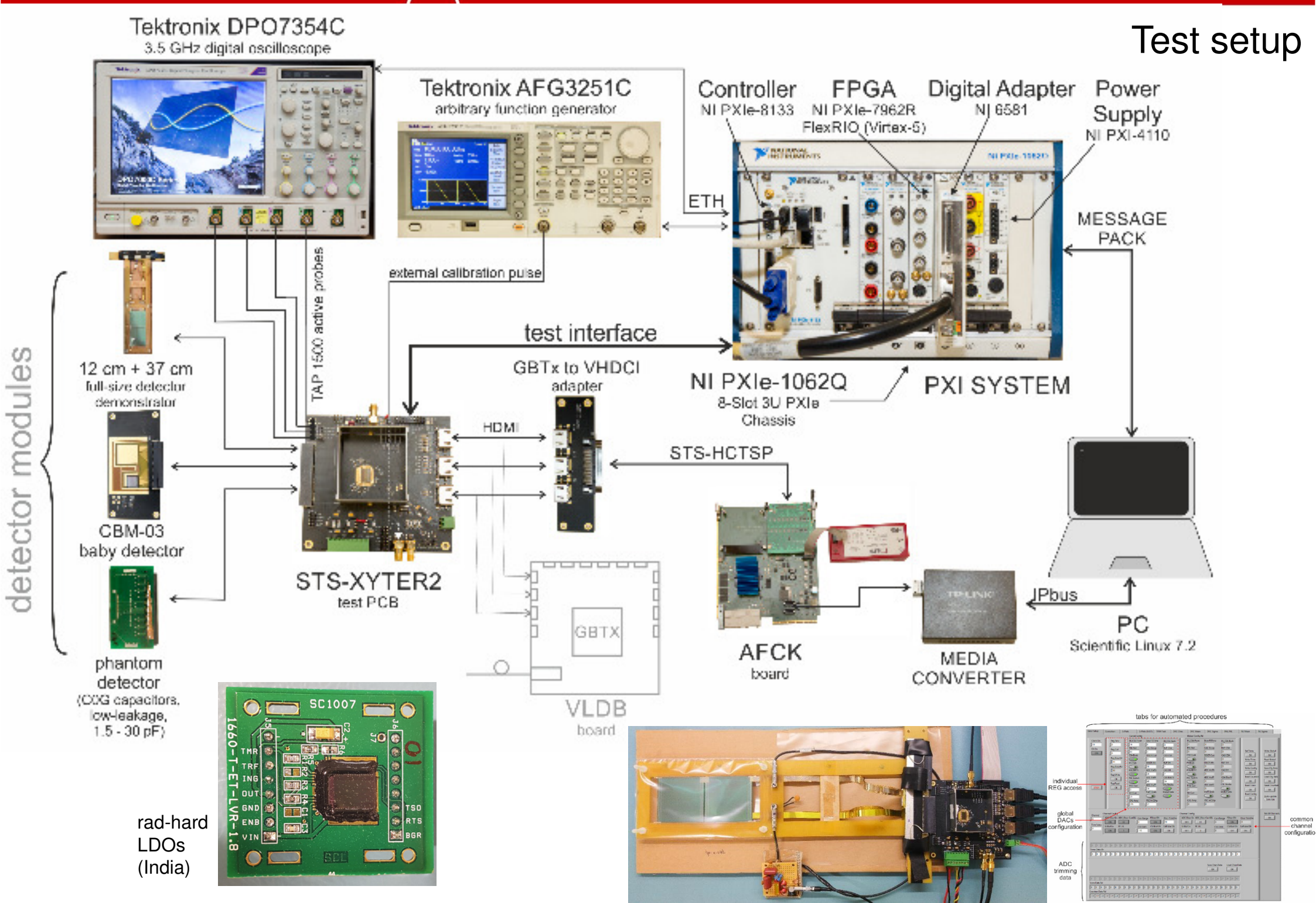
Physical interface on FEB

- shared, multi-drop, AC-coupled 160 Mbps clock & data lines (downlink)
- individual, AC-coupled, 320 Mbps (uplink)
- STS-HCTSP Protocol: fully synchronous, 8b/10b encoding, optimized for STS application, novel link synchronization technique, lossless data compression



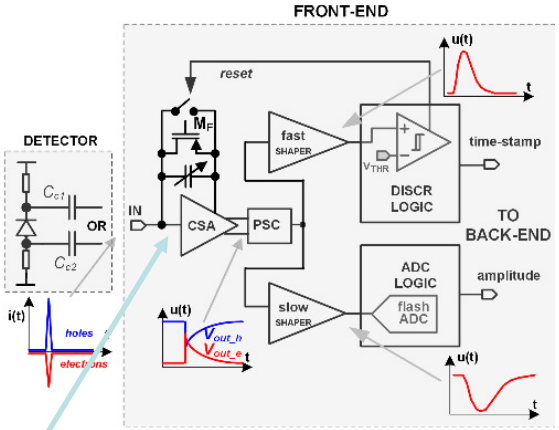
K. Kasinski, R. Szczygiel, W. Zabolotny, J. Lehnert, C.J. Schmidt, W.F.J. Müller,
A protocol for hit and control synchronous transfer for the front-end electronics at the CBM experiment, NIM A 835 (2016) 66–73.

Test setup

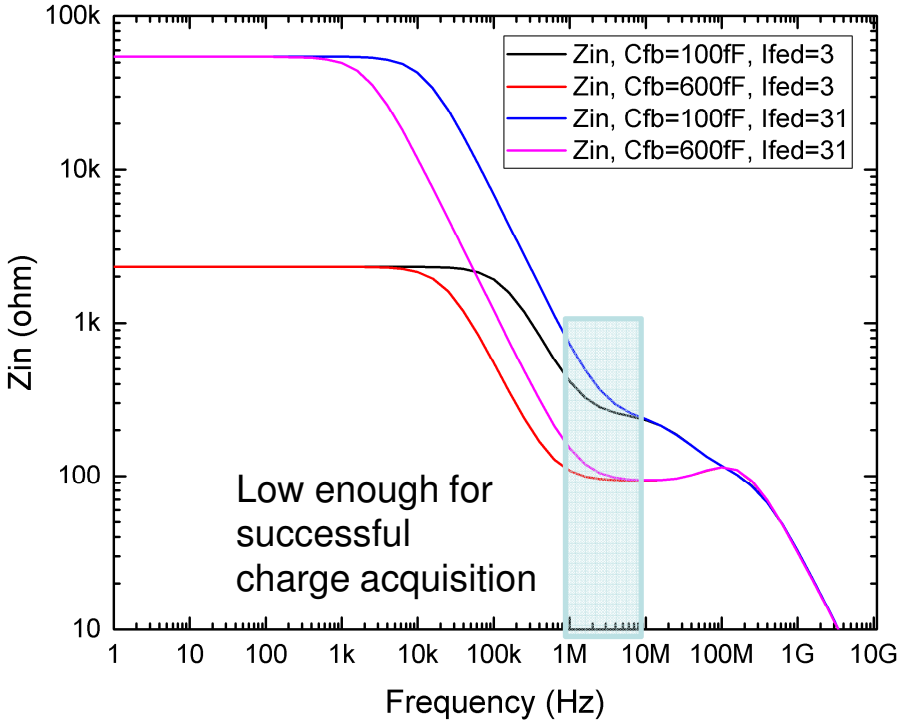

Tektronix DPO7354C
3.5 GHz digital oscilloscope
Tektronix AFG3251C
arbitrary function generator
Controller
NI PXIe-8133
FPGA
NI PXIe-7962R
FlexRIO (Virtex-5)
Digital Adapter
NI 6581
Power Supply
NI PXI-4110
ETH
MESSAGE PACK
external calibration pulse
TAP 1600 active probes
test interface
GBTx to VHDCI adapter
NI PXIe-1062Q
8-Slot 3U PXIe Chassis
PXI SYSTEM
detector modules
12 cm + 37 cm
full-size detector demonstrator
CBM-03
baby detector
phantom detector
(COG capacitors, low-leakage, 1.5 - 30 pF)
STS-XYTER2
test PCB
HDMI
STS-HCTSP
GBTX
VLDB
board
AFCK
board
MEDIA CONVERTER
JPbus
PC
Scientific Linux 7.2
rad-hard LDOs (India)
SC1007
1660-T-ET-LVR-1.8
TMR
TRF
ING
OUT
GND
ENB
VIN
TSO
RTS
BGR
tabs for automated procedures
individual REG access
global DACs configuration
ADC trimming data
common channel configuratio

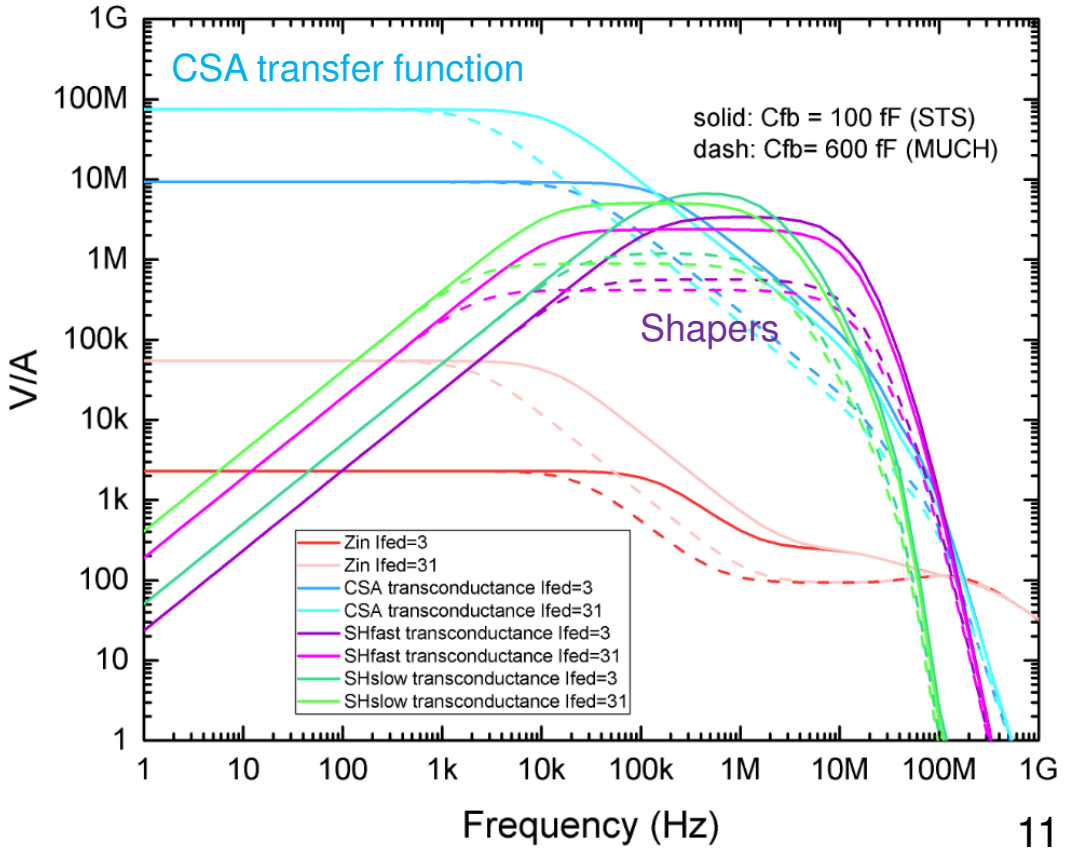
Test results:

- Smoke test: O.K.
- STS-HCTSP Protocol: O.K.
- HW chip addressing: O.K.
- synthesized registers access: O.K.
- DICE AFE registers access: O.K.
- Test hit generator: O.K.
- TS_MSB frame generation O.K.

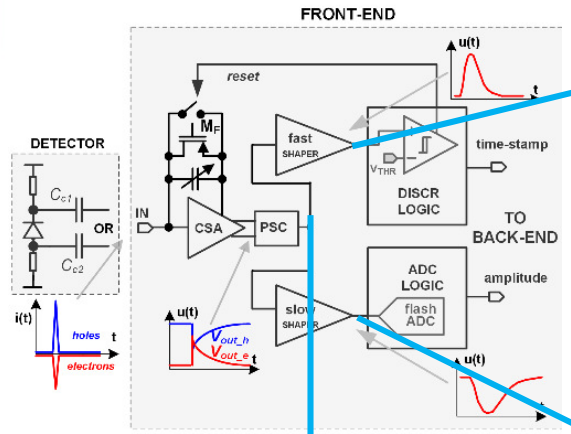


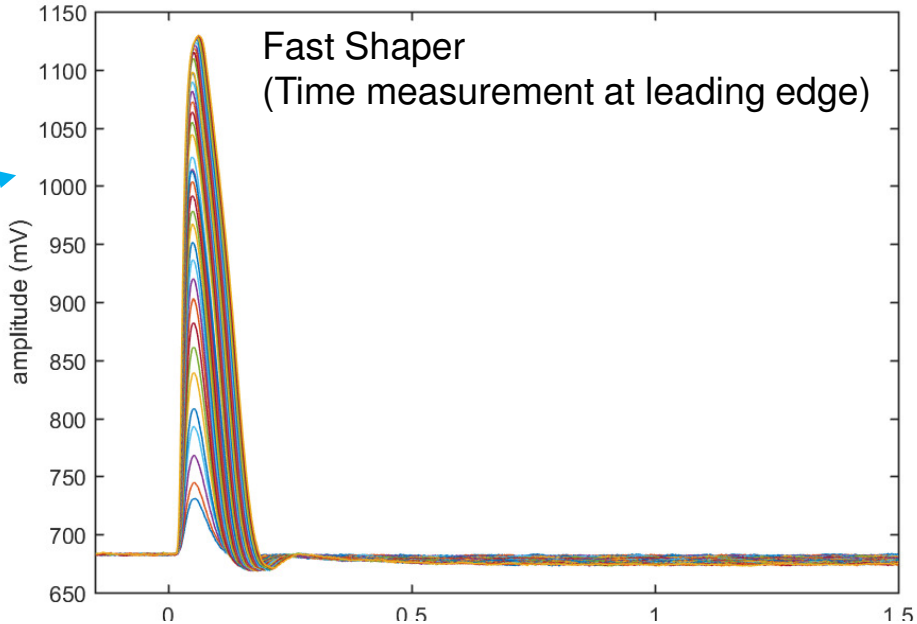
Input impedance



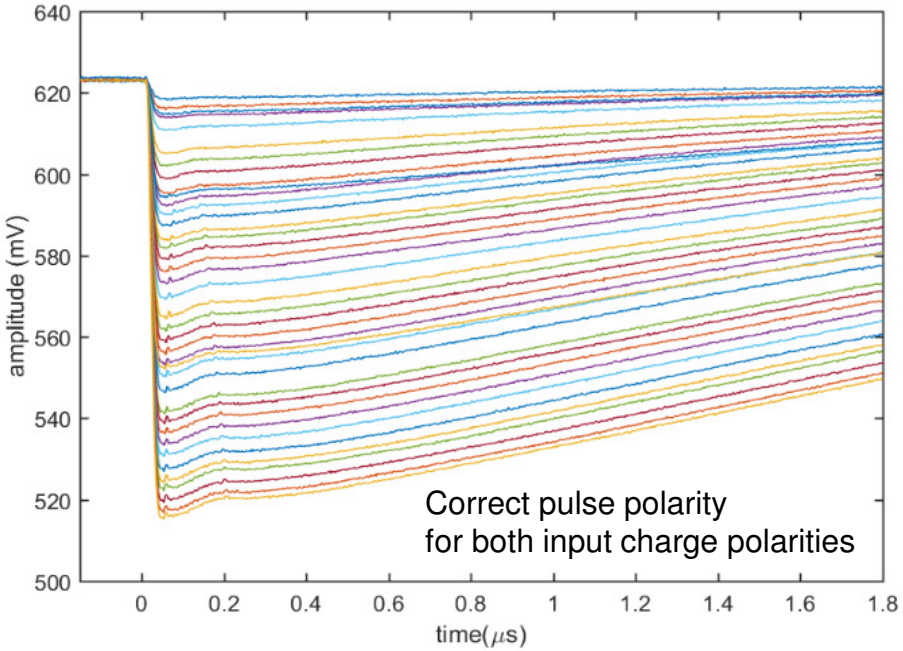


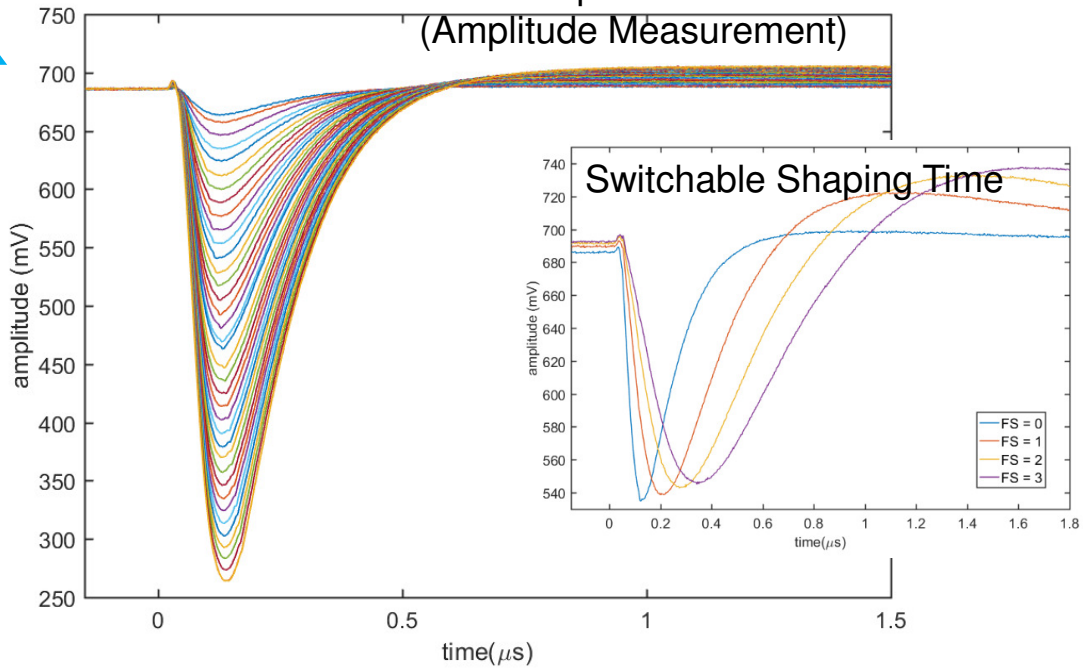
Measured waveforms





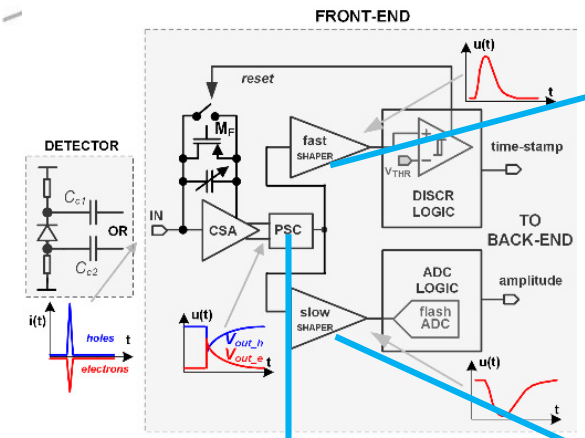
Polarity Selection Circuit

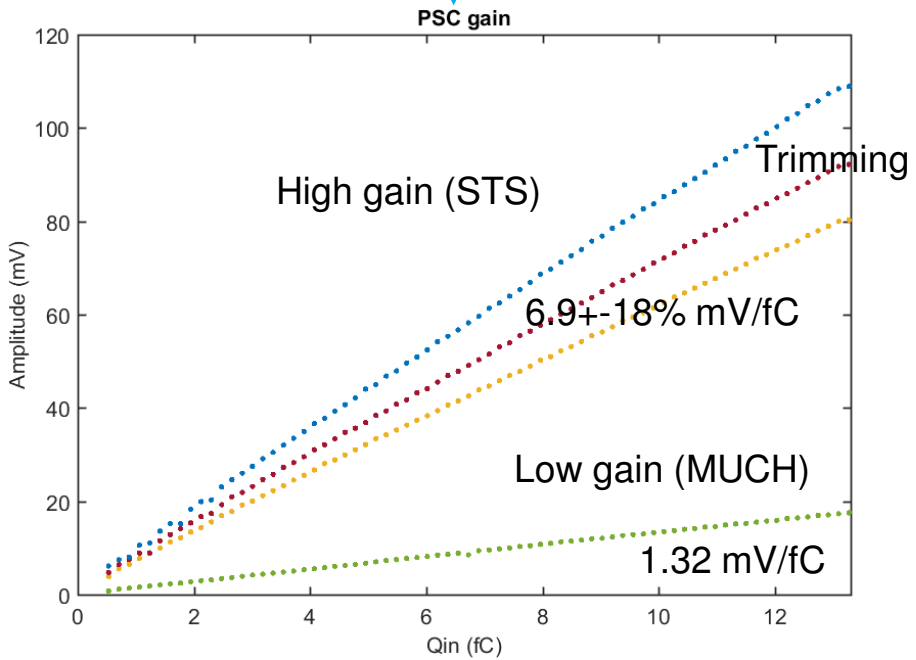


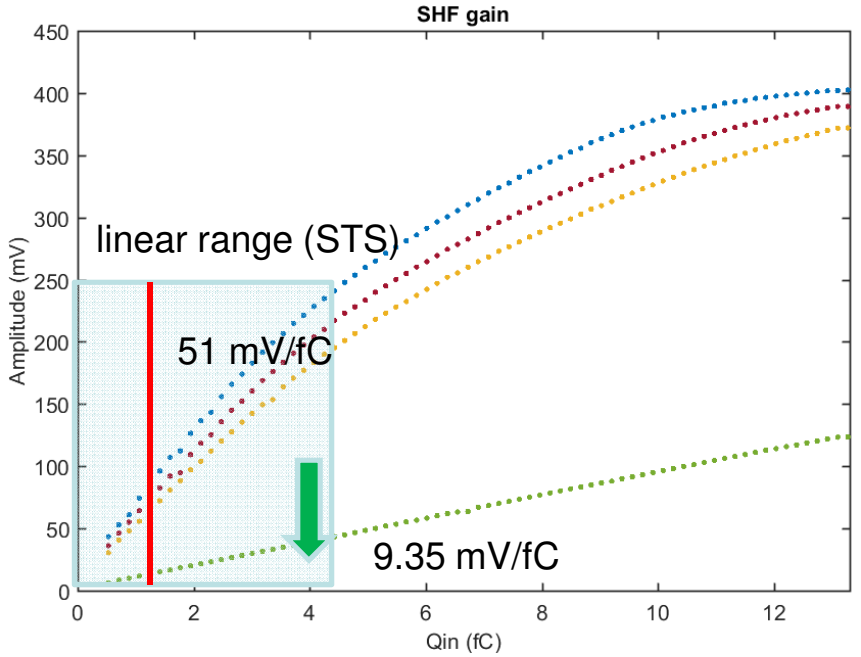


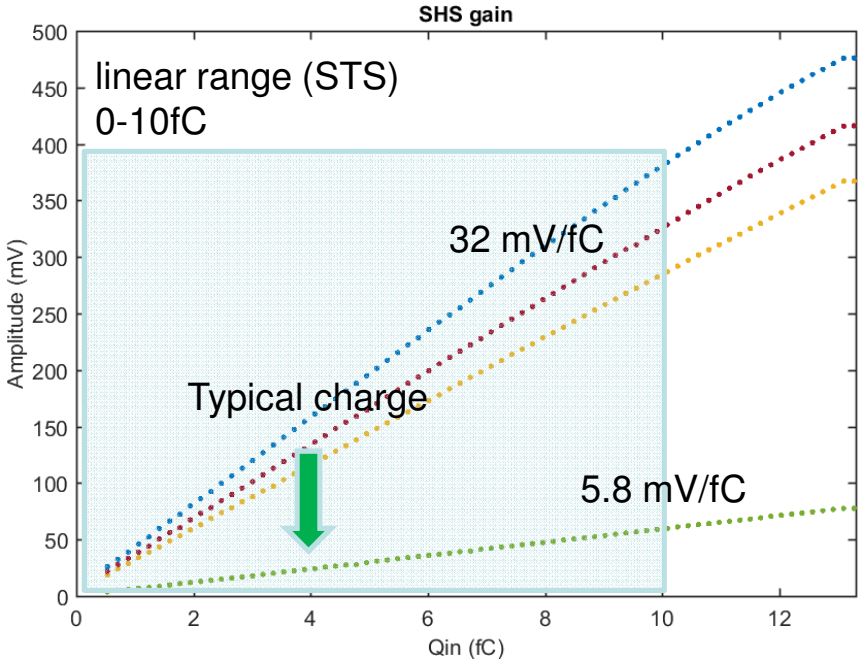
Shaping time setting	0	1	2	3
Measured t_p (ns)	116	190	262	332
Simulated t_p (ns)	90	150	220	280

Measured gain characteristics







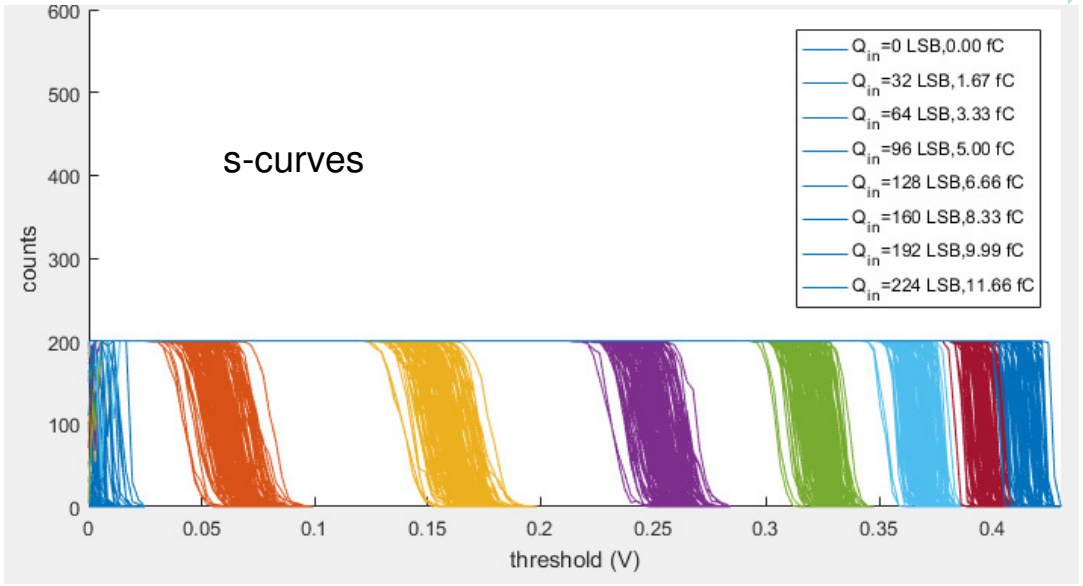


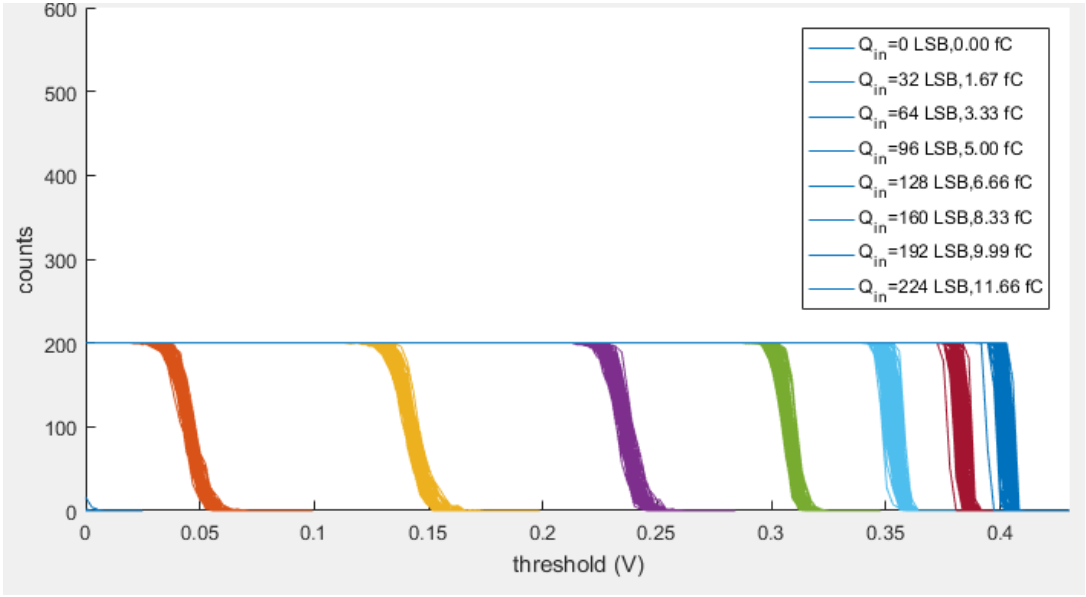
Measured at the buffered outputs of test channels

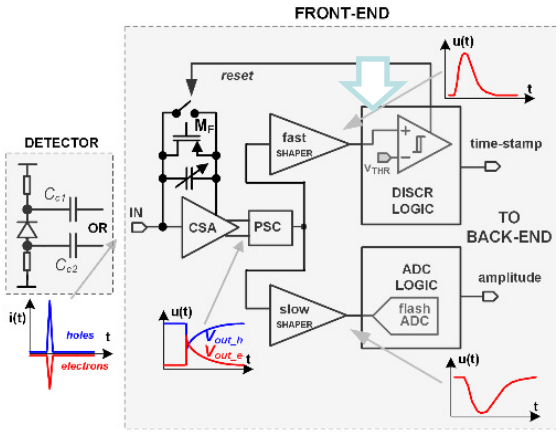
Measured effective discriminator offset spread (128 channels)

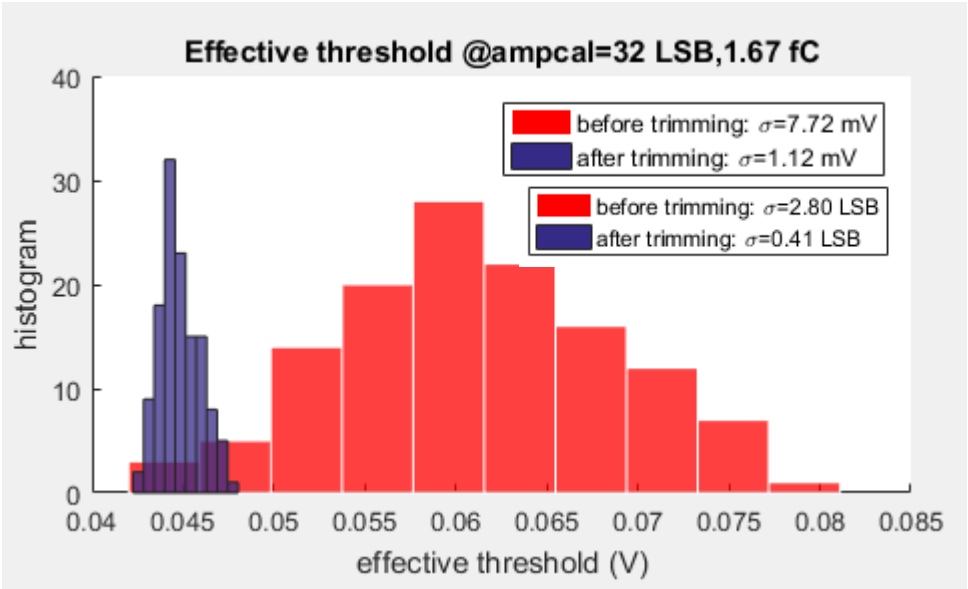
Before trimming

After trimming



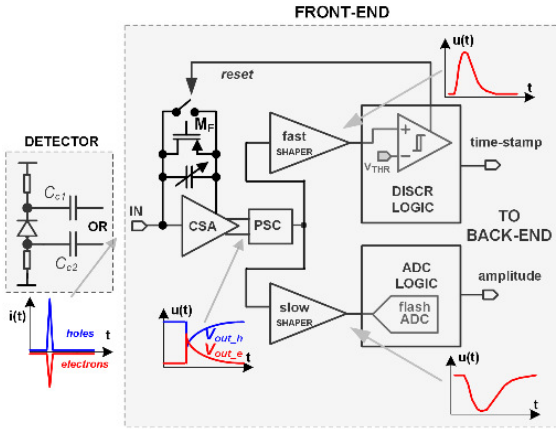


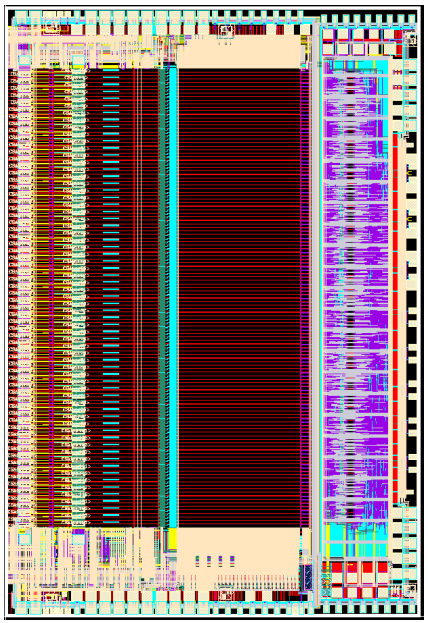




Good matching with simulations.

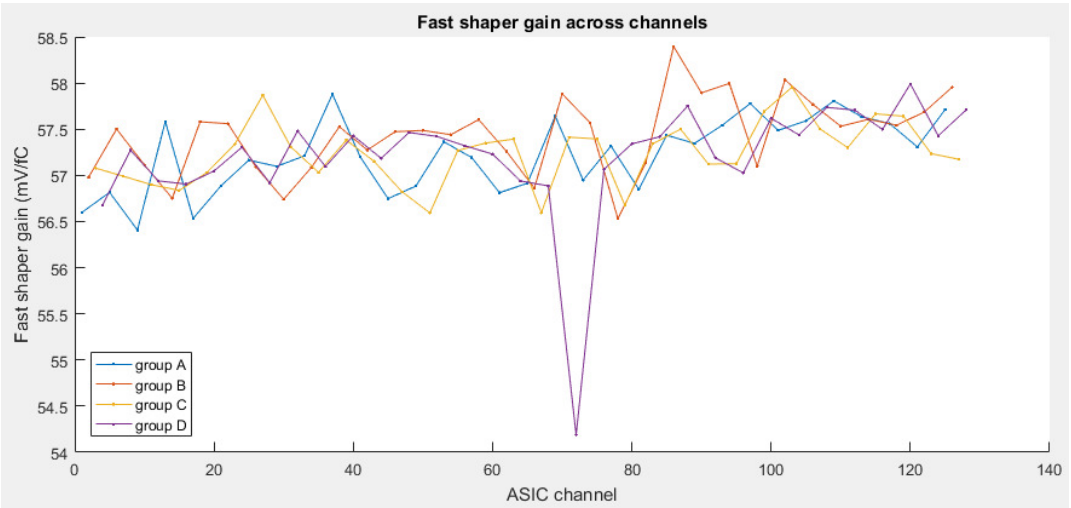
Low offset spread after trimming.

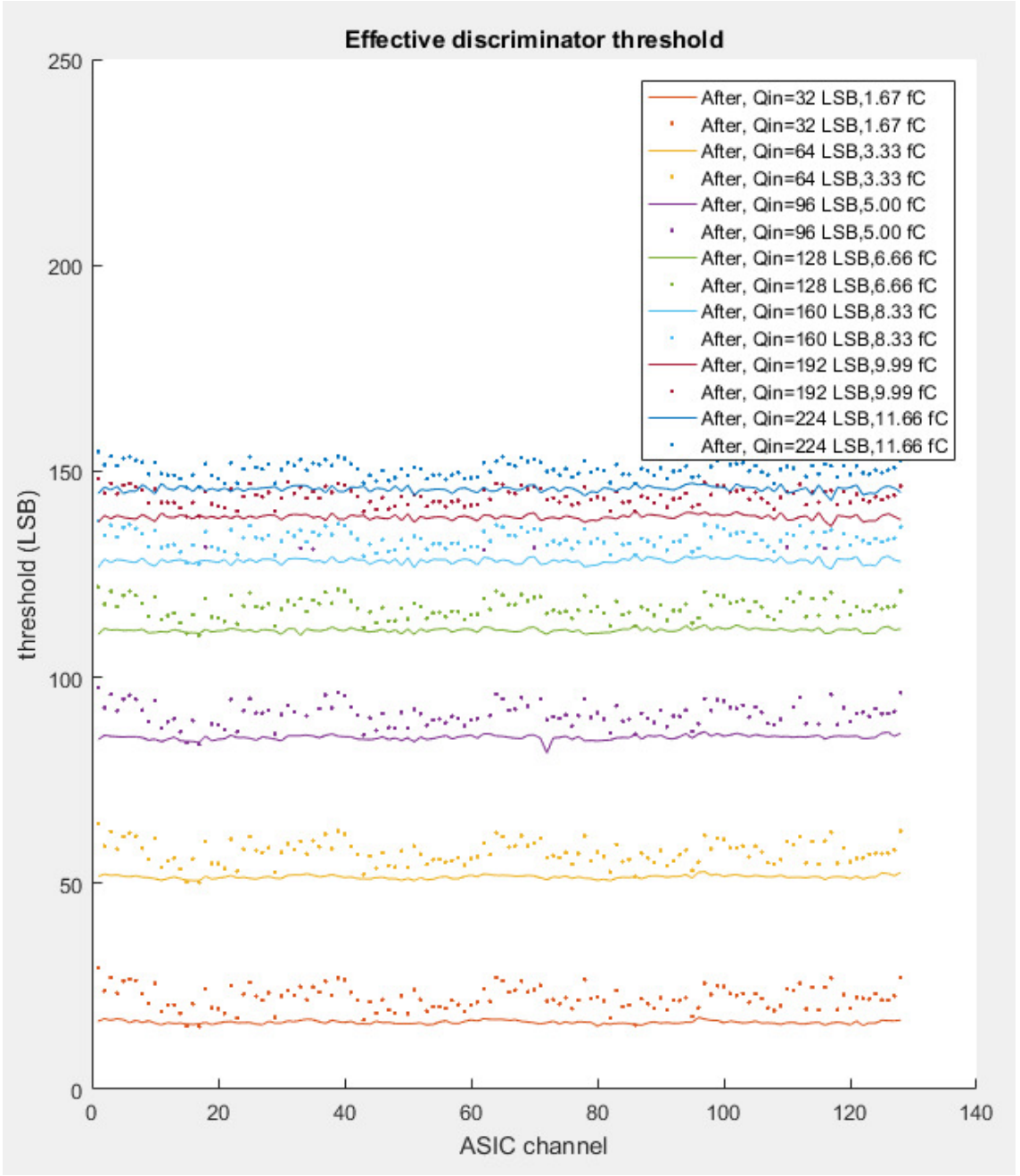




No visible trends across the channels:

- No problematic DC voltage drop on power lines
- No visible problems with biasing

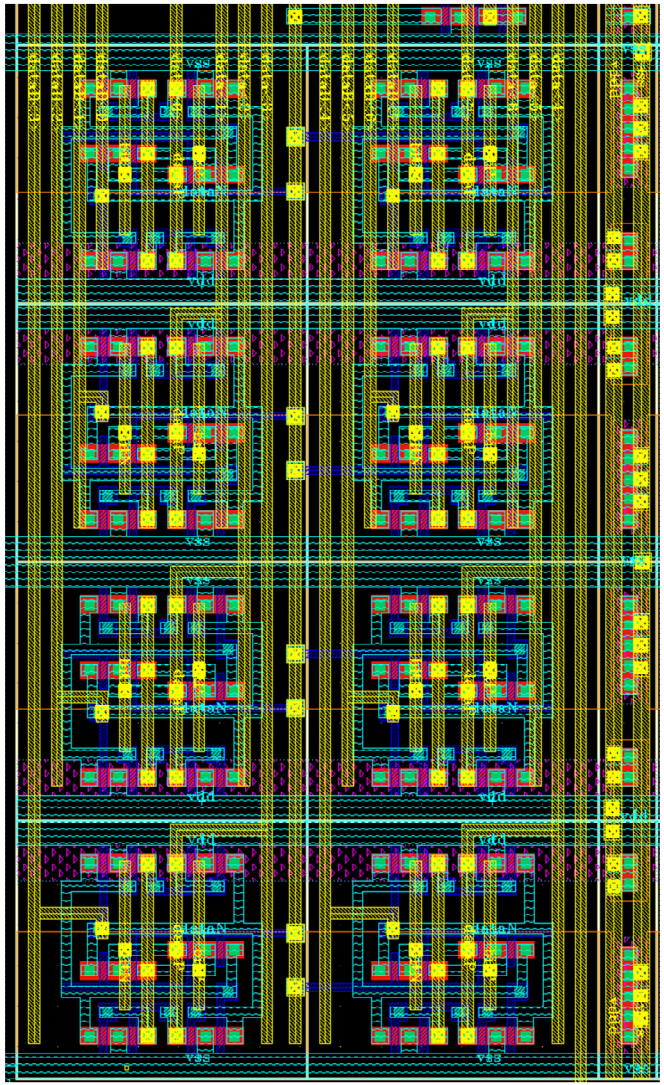




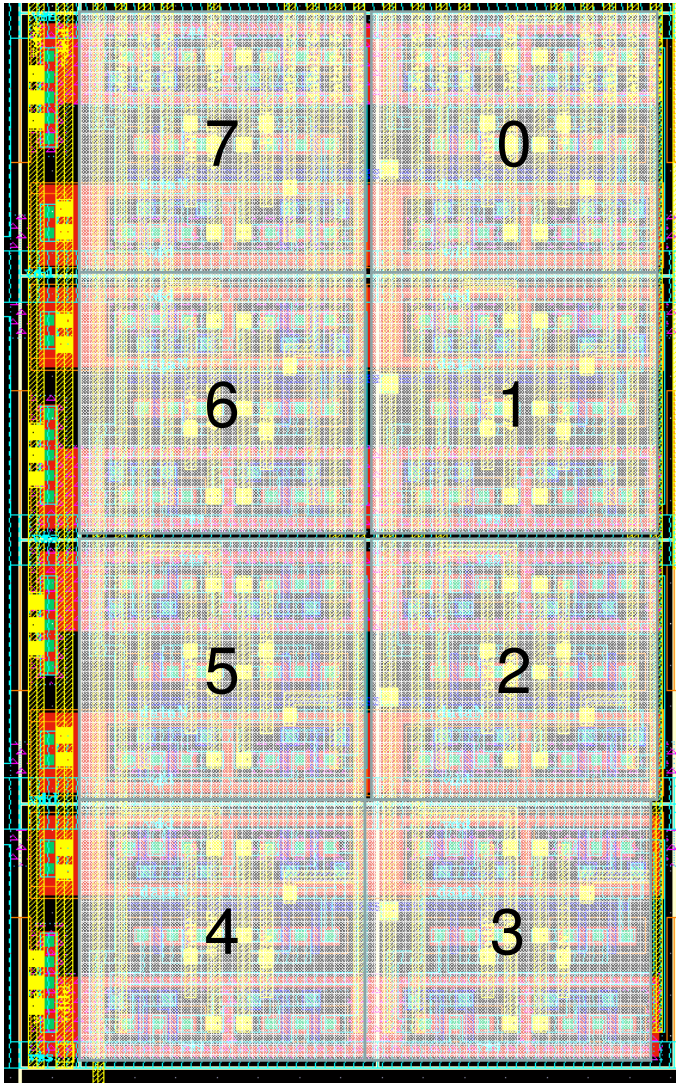
SEU immunity of the configuration memories

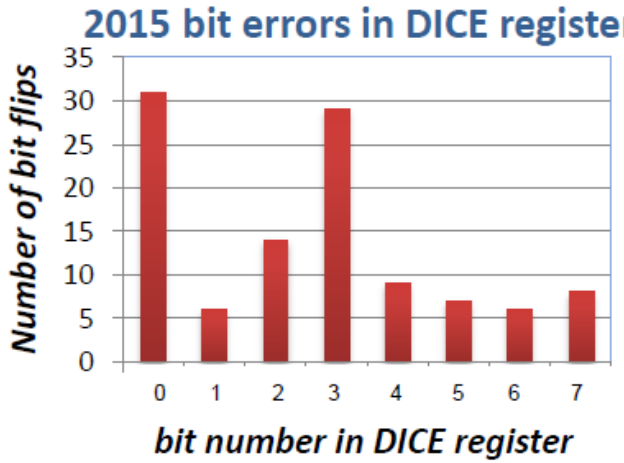
DICE Dual Interlocked Storage Cell

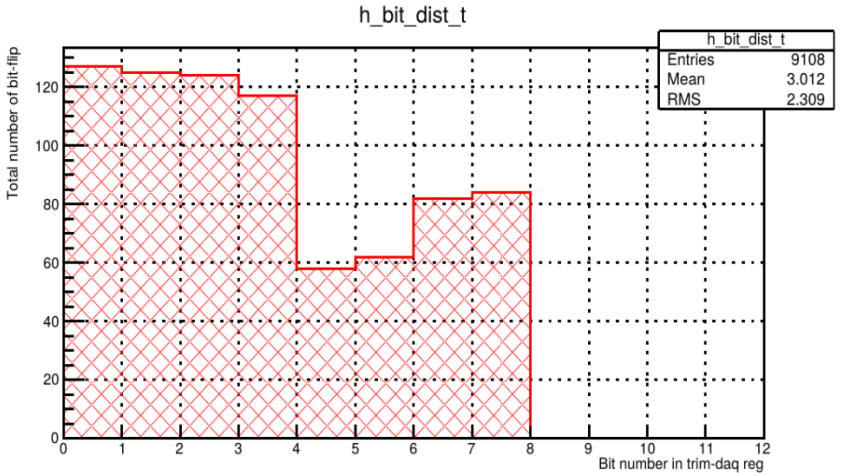
OLD



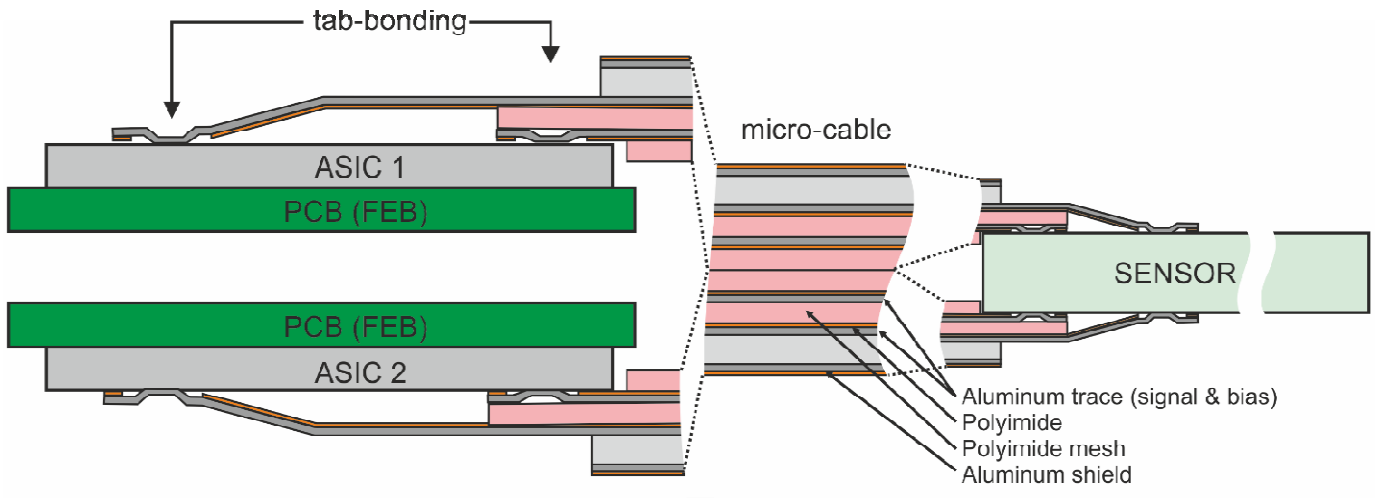
NEW (STS-XYTER2)



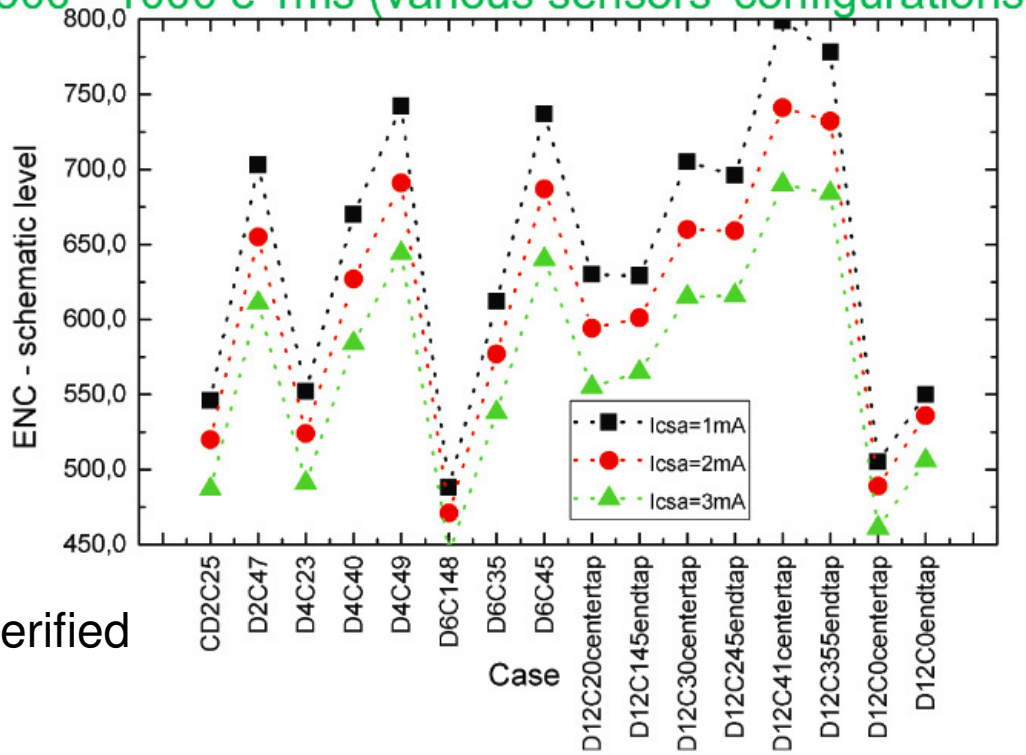




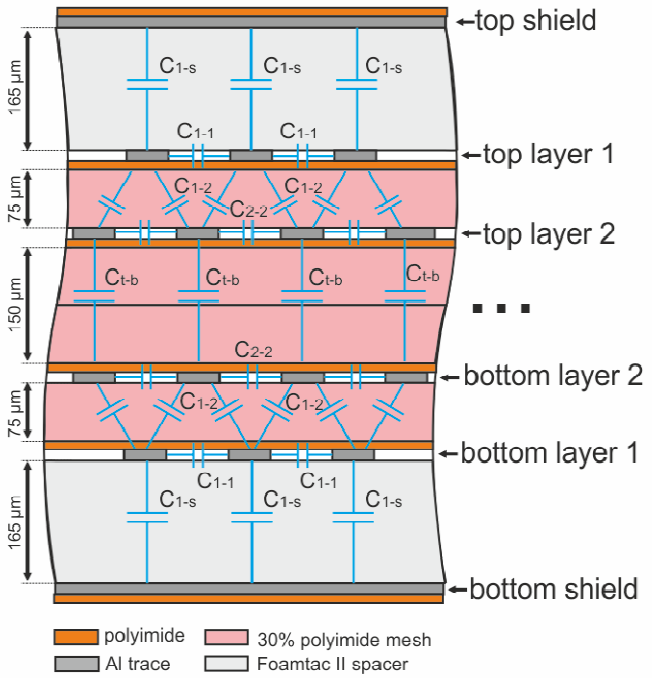
Thanks:
Joerg Lehnert
Adrian Rodriguez-Rodriguez



ENC < 500 - 1000 e⁻ rms (various sensors' configurations)



to be verified

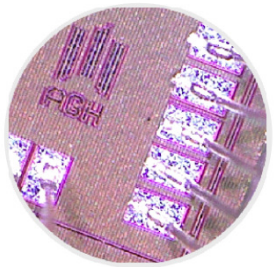


W. Zubrzycka, K. Kasinski, Noise Evaluation of the Silicon Tracking System and Muon Chamber Front-End Electronics, Proc. SPIE 2017.

Summary

- STS/MUCH-XYTER2 ASIC was developed and fabricated
- Chip is an evolution of STS-XYTER full-size prototype with major improvements
  - Optimized for silicon microstrip-based STS detector
    sensor – microcable – ASIC – power co-design
  - Readout option for MUCH GEM sensors
- More, extensive tests are currently in progress
  - tests with GEMs @ VECC, India
  - characterization @ GSI, Darmstadt, Germany
  - beam test @ COSY, Juelich, Germany
- High-volume production planned 2017/2018

Thank you for your attention



Krzysztof KASINSKI,
Weronika ZUBRZYCKA,
Robert SZCZYGIEŁ

K. Kasinski, R. Szczygiel, et al., JINST 2016 vol. 11
K. Kasinski, R. Kleczek, R. Szczygiel, JINST 2016 vol. 11.
K. Kasinski, R. Szczygiel, W. Zabolotny, JINST 2016 vol. 11.
K. Kasinski, R. Szczygiel, et al., NIM A (2016).
K. Kasinski, W. Zubrzycka, Proc. SPIE (2016).
K. Kasinski, R. Kleczek, Proc. MIXDES (2016).
K. Kasinski, at al., JINST 2017 vol. 12.
W. Zubrzycka, K. Kasinski, Proc. SPIE (2017).

Common effort of:
AGH, Kraków: P. Otfinowski, R. Kleczek
GSI, Darmstadt: J. Lehnert, A. Rodriguez, C. J. Schmidt, W. F. J. Mueller, P. Koczon, C. Simons et al.,
WUT, Warsaw: W. Zabolotny, G. Kasprowicz, A. Byszuk and others

http://www.kmet.agh.edu.pl/katedra-metrologii/zespoly-badawcze/asics/?lang=en