# Fast Reset of the Silicon Microstrip and Gas Electron Multiplier Readout Chain in the Presence of Leakage Current



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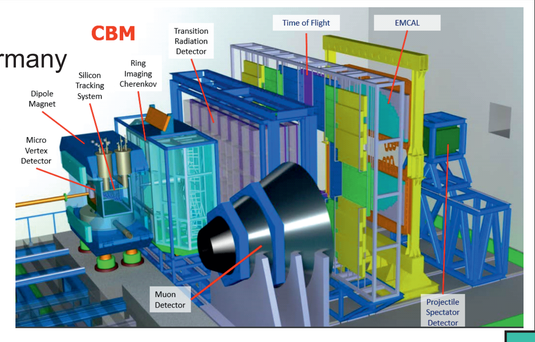
Diamentowy Grant


## Introduction

Compressed Baryonic Matter Experiment at FAIR, Germany




**Silicon Tracking System (Si strip)**

ENC <1000 e- rms
< 10 mW/channel
58 um pitch
128 channels
250 kHit/s/channel
0-10 fC range (linear)
20-50 pF sensor capacitance
e- e+ input charge polarity

**Muon Chamber (GEM)**

< 10 mW/channel
100 um pitch
64 channels

0-100 fC range (linear)
~ 50 pF sensor capacitance
single charge polarity

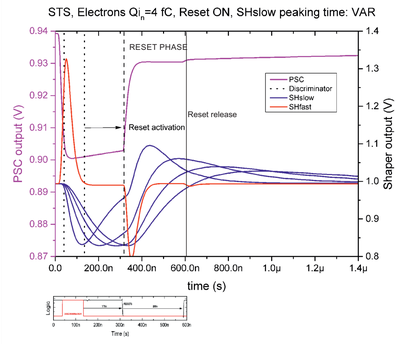
**Other detectors**

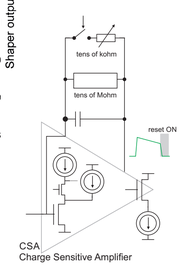
**Need for common readout IC** Most requirements are common or can be met in a single circuit.

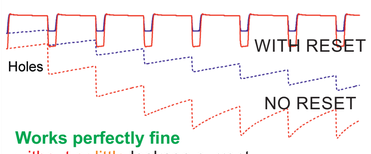
SPECIFIC REQUIREMENTS RELEVANT FOR THIS POSTER

**NEED FOR FAST BASELINE RECOVERY**
High expected rate: 250 kHit/s/channel
Beam intensity fluctuations can cause overload

**DIGITALLY-ASSISTED ANALOG CIRCUIT**
RESET OF FEEDBACK LOOP IN CSA
IN PARALLEL WITH
HIGH-VALUE RESISTANCE



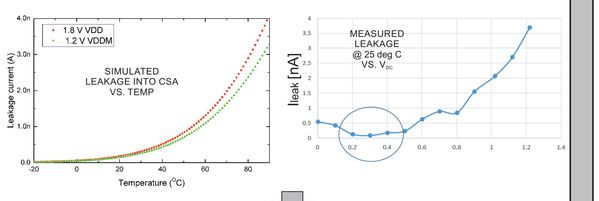




**Works perfectly fine**
without or little leakage current

**NEED FOR ESD PROTECTION AT EACH CSA INPUT!**
Silicon Microstrip & Gas Electron Multipliers (in particular)

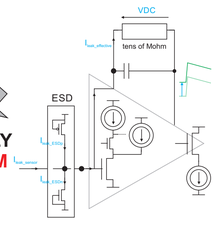
**ESD PROTECTION DIODES -> LEAKAGE CURRENT**
**SENSOR / INTERCONNECT IMPERFECTION -> LEAKAGE CURRENT**




LEAKAGE CURRENT + RESISTOR = VOLTAGE DROP
(nA range) (Mohm range) mV range

Even small (several nA) leakage currents resulting either from the protection circuit or other, external source can influence the operation of circuits, in particular when high- value feedback resistance is used in the input amplifier feedback (causing the voltage difference between the amplifier input and output nodes).

ESD -RELATED LEAKAGE CAN BE OF BOTH POLARITIES & VARIES WITH TEMPERATURE AND DC POTENTIAL AT CSA INPUT




Small DC drop itself (~tens of mV) is NOT a problem.

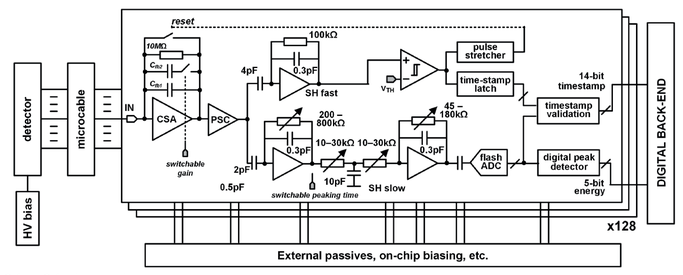
It CAN modify the effective feedback resistance of MOS transistor (increase or decrease).

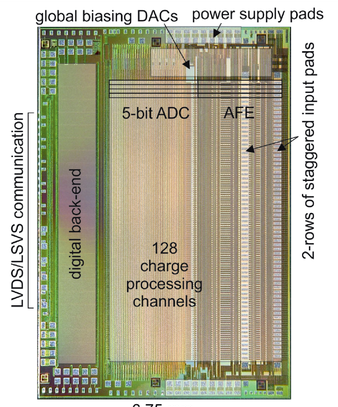
If large enough can saturate amplifier.

**TWO EFFECTS JOINTLY RESULT IN A PROBLEM**

## Prototype Readout IC for STS/MUCH

STS-MUCH-XYTER2 (SMX2) Prototype ASIC was developed & fabricated in Q3 2016



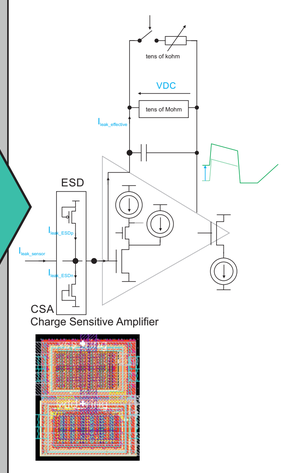

64 + 64 channels
Charge-Sensitive Amplifier + [CR-RC (fast) + comparator] + [CR-RC$^3$ (slow) + ADC continuous-time]
Flexible configuration of analog front-end (AFE), gain switching, **fast reset**, shaping time switching
5-bit amplitude & 14-bit timestamp measurement
die size: 10 mm x 6.75 mm
UMC 180 nm CMOS MM/RF

See THIS IWORID Talk:
Wed 05.07 9:00 K. Kasinski
„Test results of the STS/MUCH-XYTER2, (...)"

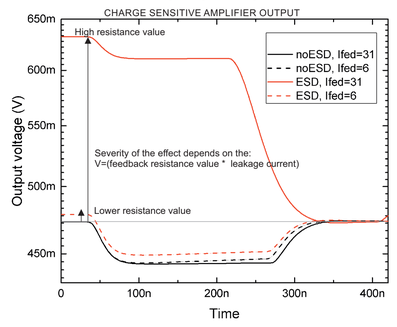

K. KASIŃSKI, P. Koczon, S. Ayet, S. Löchner, C.J. Schmidt, System-level considerations for the front-end readout ASIC in the CBM experiment from the power supply perspective, Journal of Instrumentation, 2017 vol. 12 art. no. C03023.
K. KASIŃSKI, R. SZCZYGIEL, W. Zabolotny, Back-end and interface implementation of the STS-XYTER2 prototype ASIC for the CBM experiment, Journal of Instrumentation, 2016 vol. 11 art. no. C11018.
K. Kasinski, R. Szczygiel, W. Zabolotny, J. Lehnert, C.J. Schmidt and W.F.J. Müller, A protocol for hit and control synchronous transfer for the front-end electronics at the CBM experiment, Nucl. Instrum. Meth. A 835 (2016) 66.
K. Kasinski, R. Kleczek and R. Szczygiel, Front-end readout electronics considerations for Silicon Tracking System and Muon Chamber, 2016 JINST 11 C02024.


## Fast reset circuit and leakage current effect

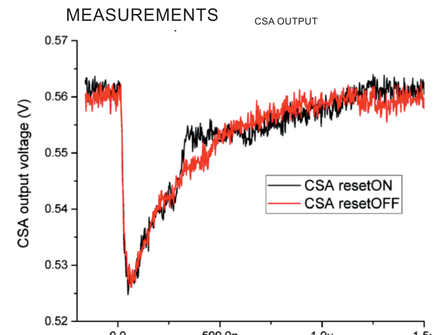
The low resistance of the pulsed reset bypasses the large resistance of the continuous reset path (feedback resistance) thus changing the DC level at the Charge Sensitive Amplifier (CSA) output. After the reset is released, changing conditions appear as fake incoming charge (because the CSA output drifts back to the original DC output voltage). The fake pulse appearing at the CSA output could interfere the subsequent stages (shapers).



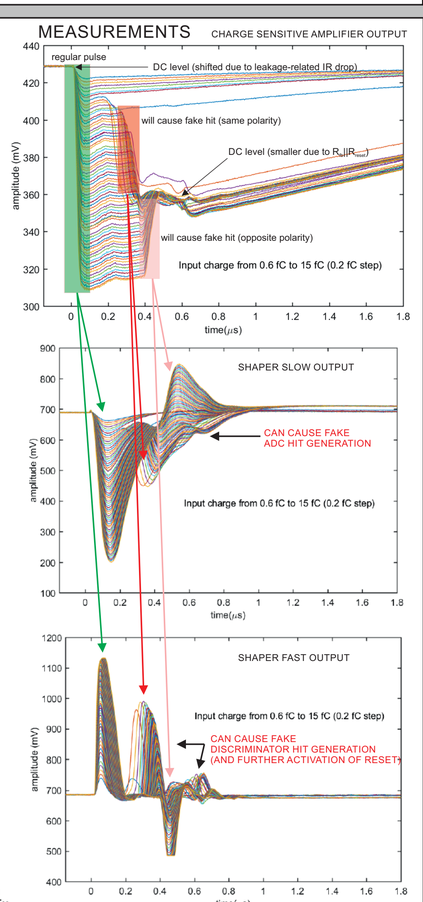

SIMULATION



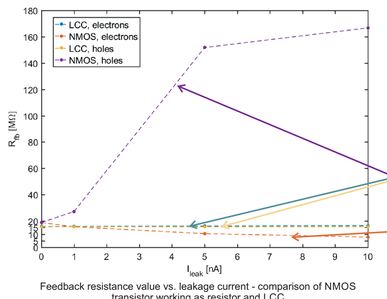

MEASUREMENTS



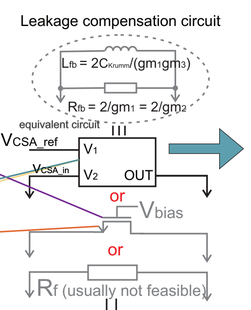

MEASUREMENTS




## The leakage compensation circuit

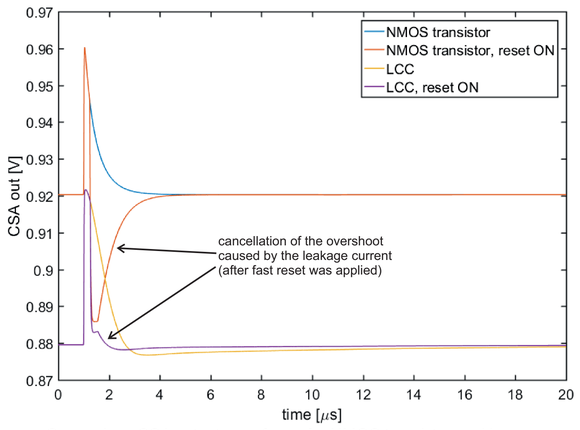



Feedback resistance value vs. leakage current - comparison of NMOS transistor working as resistor and LCC



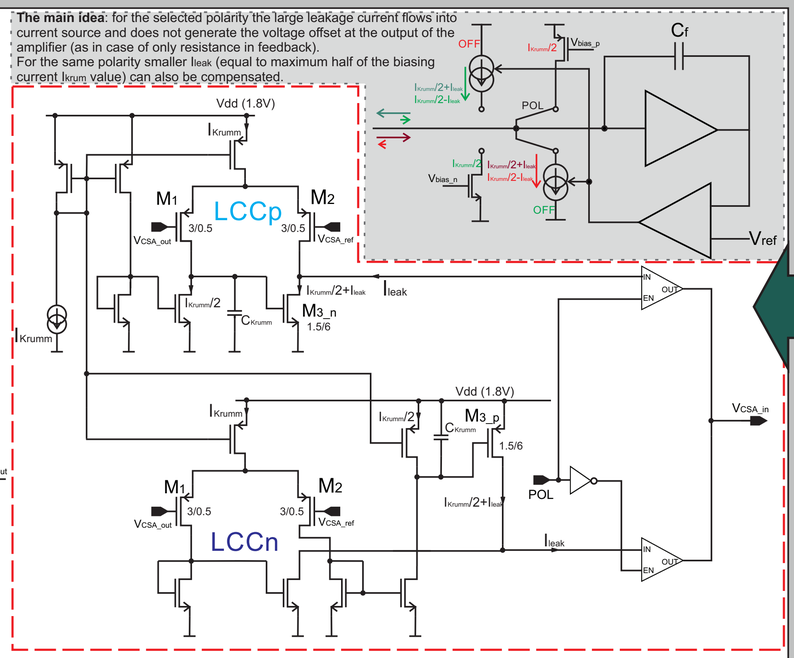

Rfb for LCC: from 6MΩ ($I_{krum}$ = 30 nA) to 40 MΩ ($I_{krum}$ = 4 nA)

Relative change of feedback resistance due to the leakage current:
- NMOS transistor: 5.88%/nA (electrons), -78.29%/nA (holes)
- LCC : **0.341%/nA** (electrons), **-0.03%/nA** (holes)

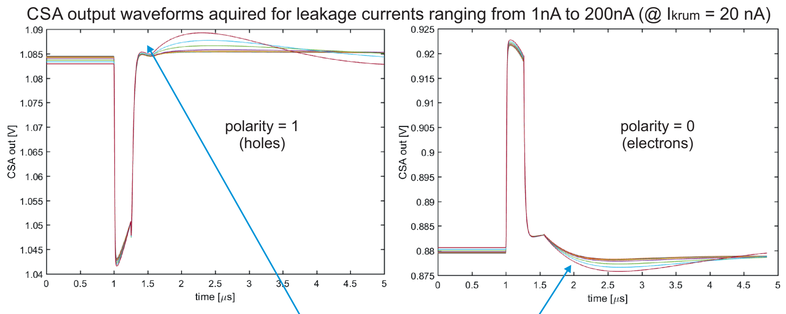


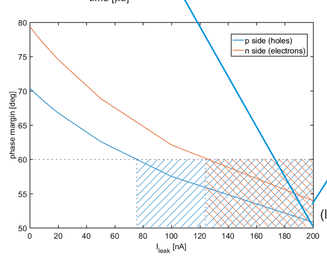

Comparison CSA output waveforms for NMOS transistor working as feedback transistor and for LCC as feedback resistor with and without fast reset enabled (@ $I_{krum}$ = 12 nA, $I_{leak}$ = 5 nA)

**The main idea**: for the selected polarity the large leakage current flows into current source and does not generate the voltage offset at the output of the amplifier (as in case of only resistance in feedback).
For the same polarity smaller $I_{leak}$ (equal to maximum half of the biasing current $I_{krum}$ value) can also be compensated.




CSA output waveforms aquired for leakage currents ranging from 1nA to 200nA (@ $I_{krum}$ = 20 nA)



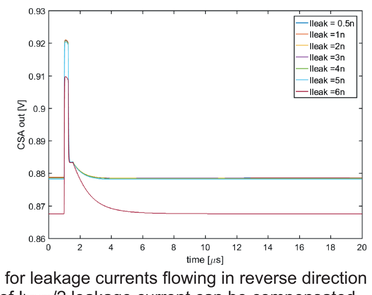




Increase of the leakage current -> change of the low frequency pole, related to the transconductance of M3 transistor and Krummenacher capacitance $C_{Krum}$

Taking into account maximum leakage current present in the system and layout area constraints, M3 transistor size and $C_{Krum}$ value were optimized to achieve minimum overshoot.

stability issues (larger overshoot)

- **Trade-off: feedback resistance vs. maximum leakage current that can be compensated**
  - preferably high $R_{fb}$ (low Krummenacher current)
  - high compensation capabilities: in normal operating conditions (with nominal leakage current flow direction) and with leakage current flowing in opposite direction -> high Krummenacher current




CSA output waveforms aquired for leakage currents flowing in reverse direction (@ $I_{krum}$ = 10 nA) - maximum of $I_{krum}$/2 leakage current can be compensated

- **Leakage current from sensor (larger)** - the polarity determined, same as the charge polarity -> compensated by the part of the LCC selected by the polarity selection bit (switch)
- **Leakage current from ESD protection circuit (small)** - the polarity depends on the temperature, independent on the charge polarity, the leakage current origin from ESD circuit has to be compensated by the LCC regardless of the polarity
- The input transistor pairs of both parts of the LCC - PMOS (the potential on the CSA input ~450 mV, NMOS pair can not be used).

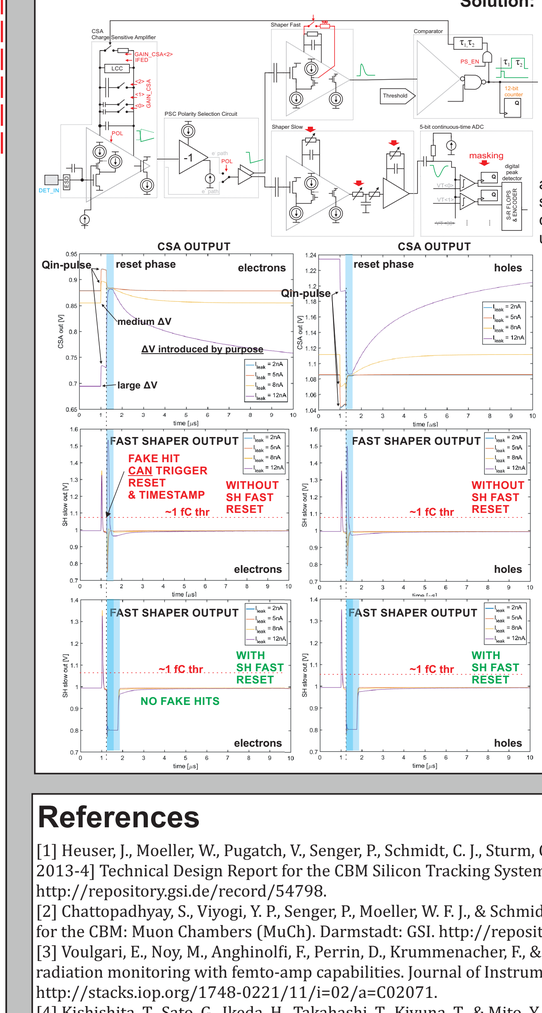
- **Advantages:**
  - compensation of sensor's leakage (known polarity) and of ESD diodes' leakage (polarity dependent of the temperature)
  - no voltage offset at the output of the amplifier caused by the leakage current present in system
  - configurable feedback resistance value (worse than typical MOS resistor)
  - feedback resistance independent of the leakage current

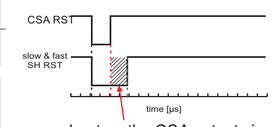
The presented approach implements a leakage current compensation for both polarities of this current to reduce the voltage offset at the CSA output and a sequenced pulsed reset of all three stages of the charge processing to achieve very fast recovery from overload regardless of harsh operating conditions.

## Sequenced reset

**AIM: Make circuits insensitive to any transients that can occur during reset phase.**

**Solution:**

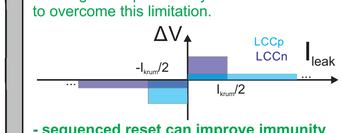



an overshoot on the CSA output signal -> shapers should not respond with signal containing second pulse with polarity that can fire up the comparator / ADC

**Conclusions:**

- High-value feedback resistances (> 10 MΩ) are common in charge-sensitive amplifiers.
- Growing speed requirements impose using digitally-assisted circuits (e.g. pulsed reset).
- Even small leakage current can compromise the functionality (e.g. ESD-protection).
- **Krummenacher circuit can successfully compensate the leakage current.**
- Its capabilities are non-symmetrical, though.
- adding a complementary circuit allows to overcome this limitation.




- **sequenced reset can improve immunity to reset-related transients** (if any - e.g. by excessive leakage > $I_{krum}$/2 in unsupported direction)
- successive reset of long time-constant shaper amplfiers without transients is non-trivial

## References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