

ADC based DAQ Status

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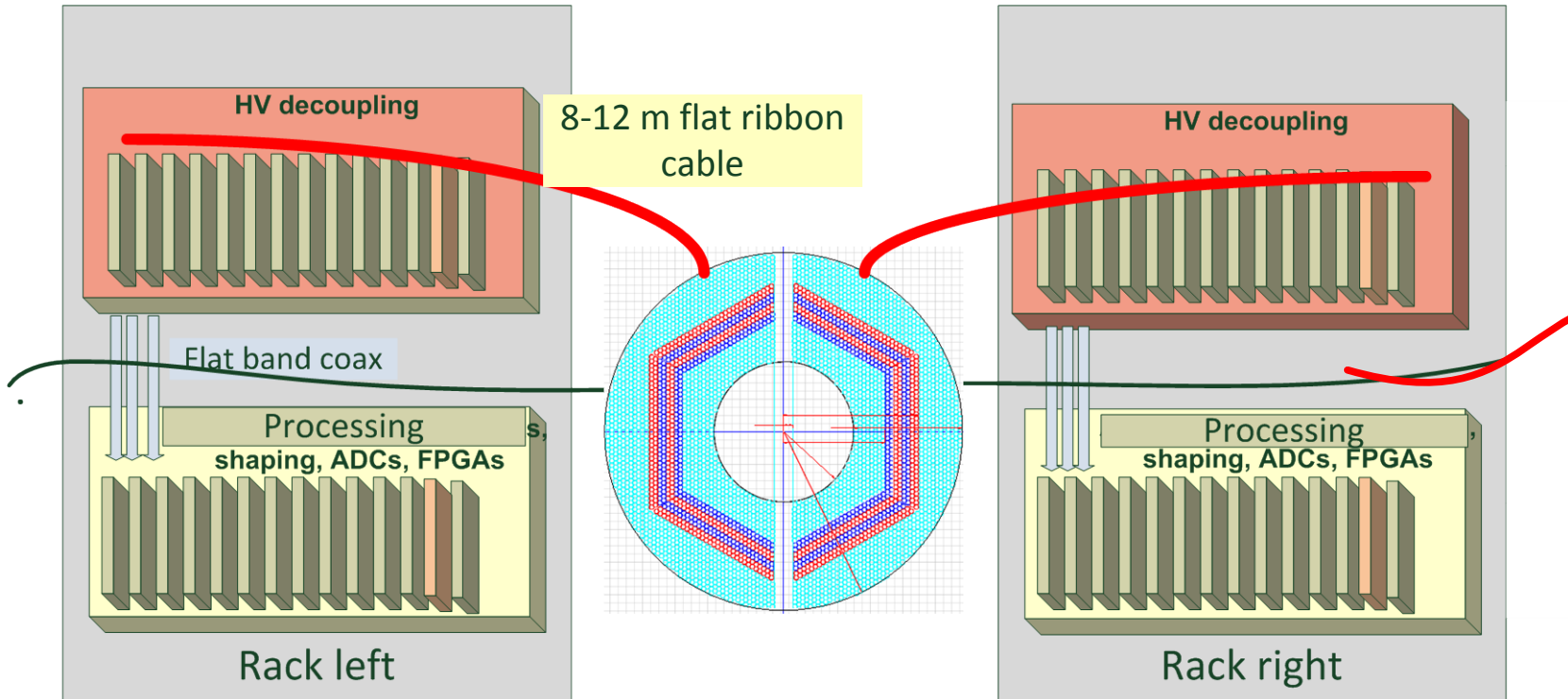
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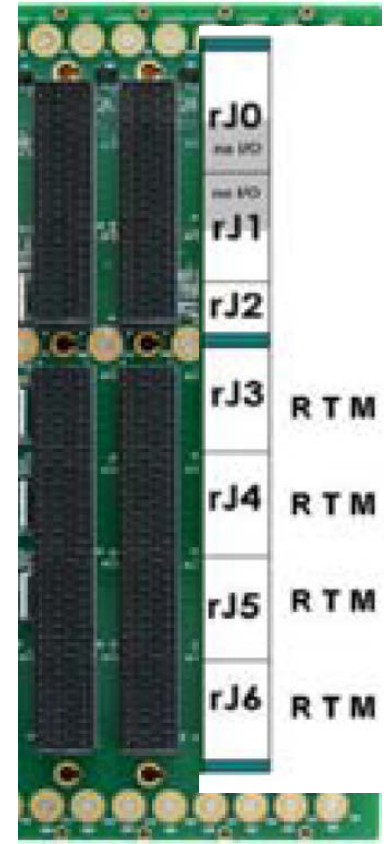
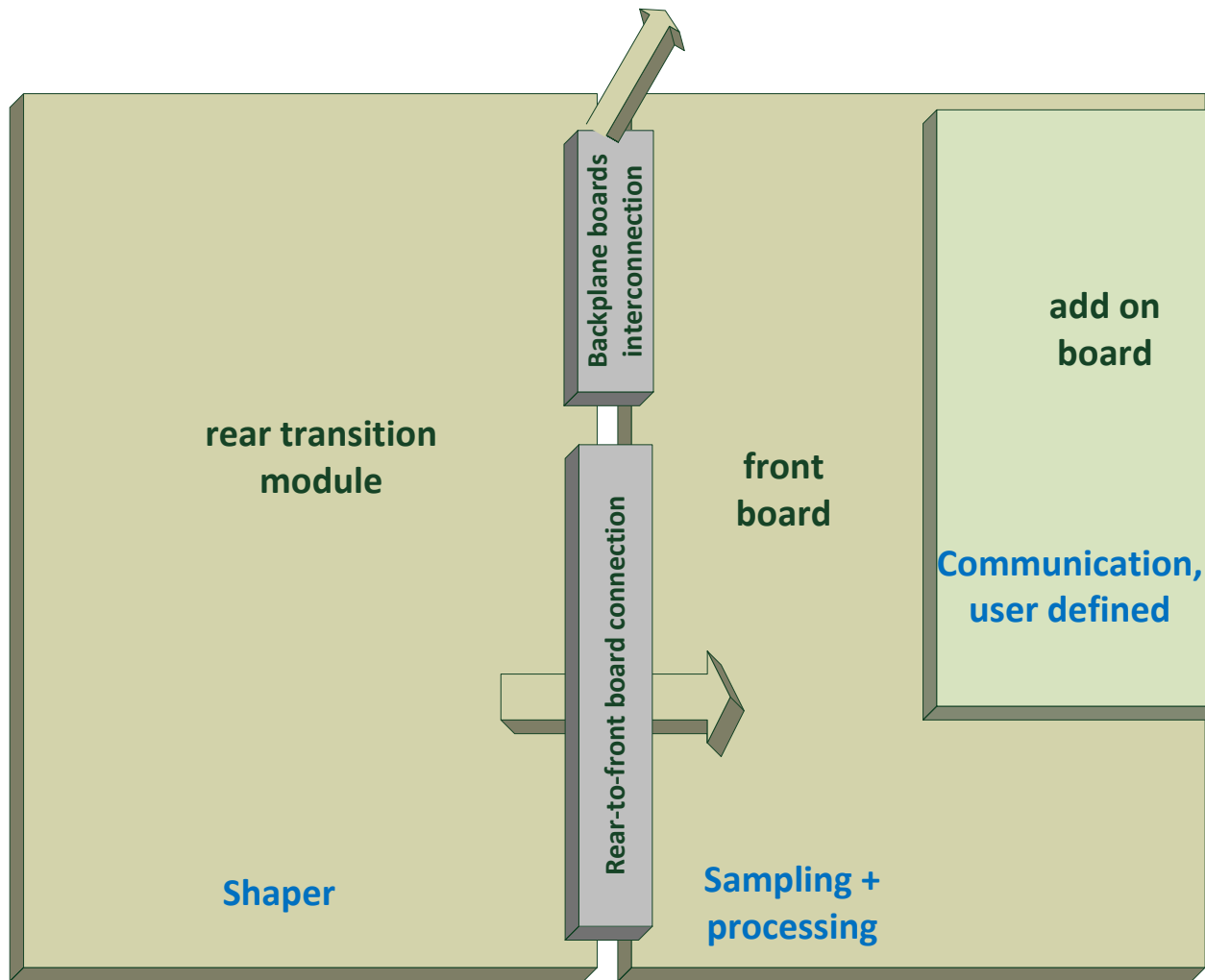
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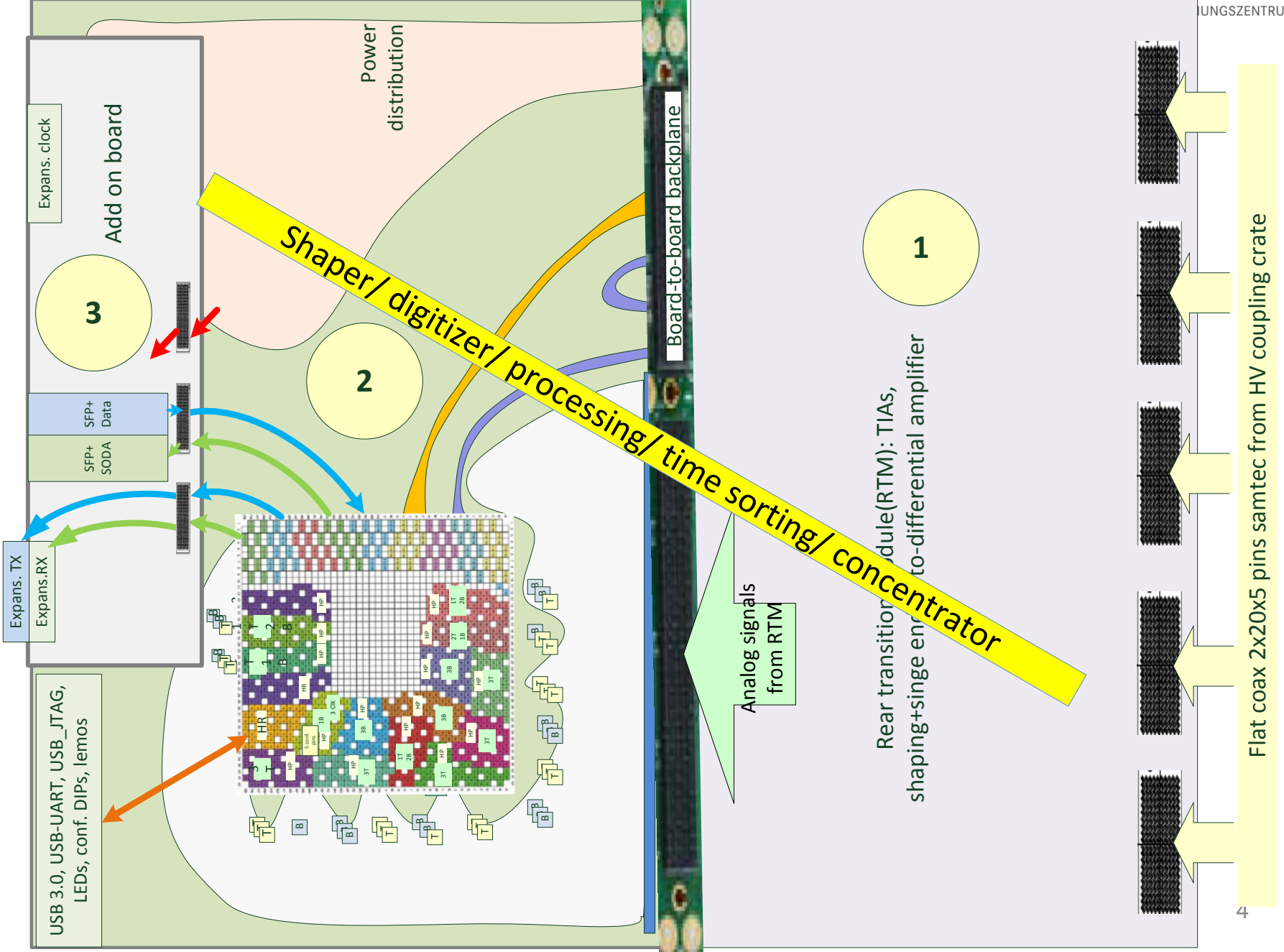
System overview



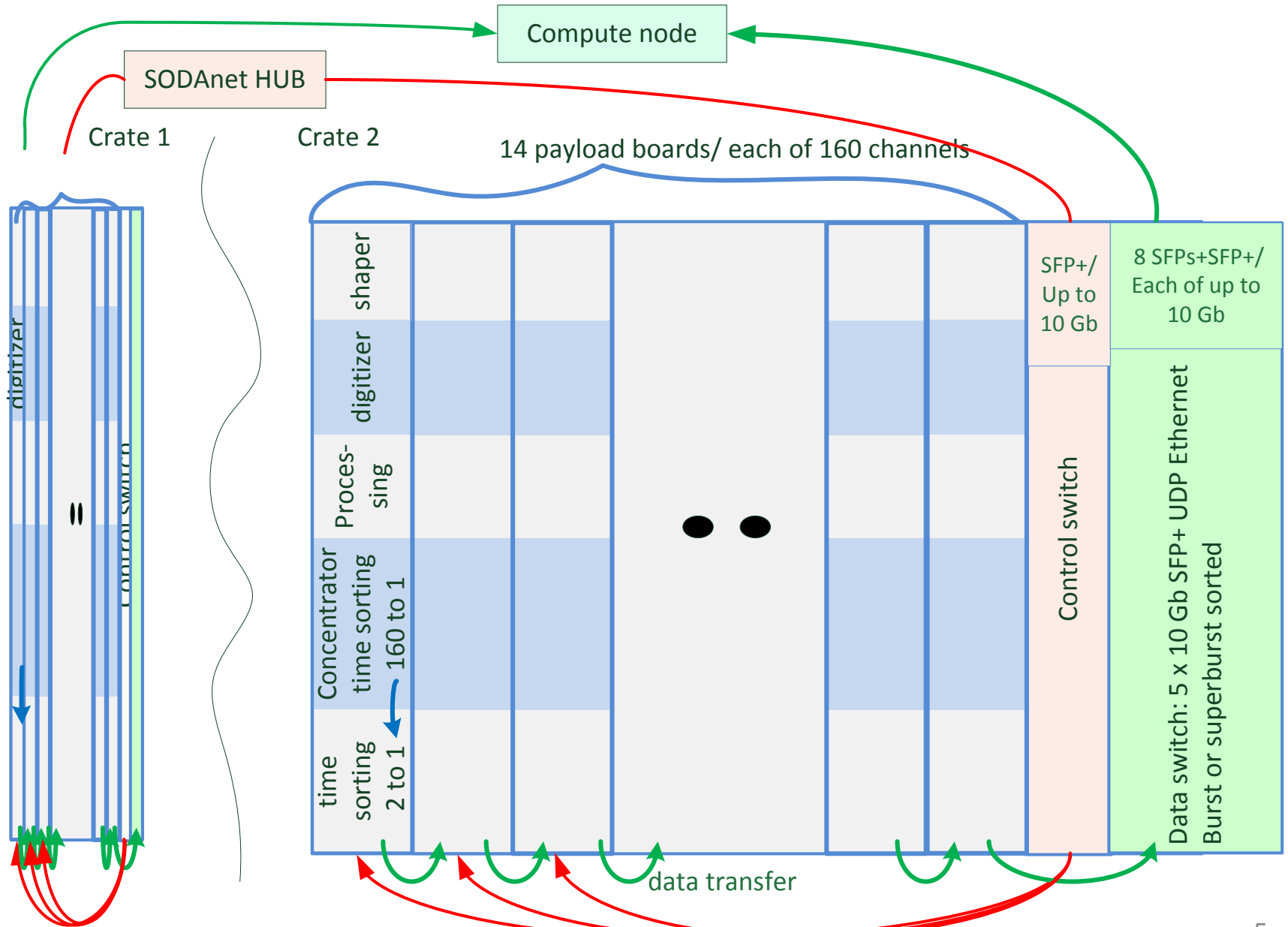
16-Slot open VPX crate



Boards Overview



STT DAQ structure



Time synchronization by SODAnet 1

We need only two SODAnet channels (one per DAQ crate)

Link to SODAnet source:

- XC7V585T(36 GTX)→ GTX up to 10 Gb and SFP+ (compatible to Kintex GTX on TRB board); 4.8 Gb transfer is foreseen for SODA

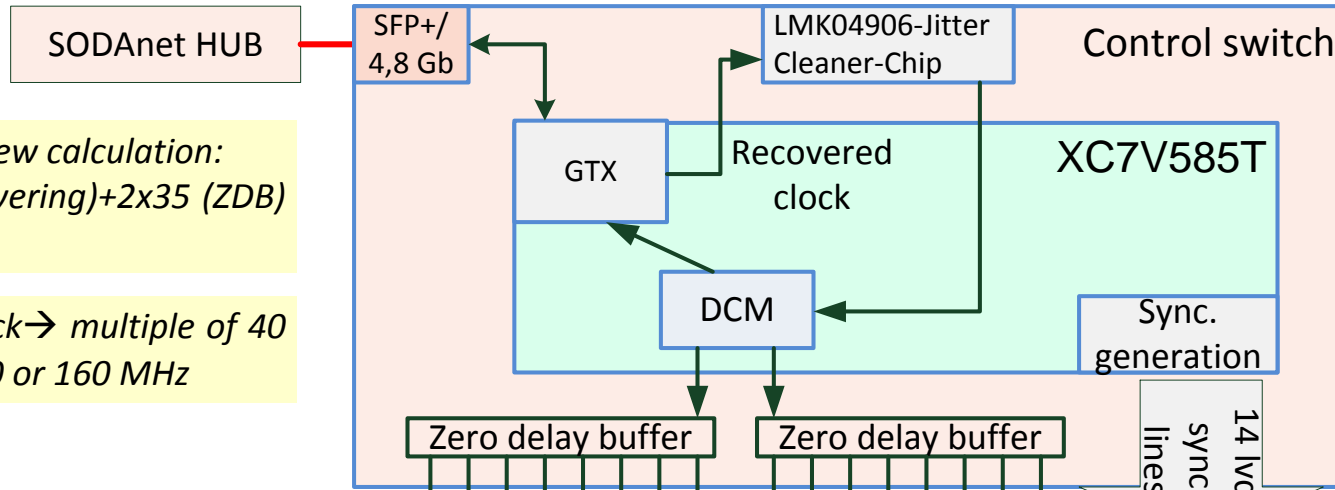
Number of links to readout boards: 0, inside the payload board

Number of links to data switch inside the same crate via backplane : up to 28 (2 x 14) of 10 Gb,
the total BW from payload boards to data switch: 280 Gbs

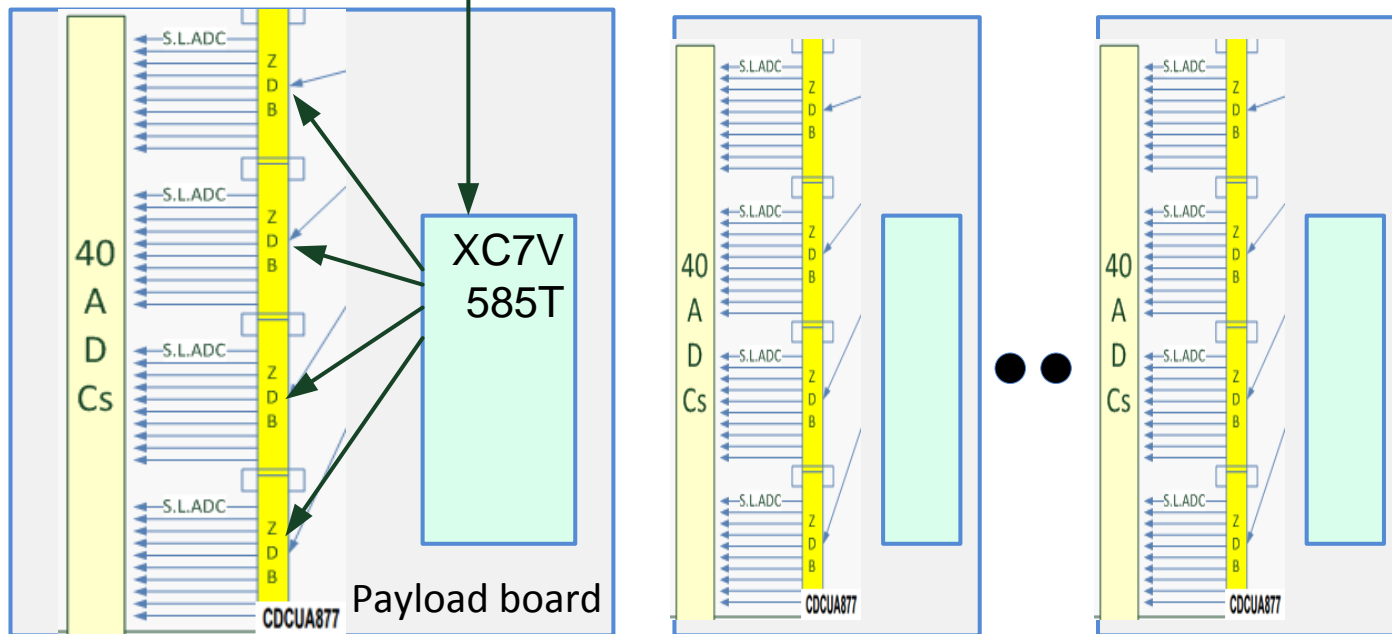
Timing with SODAnet

1. clock skew calculation:
 $70 \text{ ps}(\text{recovering}) + 2 \times 35 \text{ (ZDB)}$
 $< 145 \text{ ps}$

2. ADC clock \rightarrow multiple of 40 MHz \rightarrow 120 or 160 MHz



14 payload ADCs I/Os clocks, same length



Readout boards & data concentrator

- Channels number per board: 160
- Board per crate: 14 payload, 1 data switch + 1 control switch
- Boards for 2 crates x 2112 channels: $16 \times 2 = 32$ boards

Readout boards & data concentrator: payload board

- Data word size from payload board to data switch

Payload to data switch			
Straw number	time	energy	reserve
12 bits	14 (9+5)	9	5
5 bytes			
BW required: $160 \times 0,7 \text{MHit} \times 40 \text{ bits} = 4,5 \text{Gbps}$			
BW available: 8-20 Gbps			

- Buffer time $\rightarrow 2\mu\text{s}$;
- Required buffer size $\rightarrow 9 \text{ Kb} (2 \times 4,5) \rightarrow 1,1 \text{ KB}$ board allows $\sim 2,5$
- Max. hit number per time window $\rightarrow 225$ board allows ~ 500
- Max. hit number per second $\rightarrow 160 \times 0,7 = 102 \text{ MHit}$ board allows ~ 200

2 x

Crate					
Burst size	Links number	Type of link	Data throughput per link	Required BW	Avail. BW
16 KB (1,1x14)	8/16	SFP+, Ethernet, UDP	10 Gbps	63 Gbps	80/160 Gbps

Connection to compute nodes: data format

UDP packets size <62 KB				
Super burst number / bytes	Data size / bytes	Packet /burst nmb.	last-pack. flag	Payload data
4	2	15 bits	1 bit	16 KB
		2 bytes		

Straw number	time	energy	reserve
12 bits	14	9	5

5 bytes

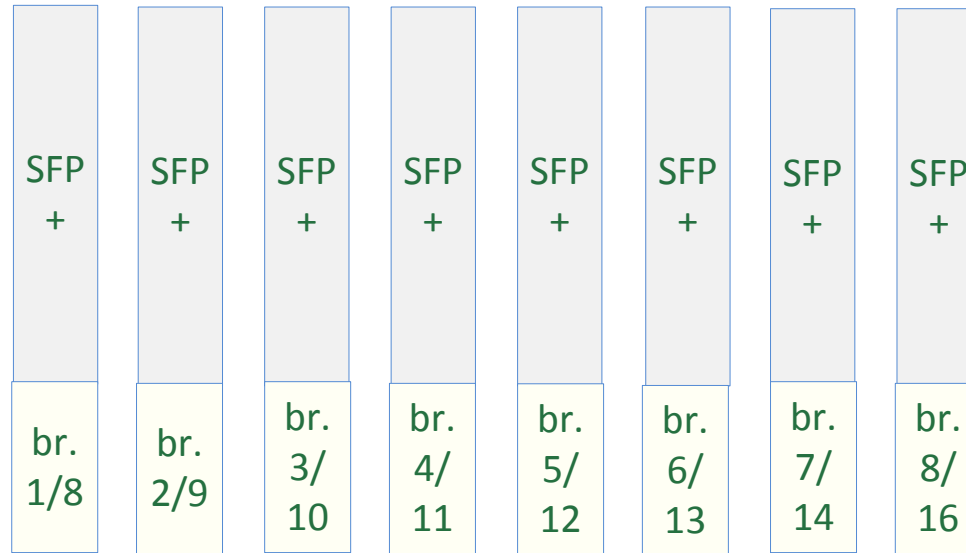
Straw number	time	energy	reserve
12 bits	14	9	5

5 bytes

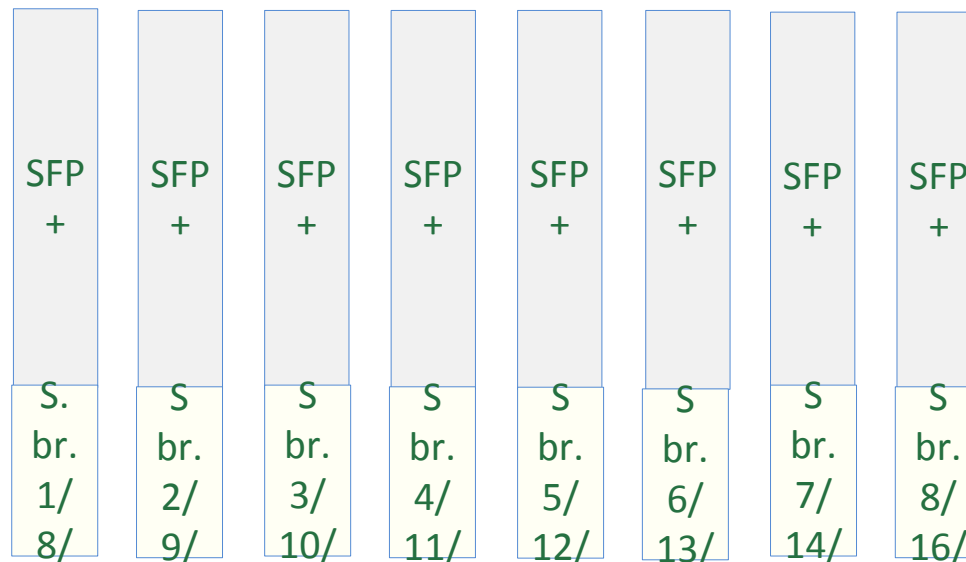
12	14	9	5

5 bytes

Burst or super burst to SFP links distribution



or



Power consumption per channel, mW

HV coupling (front end)	shaper	ADC	FPGA-proc.	Links to compute node
~ 5	115	110	100	25

355 mW

+LDOs in shaper, ADCs and MGTs $\rightarrow 0,15 \times 250 = 40$ mW

Total channel power cons. up to compute node **400 mW**

Safety factor for crate/board power supply 1,7

Backup

2.7 Test beam results 28.03.2016

1 GeV/c, Ar- CO₂ 80/20, 1800 V

