Minutes of the STT Readout Meeting (ezuce) on July-11th, 2017

Participants: Tassos Belias, Piotr Salabura, Greg Korcyl, Marcin Kajetanowicz, Marek Idzik, Krzysztof Pysz, Pawel Kulessa, Johan Messchendorp, Peter Wintz, Ljuba Jokhovets

Meeting web page with program and presentation slides: https://indico.gsi.de/conferenceDisplay.py?confId=6252

At first Peter reported about the CBAC meeting end of June in Julich for the COSY beam time requests. For the STT the request of 1 week proton and 1 week deuteron beamtime was fully approved and recommended by the advisory committee. The allocated beamtime is a 2-weeks block from 12/03/ till 26/03/2017. We might get first beam already in the MD (=machine development) week before. 1-2 days will be needed without beam to switch from the proton to deuteron beam source. This beamtime will be dedicated to pre-series tests of both readout systems.

Then a sketch of the cable routing scheme of the STT system at the PANDA target spectrometer (TS) was discussed. The STT system will be split into two independent half-barrels (2112 channels each) including cabling and supplies up to the two racks in front of the TS, one rack to the left and one rack to the right on the TS moveable platform. As Tassos remarked, the exact rack location (top or bottom) will be discussed and decided within the Mechanics Integration Group. The STT-preferred location is the top rack on each side yielding shortest cabling lengths of about 7-8 m. The proposed scheme avoids patch panels in front of the TS opening and minimizes the interference with the other detector systems.

Main topic of the meeting was the detailed system hardware architecture of the two readout systems and presentations were given by Greg for the ASIC/TRB and Ljuba for the ADC-based readout system (slides on the meeting web page). The explicit links to the SODAnet (time synchronization) and links to the compute nodes (event building) were included in both layouts. For both systems the readout is split into 2 readout crates, one crate for each STT half-barrel.

Data rates in the configurations were considered for the PANDA full nominal luminosity case (2×10^{32} $cm^{-2}s^{-1}$). As mentioned in earlier meetings the existing TRB3 HW will be sufficient for the phase-1 experiments, but the TRB3 (BW limit by GbE) will need a HW upgrade for the full luminosity case. Activities in this direction have already started within the GSI/FAIR community. The presented ADC-based solution is designed for the full luminosity case and includes about a factor of 2 safety margin for buffers and bandwidths. The new HW for the ADC system is planned to be ready by September. Four readout boards (160 ch each) will be produced for the pre-series setup.

The power consumption of the front-end ASIC boards in the current design is about 45 mW per channel (ASIC/LVDS ~ 35mV, rest voltage supply part) which results in 200 Watt for the STT. Realistic numbers and temperature effects should be measured with a system setup. The voltage regulation on each board was identified by Marek and Marcin as a possible source for a further power reduction. The use of a lower input supply voltage will be investigated in Krakow.

A longer discussion started about the need of time sorted hits at the stage of the readout boards or whether that should be done at the compute nodes where the event building and event hit association occurs. One has to disentangle time sorted hits from event associated hits due to possible time overlapping of hits from different events. Ljuba pointed out that the ADC-RO system and HW of each readout board (160 ch) features a time sorting of the hits as part of the data concentrator. In the current TRB3 system layout this task is not foreseen, but rather seen as a task for the event processing in the compute nodes. Nevertheless, Greg showed that if this task is needed, additional HW (even commercial HW, remark by Marcin) can be added to the system layout.

It was concluded that the requirements for a hit sorting should be clarified together with the PANDA-DAQ group and consequences to be discussed during the next meeting. No other open point in the system layouts was seen or addressed during this meeting. The next meeting is foreseen for end of August and the date will be fixed soon.

Further remarks received after the meeting:

Greg, on the dating sorting issue: the TRB could be internally triggered for each burst and data transmission triggered by a superburst (=16x bursts) signal. Then the data is naturally sorted on a burst per burst basis. Issue is strongly connected to the data processing algorithm after the burst-building. This algorithm [or event building scheme] is not existing at the moment and therefore hard to say what data order is better [or needed] in the end.

Ljuba, on time sorting in the ADC-based system: Each of the [14] payload boards [(160ch each)] transmits through the backplane time sorted data to the data switch [one per crate], where the final sorting of 14 payload data streams to one occurs, then a burst- or super-burst ordering and data distribution to the compute nodes. The crate provides a fully time sorted data stream.