Development of the CBM RICH readout and DAQ

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for the CBM-RICH collaboration

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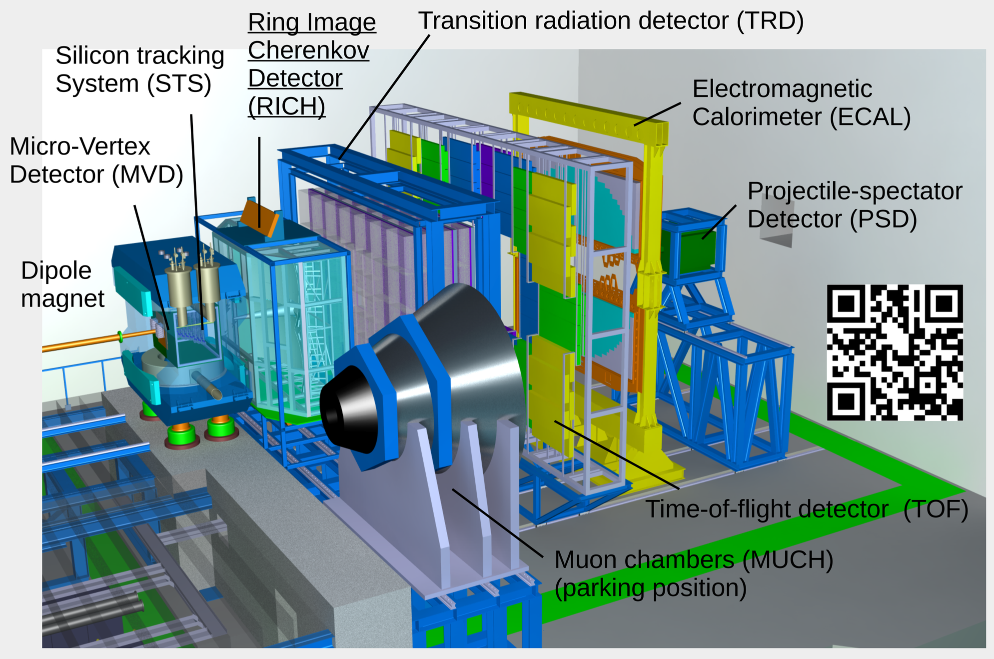
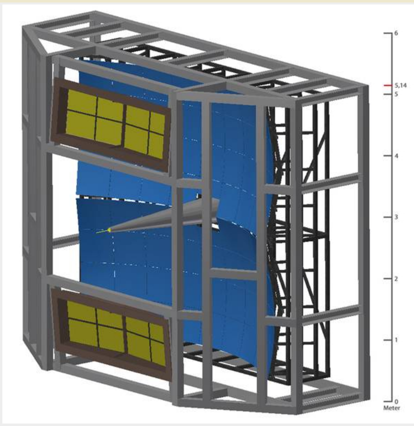
Introduction

The CBM experiment at the future FAIR facility (Darmstadt, Germany) will investigate strongly interacting matter at high net-baryon densities but moderate temperatures in heavy-ion collisions. Electromagnetic decays in the fireball are among the most sensitive probes for the created matter. The SIS 100 synchrotron will deliver ion beams from proton to uranium with energies of up to 11 AGeV for the heaviest nuclei. Beam interactions of up to 10^9 per second will provide nuclear interaction rates up to 10^7 per second for a fixed target experiment.





Such a high interaction rate is necessary for accessing rare probes. As a consequence of the high interaction rate, triggerless readout and full event reconstruction "on the fly" are foreseen.

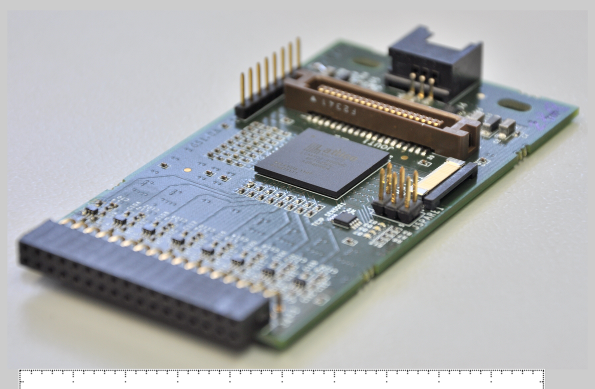
CBM RICH Tech. Design Report:

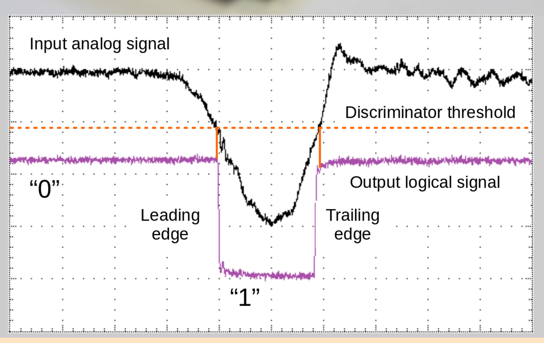
The CBM RICH detector is required for identifying di-electrons in a momentum range up to 8 GeV/c. It is a classical RICH detector with gaseous radiator, spherical mirrors and segmented photosensitive camera made of ~1000 Hamamatsu H12700 multi-anode photomultiplier tubes. The MAPMTs will be read out by self-triggered FPGA-based frond end boards detecting only time information.

Readout channel

PADIWA

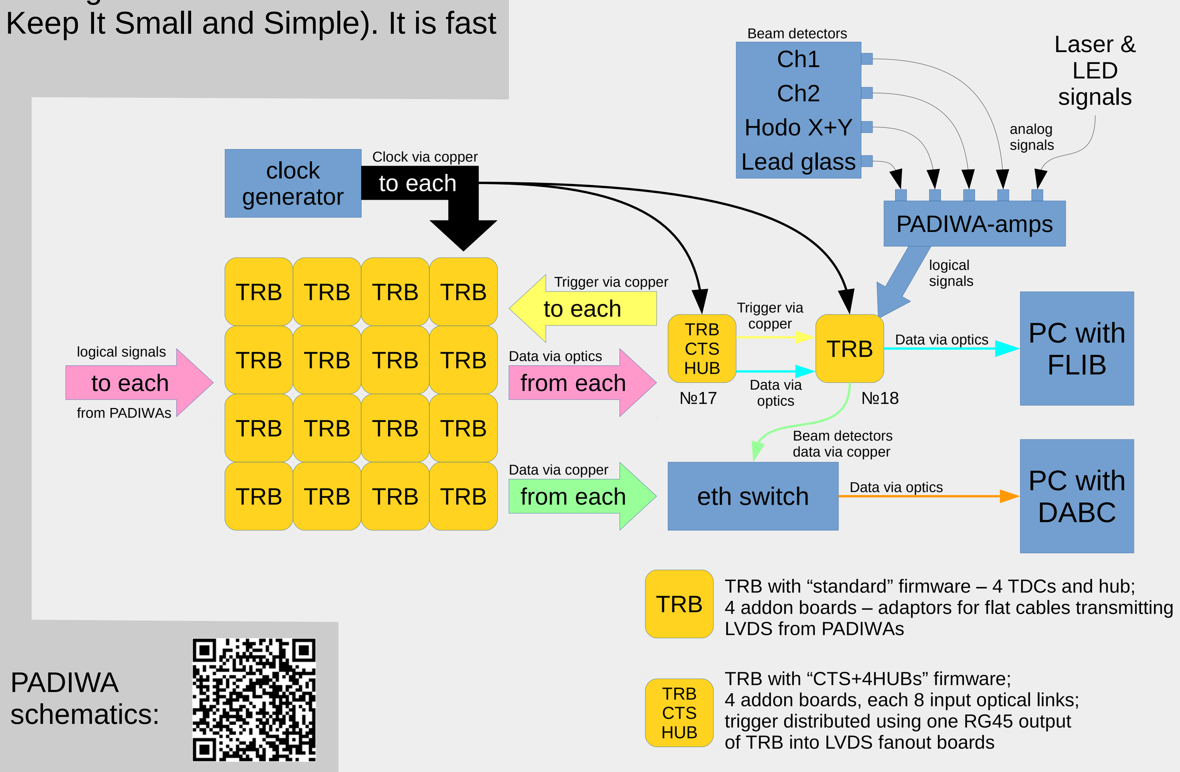
PADIWA is a 16 channel front end board which realises a preamplifier and a discriminator, the latter inide an FPGA. Its design follows the COME&KISS principle (COmplex comMErcial Elements & Keep It Small and Simple). It is fast and it has small dead time.



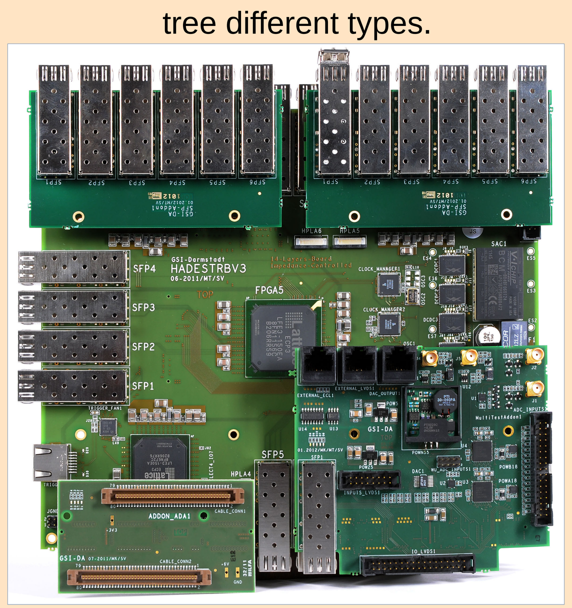


PADIWA schematics:

CBM RICH prototype readout & DAQ scheme

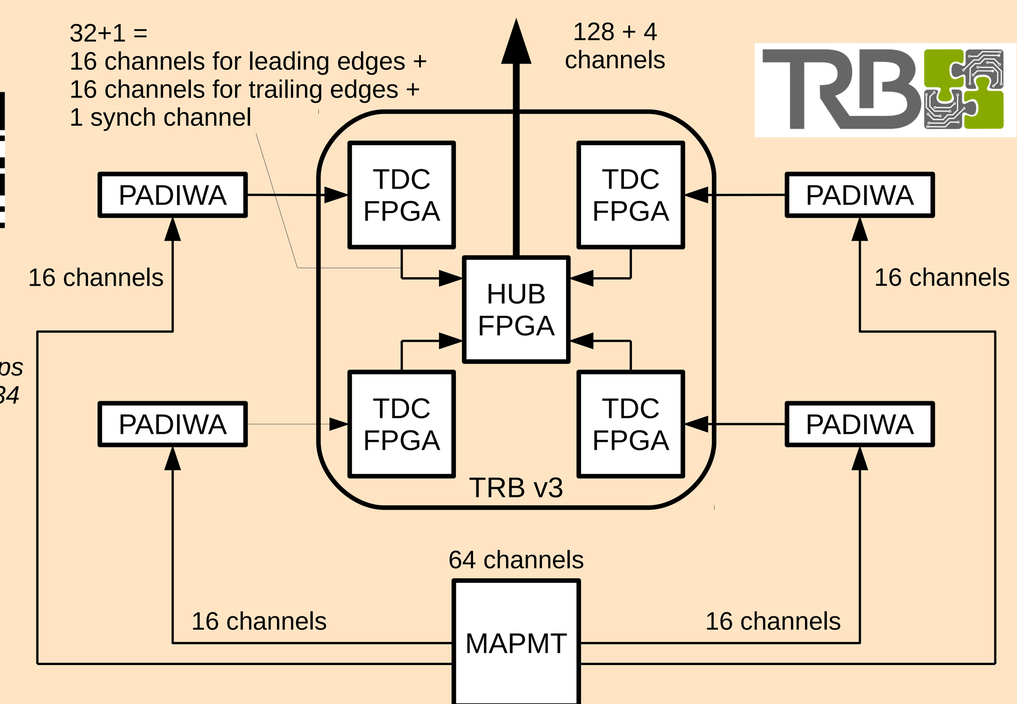


TRB v3



TRB v3 with addon boards of tree different types.

TRB v3 is a multifunctional board which has 5 FPGAs. The main TRB configuration used in CBM RICH has 4 peripheral FPGAs programmed as TDCs and 1 central FPGA programmed as HUB. The TRB board can be extended with a number of different addon boards. 4 PADIWAs and 1 TRB v3 are required to read out one 64-pixel MAPMT. Leading and trailing edges of one PADIWA channel are split at the first stage of the TDC in order to measure leading and trailing edges of the discriminated signal using two TDC channels, and thus allowing the measurement of time-over-threshold.



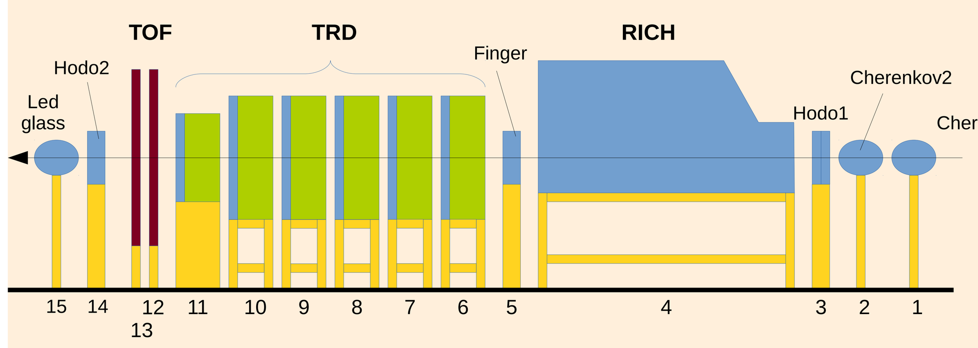
C. Ugur, G. Korcyl, J. Michel, M. Penschuk and M. Traxler, "264 Channel TDC Platform Applying 65 Channel High Precision (7.2 ps RMS) FPGA Based TDCs", doi: 10.1109/NoMeTDC.2013.6658234

First Level Event Selection Interface Board (FLIB)

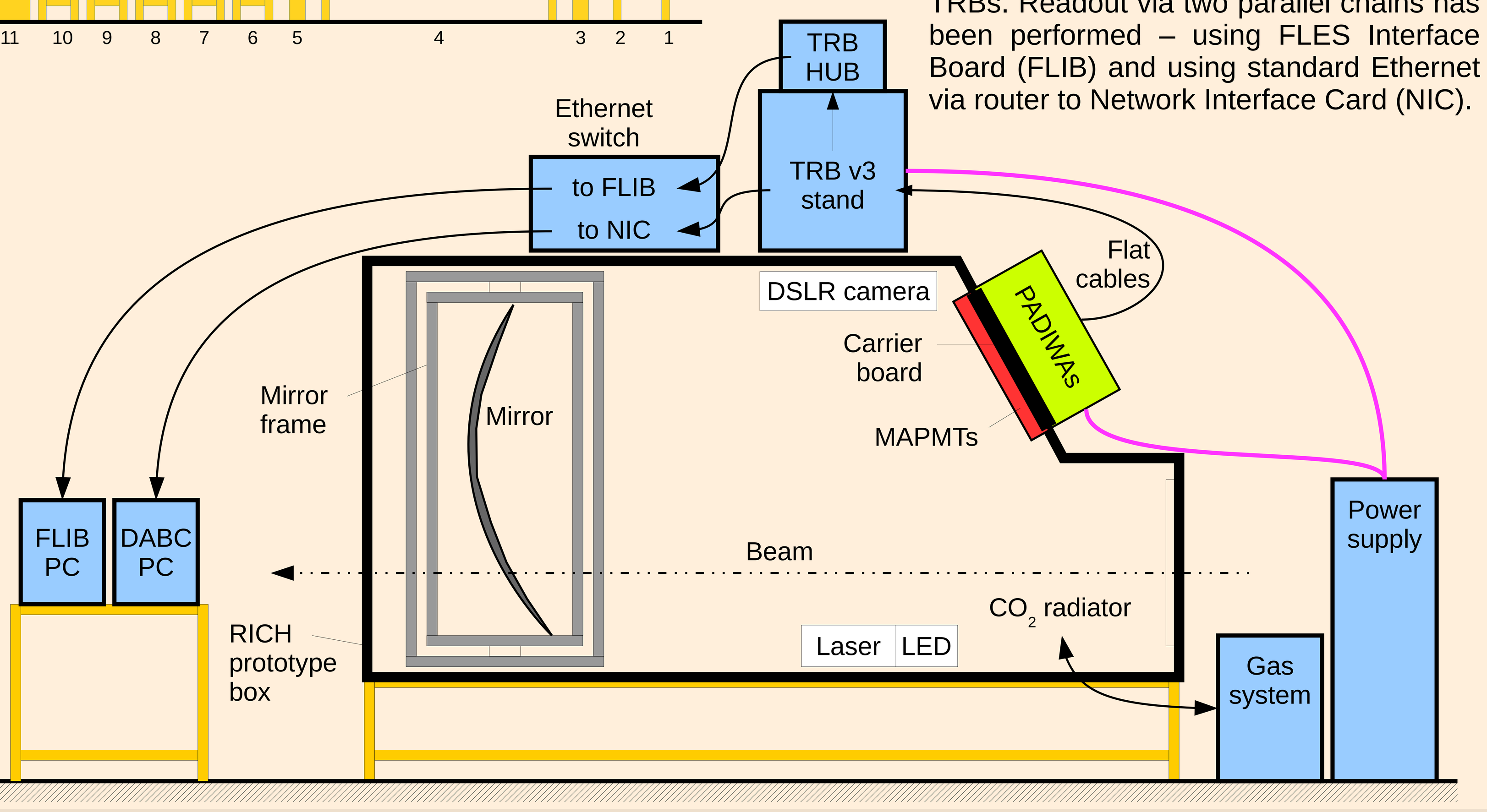
CBM FLES Interface board is required to serve as an interface between the custom FPGA-based electronics and the PC. For the first time a commercially available PCI-E board HTG-K7 as FLIB has been successfully tested with several detectors in the beam conditions.

Experimental setups

Beamtime setup

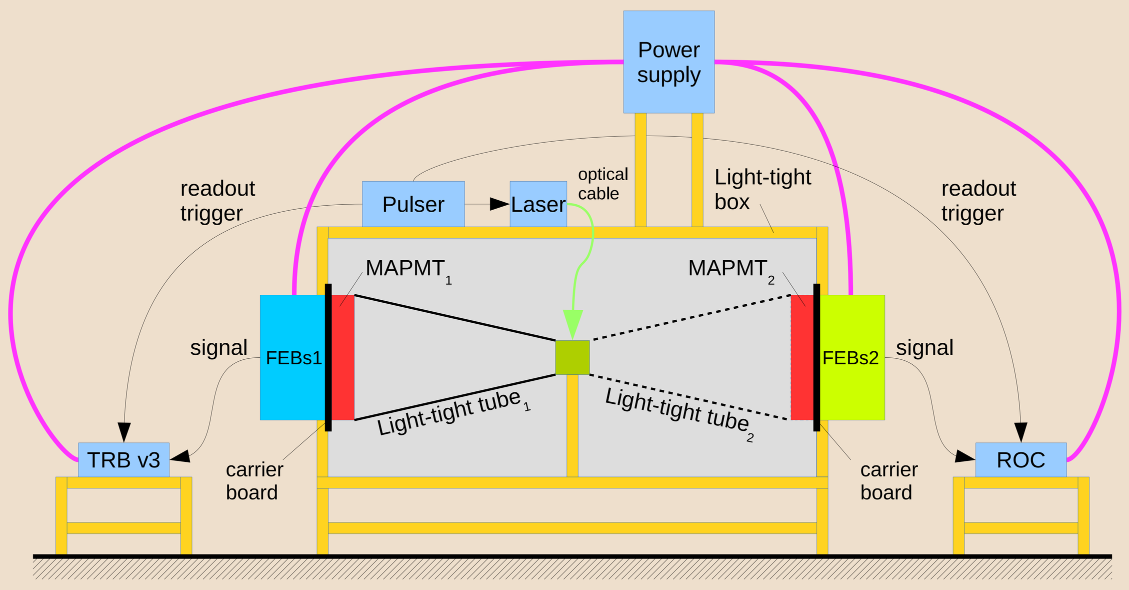


During our Nov 2014 CERN-PS beamtime a CBM RICH prototype including a camera of 16 MAPMTs partially coated with p-terphenyl as WLS coating has been succefully tested. The MAPMTs were read out by 64 PADIWAs and 64 TDCs on 16 TRBs. Readout via two parallel chains has been performed – using FPGA Interface Board (FLIB) and using standard Ethernet via router to Network Interface Card (NIC).



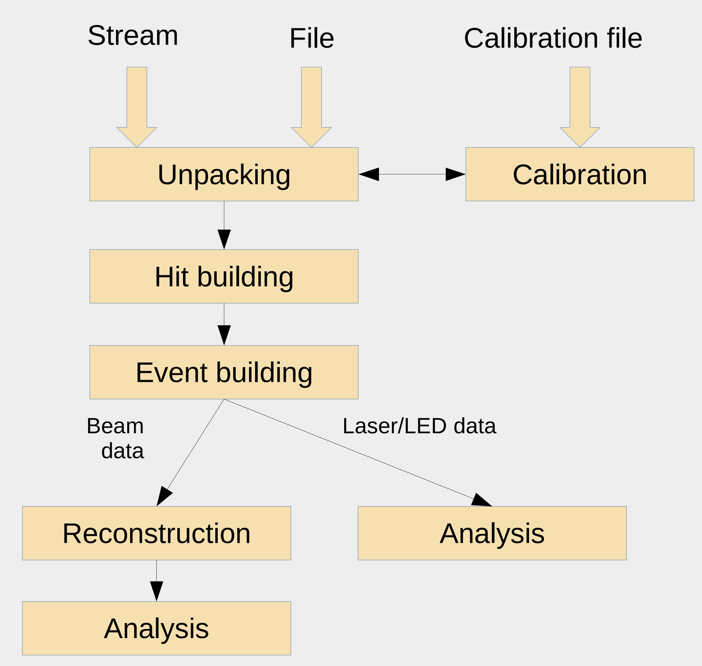
Laboratory setup

In order to study the CBM RICH readout & DAQ system and its separate components a dedicated laboratory stand has been built. The main parts of the setup are the picosecond laser illuminating the H12700 MAPMT read out by one of two readout chains. The first chain is based on nXYTER and SysCore ROC and measurements using this electronics are used as the reference measurements. The second chain is the studied one and it consists of the minimal number of components required to read out 1 MAPMT – 4 PADIWAs and 1 TRB v3.



Software

CBM RICH beamtime and lab data analysis

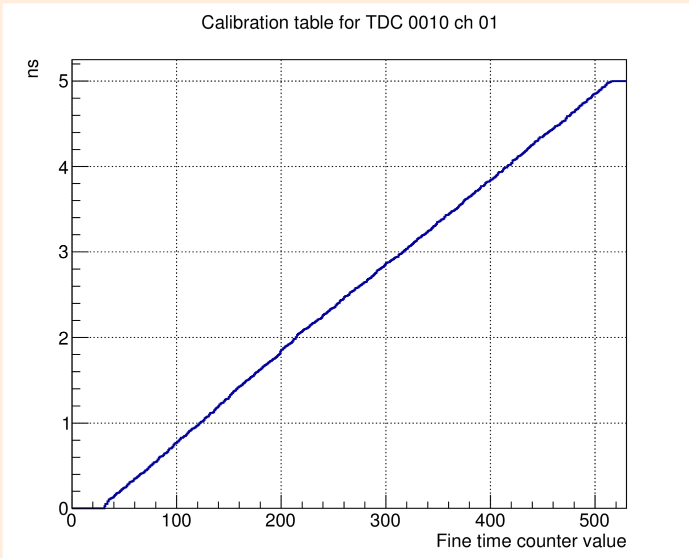


CbmRoot, FairRoot

All presented results have been obtained using the code, developed in the frame of CbmRoot. It is based on FairRoot which is in turn based on ROOT.

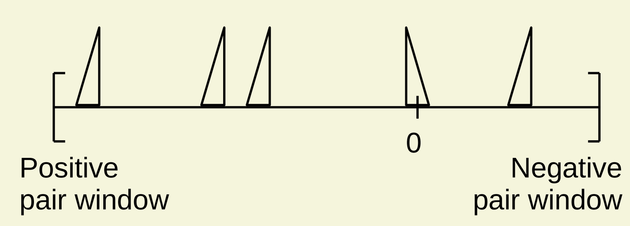
Calibration

Fine time counter is implemented in TDC using tapped delay line technology. There is a standard technique to calibrate such counters which is based on the fact that the distribution of time stamps from a source uncorrelated with the FPGA itself has to be homogeneous. Derivations from this homogeneity stem from varying bin sizes of the TDC and can thus be corrected. As result of analysis of some portion of data a look-up table is built for each channel which gives the correspondence between the fine time counter value and time in nanoseconds.
An example of such a table is shown below.



Hit building – edge matching

The TDC FPGA firmware used during the beam tests had the following feature: analog pulses processed by 1 PADIWA channel were split into two channels before timestamp detection. As result the procedure of software hit reconstruction or "edge matching" was required. For every trailing edge the corresponding leading edge has to be found in the buffer of leading edges.



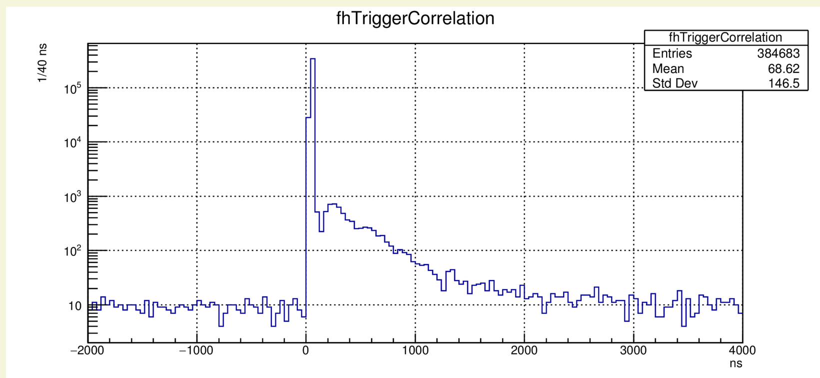
Event building

As the electronics is self-triggered and data acquisition is in free-running mode, input data comes in portions which have nothing common with real events though we call them DAQ-events. A procedure of event building is required in order to provide correct information to reconstruction algorithms and further analysis.

Analysis results

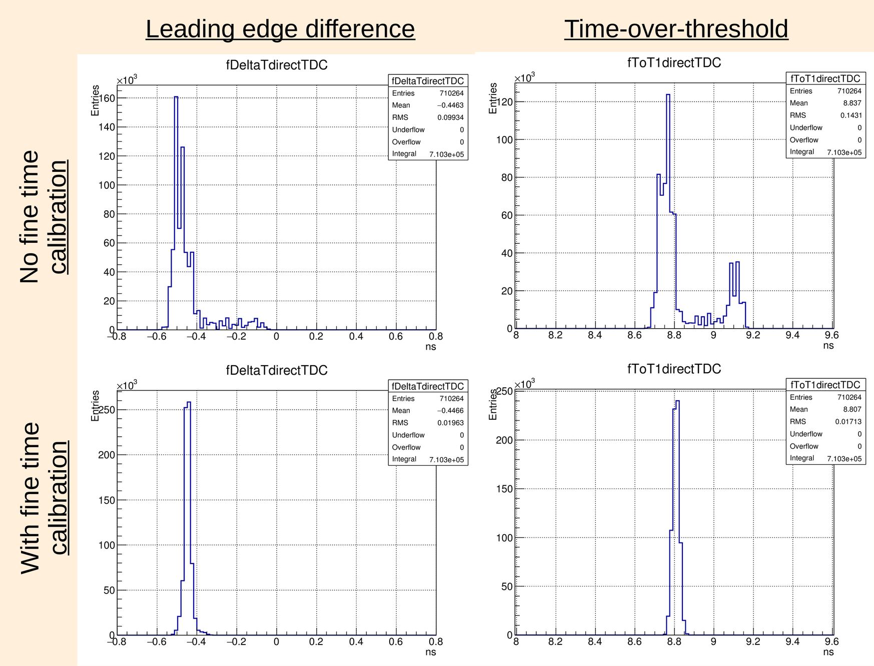
Simultaneous hits

In order to analyse the time characteristics of the readout chain and its components we use the fact that the hits of one laser flash (duration 10-20ps) come to the photosensitive camera simultaneously (given its time precision of ~300 ps TTS). The same is applicable to all the photons of a single Cherenkov ring.



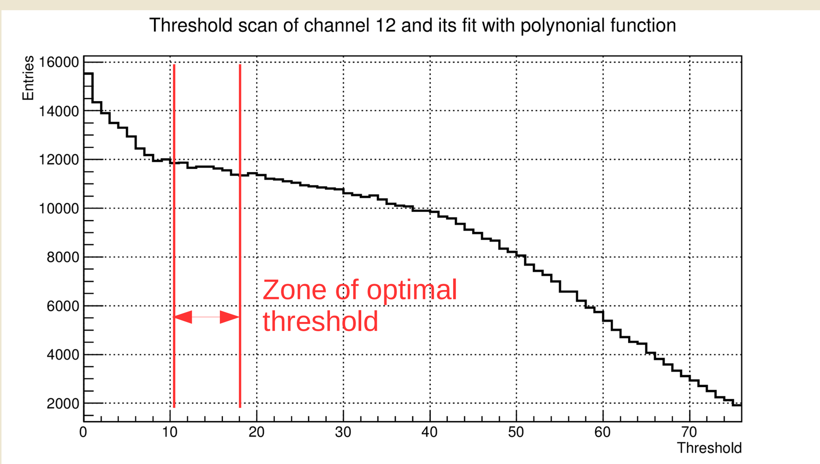
Time resolution of time-to-digital convertors

For measurements of time resolution of TDCs, a 10ns-wide pulse from a high-precision pulse generator was split into two and sent to different pairs of input channels using identical cables. Examples of the distribution of the difference between the two registered timestamps $\Delta t_i = t_i - t_j$ which were sent directly to TDC simultaneously and measured pulse width are shown below before and after applying fine time calibration.



Threshold scan

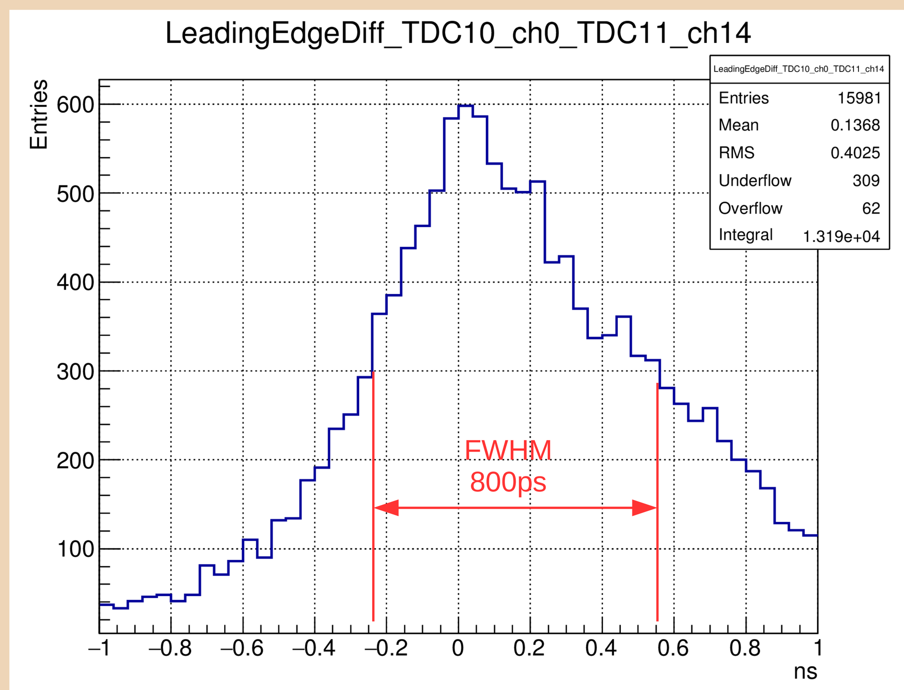
Readout of MAPMTs detecting single photons always requires tuning of front end electronics threshold. It has been proven that analysis of the dependency of data rate vs. threshold can be used to find the optimal threhold.



Time resolution of the full readout chain

From the "leading edge difference" distribution we derive the time resolution of the full readout chain as $\frac{FWHM}{\sqrt{2}} = 566\,ps$

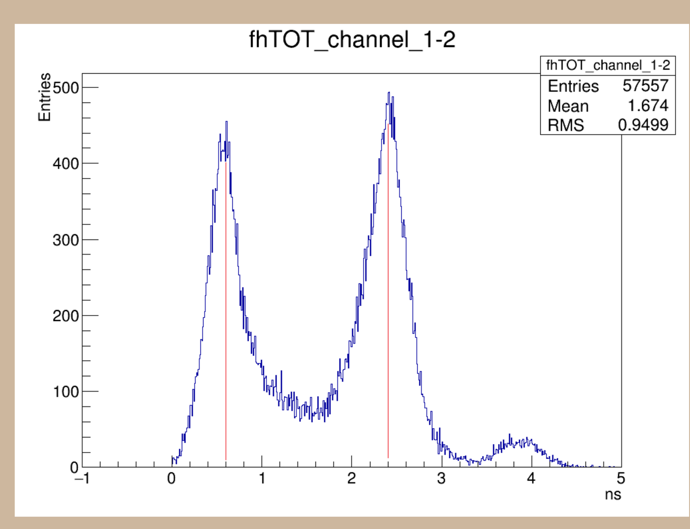
The theoretical limit is in order of 350 ps and it is dictated by the transition time spread of the multi-anode photomultiplier tube.

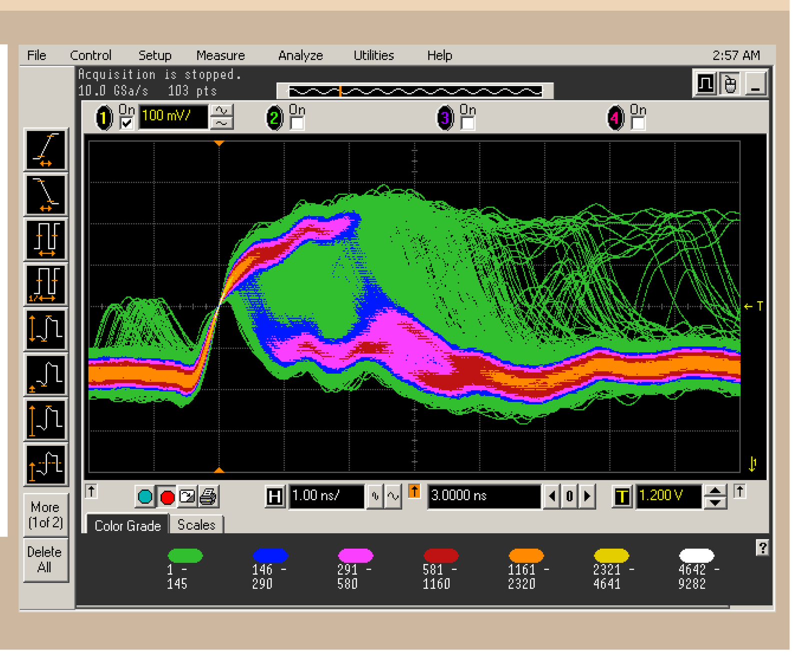


Multi-peak time-over-threshold

Preliminary analysis of the data received during the beam tests showed unexpected distributions of time-over-threshold values for individual channels. The setup in the lab has been built and measurements using a fast scope has been performed showing that the peaks appear due to wrong shape of the TDC input signal.

Such situation can be caused by the presence of periodical noise. It is well described in the following paper:





F. Gonnella, V. Kozhuharov and M. Raggi. "Time over threshold in the presence of noise", doi:10.1016/j.nima.2015.04.028