Design and Evaluation of an FPGA Online Feature Extraction Data Pre-Processing Stage For The CBM-TRD Experiment

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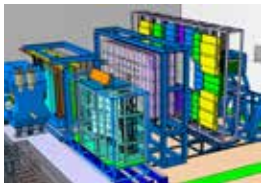
The Compressed Baryonic Matter (CBM) Experiment

- Explore the QCD phase diagram in the region of high baryon densities using high-energy nucleus-nucleus collisions
- Located at the International Facility for Antiproton and Ion Research (FAIR), Darmstadt, Germany
- A data rate of about 1 TB/s and an event rate of approximately 10 MHz is expected for the final experiment
- Self-triggered and time-stamped



CBM setup for the SIS100

The Transition Radiation Detector (TRD)

SIS100 configuration
- Provides identification of electrons
- High interaction rates
- Pion supression > 100

Front-End Electronics

- Readout of cathode pads with the Self-Triggered Pulse Amplification and Digitization ASIC (SPADIC)
- Charge-sensitive amplifier with 32 channels
- Free-streaming
- Forced neighbour readout

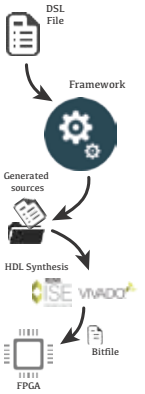
The Feature Extraction Framework - Overview

Overview
- An HDL design is described in a Domain Specific Language (DSL)
- No HDL coding is needed
- Reuse of existing HDL designs
- Integration into Xilinx synthesis tools (ISE and Vivado)

Data Stream Handling
- Automatic insertion of decoding logic for meta-data and payload words
- Protocol independent processing
  - Different front-end message formats
  - Framework can be used for different HEP experiments
- Standarized core interface for data streaming: AXI4-Streamer
  - Stream-message format is described inside the DSL file

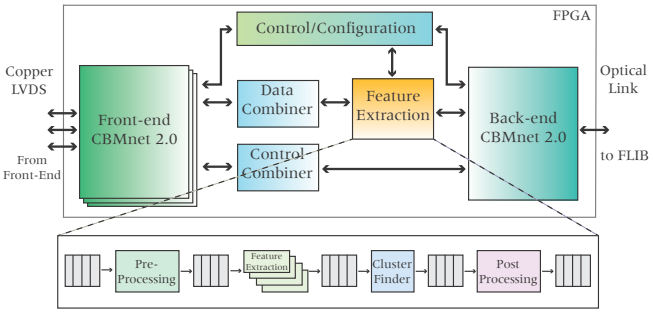
System Manager
- Clock managers, FIFOs and IOs are automatically managed

Project Generation
- A synthetizable design project is created for a given DSL file
- Automatically generated code written in VHDL



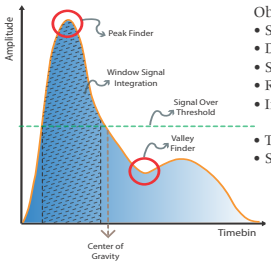
Experimental Design

- Developed and tested on a SysCore3 Spartan-6 FPGA board
- Optical CBMnet 2.0 modules running at 125 MHz
- Selection of feature extraction algorithms done at compilation time
- CBMnet 2.0 transport link
  - Special Deterministic Latency Messages (DLM) for time synchronization
- Configuration for system and feature extraction cores via control messages



- Preprocessing:
  - Overflow detection, pedestal reduction, baseline correction
- Feature extraction cores can be easily duplicated according to desing constraints
  - Data troughput or resource consumption
- Different discriminators can be used for the cluster finder algorithm
- Post processing algorithms can be applied on found clusters
  - Reduction algorithms such as center of gravity and integrators

Feature Extraction Concept



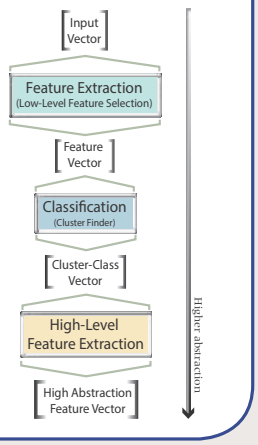
Objectives:
- Selection of relevant set of features from an input vector
- Dimension reduction
- Savings in memory and time consuption
- Representation of an object in a compact feature vector
- Informative and non-redundant

- TRD time-based signals provide multiple features
- Suitable for offline and later reconstruction algorithms

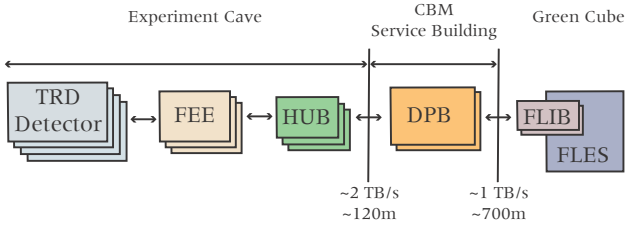
Feature Extraction
- Selection of best features for dimension reduction
- Retain their discriminatory information as much as possible

Classification
- Assigns a class to a feature vector
- Classification based on discriminators

High-level feature extraction (Post-Processing)
- Further reduction of members of a given class



CBM/TRD Readout Architecture



- TRD read-out by multiple Spadic 1.0 front-end boards
- Data Processing Board (DPB) implements
  - Read-out Controller (ROC)
  - Feature extraction processing algorithms
  - Data sorting and buffering
- Multiple input/output optical links

Outline and Future Work

Outline:

- Multiple feature extraction algorithms already available as HDL cores
- A Feature extraction framework has been used and tested for
  - Reutilization of HDL designs
  - Reconfiguration of HDL designs
  - Automatic stream-message handling and decoding
  - Generation of build and synthesis projects for new and already available HDL projects
- Experimental setup tested during CERN-SPS (2015) and CERN-PS (2014) beam test runs

Future Work:

- Firmware upgrades
  - Migration to Kintex-7 based AFCK board
    - New Data Processing Board platform for the CBM data acquisition chain
  - Data transmission link from CBMnet 2.0 to GBTx
  - Increased number of front-end electronics boards for the new DPB versions
  - Integration of Spadic 2.0

CBM

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