Quality Evaluation System for CBM-TOF Super Module

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Abstract. The Time-of-Flight (TOF) system in the Compressed Baryonic Matter (CBM) experiment is comprised with super module (SM) detectors, each of which contains serval Multi-gap Resistive Plate Chambers (MRPCs). For the purpose of quality evaluation of CBM-TOF SM, the readout electronic system is proposed in this paper. It consists of three kernel parts: front-end electronics (FEE), back-end electronics (BEE) and data acquisition (DAQ) software. There are 10 TDC boards with 20 ps time digitizing precision for 320-channel time digitizing and 1 TRM for reading out multiple TDC boards, serving as FEE. BEE are composed of 20 data readout modules (DRM) divided into four groups resided inside two PXI-6U crates and 1 CTM for clock and trigger distribution. DAQ software receives the data from DRM and distributes command to DRM through the Gigabit Ethernet port. Preliminary test results show that the evaluation system can be used for the quality control of CBM-TOF SM.

Keywords: CBM-TOF SM, readout electronic, Quality Evaluation.

1 Introduction

The Time-of-Flight (TOF) system in the Compressed Baryonic Matter (CBM) experiment is composed of 6 different type of super module (SM) detectors named M1 to M6, each of which contains several high resolution Multi-gap Resistive Plate Chambers (MRPCs). As for the M5 and M6, each SM contains 5 MRPCs, which supports up to 320 electronic channels for high-precise time measurement. In order to meet the minimal requirement of 80 ps global time resolution, the resolution of time to digital converter (TDC) board should be 25 ps or better [1][2][3].

For now, MRPC detectors for CBM-TOF are still under development. During the process of MRPC mass production, quality evaluation system is required to ensure that the detectors achieve the expected performance. For the purpose of quality evaluation of CBM-TOF SM, a 320-channel time digitizing and readout electronic system for high density and high resolution time measurement is designed.

2 System architecture

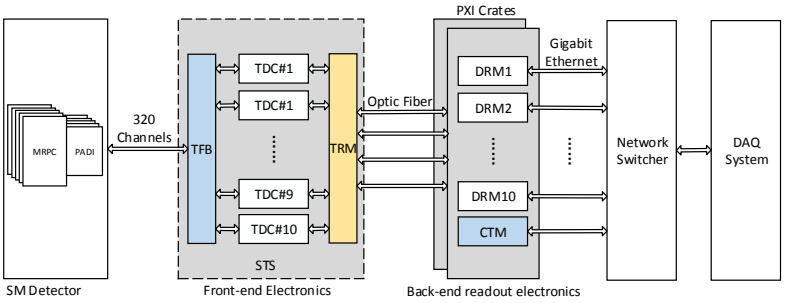

Fig. 1. Architecture of quality evaluation system

The quality evaluation system has a distributed architecture, as shown in **Fig. 1**, including SM detectors, front-end electronics (FEE), back-end electronics (BEE) and data acquisition (DAQ) software.

2.1 Front end electronics

SM TDC station (STS) is designed as an integrated and independent structure, closed to the SM detectors, serving as FEE. Each STS mainly contains 10 TDC boards for 320-channel time digitizing and 1 TDC Readout Motherboard (TRM) for reading out 10 TDC boards. 10 TDC boards are plugged into the TRM through golden fingers.

A prototype of high resolution and density FPGA TDC board is designed, which can support up to 32 electronic channels with a time resolution better than 20 ps and Time over Threshold (TOT) measurement [4][5]. Gigabit transceiver (GTP) is used to transmit the time measurement data to the TRM and to receive the command from TRM through golden finger connector. And the clock and trigger for TDC board are buffered in from TRM through the golden finger connector.

The main functions of the TRM are early data aggregation, control of the TDC boards, clock and trigger synchronization, and power supply. TRM has two Xilinx Kintex-7 series FPGA (XC7K70T-1FFG676), each of which aggregates time measurement data from 5 TDC boards concurrently and transmits the data to the back-end readout electronics with 2 optical uplinks with 2.5Gbps each. Two optical transceivers (SFP or SFP+) in TRM are used to receive high-precision synchronous clock and trigger from DRM through two optical downlink.

2.2 Back-end electronics

BEE act as the interface between FEE and DAQ software. BEE are capable of receiving data from STS through four optical uplink and delivering it to DAQ system via Ethernet port at the rate of 9Gbps. In addition, BEE should also be responsible for transferring the command to the FEE through one optical downlink and distributing the synchronous clock and trigger to the FEE through two optical downlink.

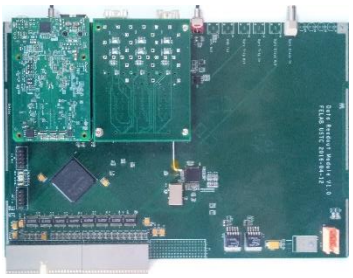

Fig. 2. Photograph of DRM

As shown in **Fig. 2**, a prototype of DRM is designed for data readout and clock and trigger distribution. DRM receives data from TRM through optical link and distributes the clock and trigger to TRM reversely. To deal with the massive data receiving from TRM through four optical link, 20 DRM divided into four groups resided inside two PXI-6U crates are introduced to the system. Among 5 DRMs from the same group, a master module receives data from TRM at the rate of the 2.5Gbps though one optical link and sends to all slave ones alone a daisy chain through differential cable, as shown in **Fig. 3**. As a result, each DRM needs to process the data at the rate of 0.5Gbps. Once data arrives at DRM, they are relayed to the DAQ system through a Gigabit Ethernet port on each DRM concurrently.

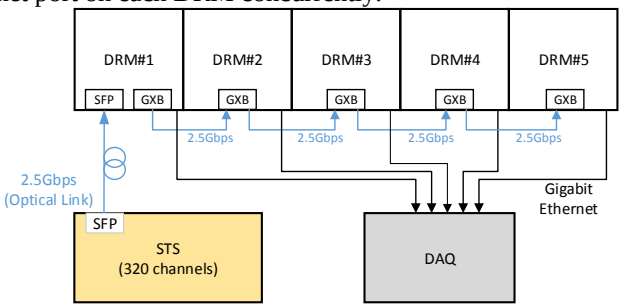

Fig. 3. Data transmission flow of one DRM group

2.3 Data acquisition software

DAQ software is running on the back-end server for data aggregation and saving, monitoring the system status and distribution the command from graphical user interface (GUI). DAQ software receives TDC data from each DRM and saves the assembled data into hard disk for further offline analysis. For the convenience of the operating and monitoring, a GUI implemented by QT5 is designed.

3 Tests and results

For confirming the performance of quality evaluation system, cable delay method is conducted. Two hit signals generated by a pulse generator (AFG3252) with a certain

time delay are connected to two TDC channels. Assuming that two channel are uncorrelated, the time resolution of one single channel is equal to the RMS value of the measurement divided by $2^{1/2}$. As shown in **Fig. 4**, the time resolution of the leading edge time is better than 20ps, which is better than the requirement.

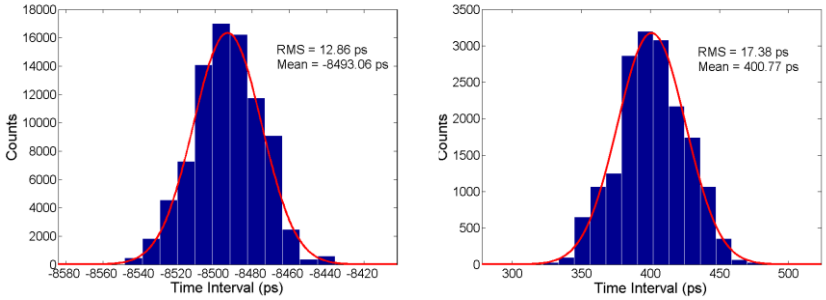

Fig. 4. Left: Time measurement results of two channels from same TDC. Right: Time measurement of two channel from two separate TDC boards.

4 Conclusion

A 320-channel time digitizing and readout electronic system is designed for quality evaluation of CBM-TOF SM. The system has a distributed and extensible architecture, mainly including FEE, BEE, and DAQ software. The laboratory test results show that quality evaluation system can work correctly and overall system has time resolution of 20 ps. The evaluation system can be subsequently used for quality control of CBM-TOF SM.

Acknowledgment

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