Back-end and interface implementation of the STS-XYTER2 prototype ASIC for the CBM experiment at FAIR

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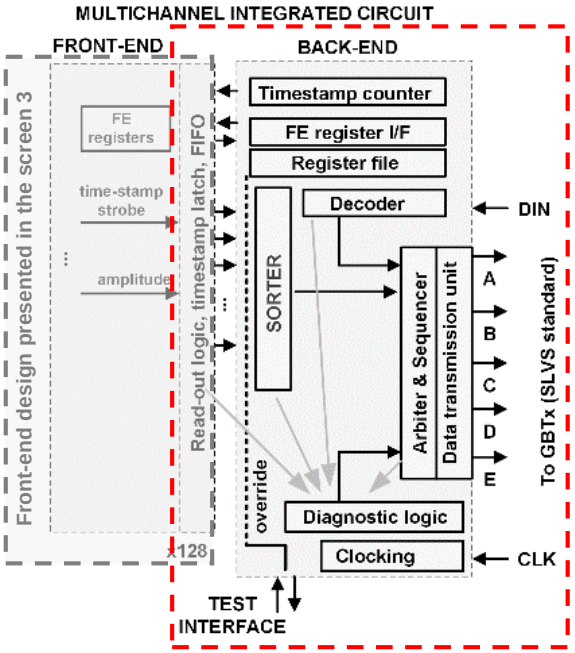
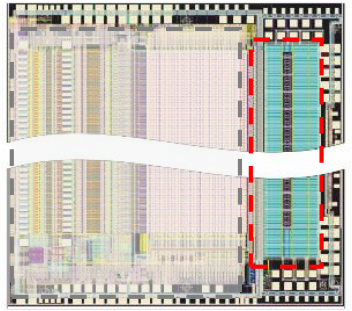
Each front-end readout ASIC for the Physics experiments requires **robust and effective hit data streaming and control mechanism**. A new STS/MUCH-XYTER2 full-size prototype chip for the **Silicon Tracking System and Muon Chamber** detectors at the Compressed Baryonic Matter experiment at Facility for Antiproton and Ion Research (FAIR, Germany) is a 128-channel time and amplitude measuring solution for silicon microstrip tracker and gas detectors and is supposed to operate at 250 kHit/s/channel hit rate, each producing 27 bits of information (5-bit amplitude, 14-bit timestamp, position and diagnostics data). The back-end implements fast channel read-out, timestamp-wise hit sorting and data streaming via scalable interface implementing a dedicated protocol (STS-HCTSP) for chip control and hit transfer with data bandwidth from 9.7 MHit/s up to 47 MHit/s. It also includes multiple options for link diagnostics, failure detection and throttling features. The back-end is designed to operate with the data acquisition architecture based on the modified CERN GBTx transceivers. This paper presents the details of the back-end and interface implementation in the UMC 180 nm CMOS process.



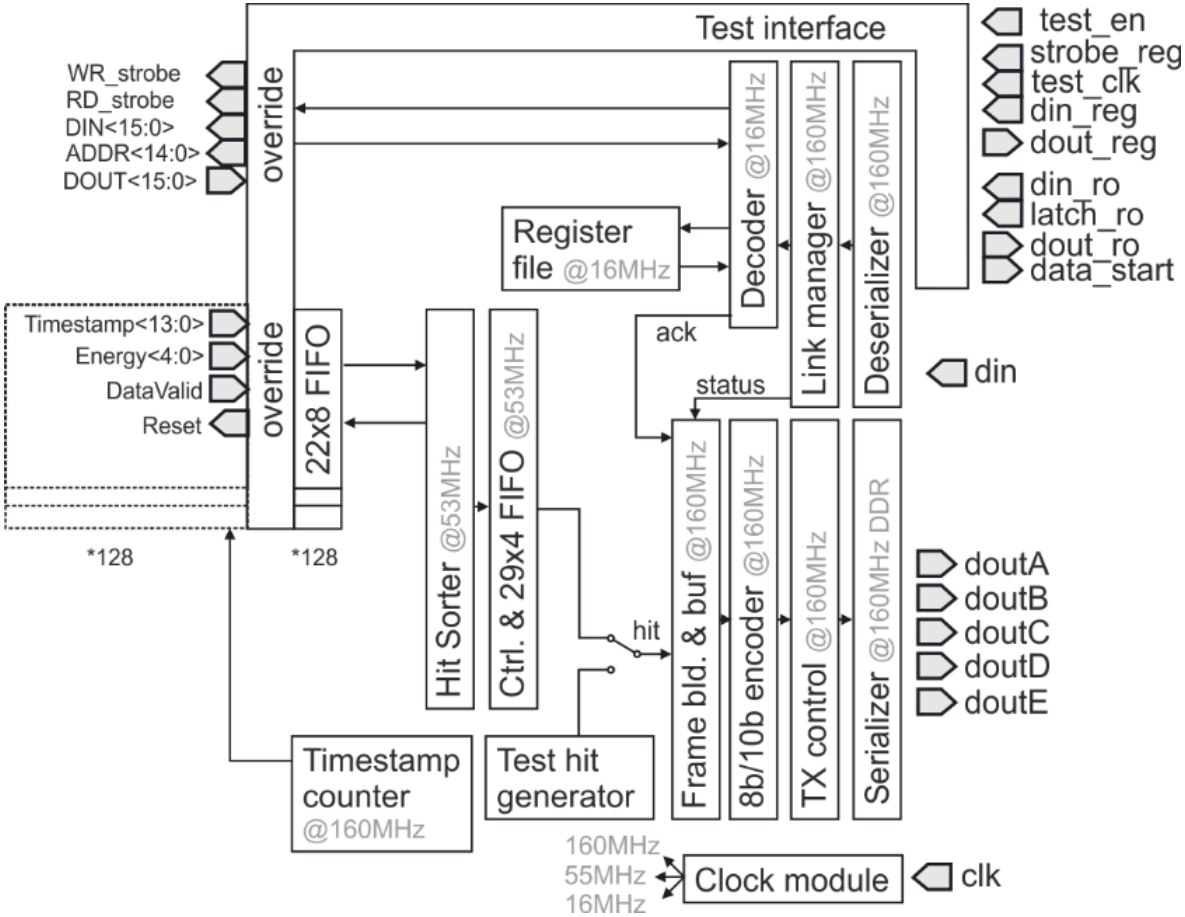

STS-XYTER2 CHIP (2016)

Come along and find more details on:

STS-HCTSP Protocol, data & control flow, diagnostic tools, throttling features...

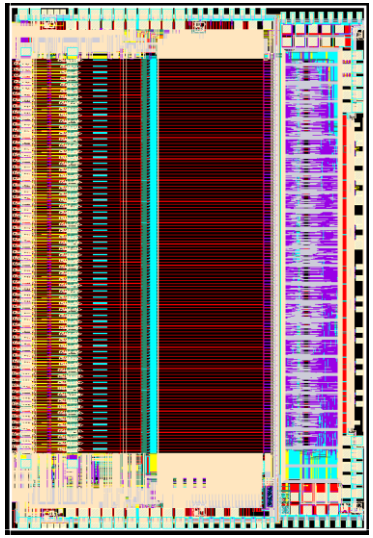
STS-XYTER2 Back-end

- Data path
- Control path
- Test interface
- Diagnostic features

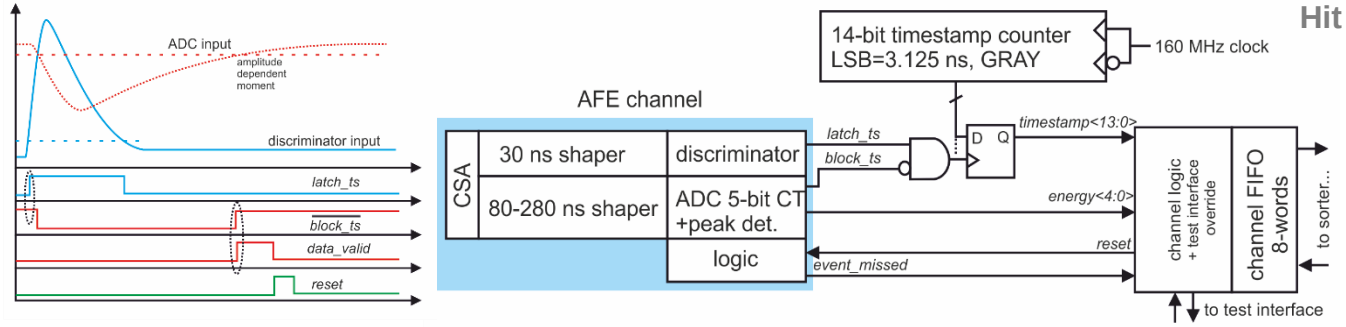


Logic triplication on control path & register file

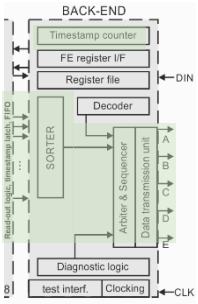
The GBTx-based readout helps keeping the ASIC simple (e.g. no prog. delays)

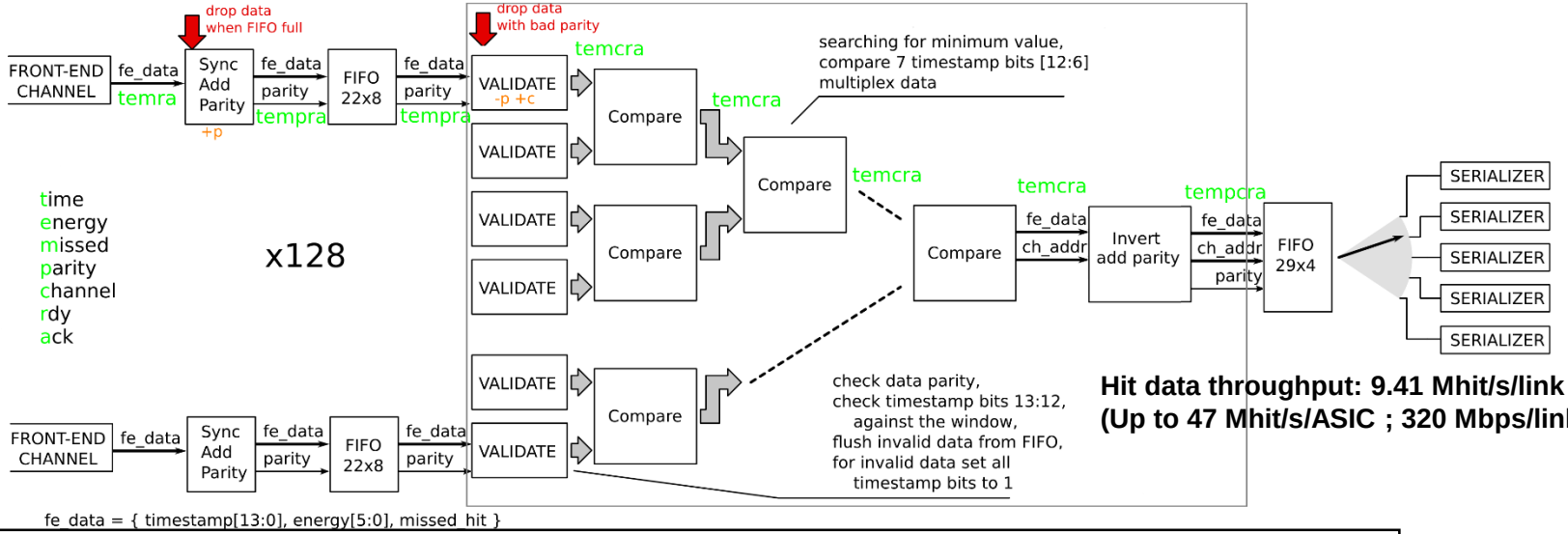


Hit Data flow - simplified



Hit data: 27 bits
7-bit channel address
5-bit energy
14-bit timestamp
1-bit event_missed flag



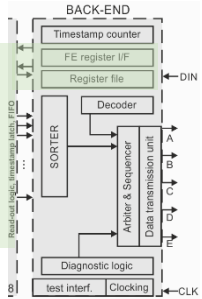


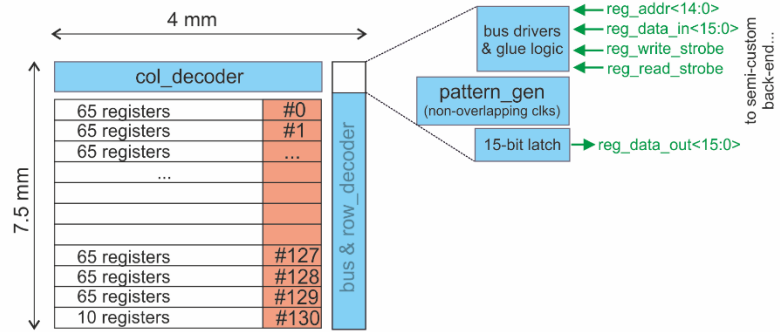
Hit data throughput: 9.41 Mhit/s/link
(Up to 47 Mhit/s/ASIC ; 320 Mbps/link)

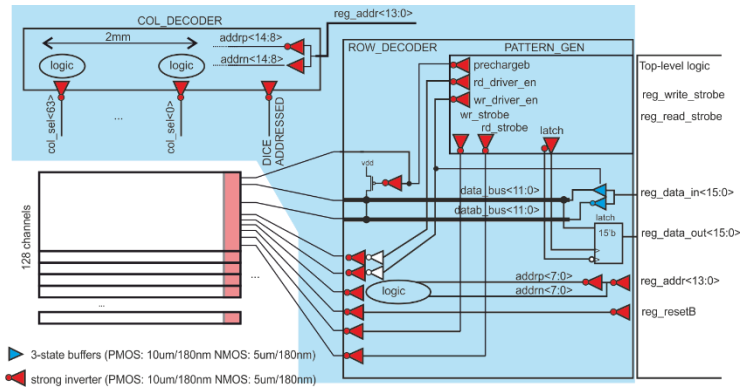
- 8-word long channel FIFOs. Sorter checks the timestamp MSB TS<13:6> only! (covers intrinsic uncertainty in the front-end)
- No geographical segmentation. Every hit via any of 1-5 links. Number of links is programmable.
- Ack. from command decoder have priority over hit data

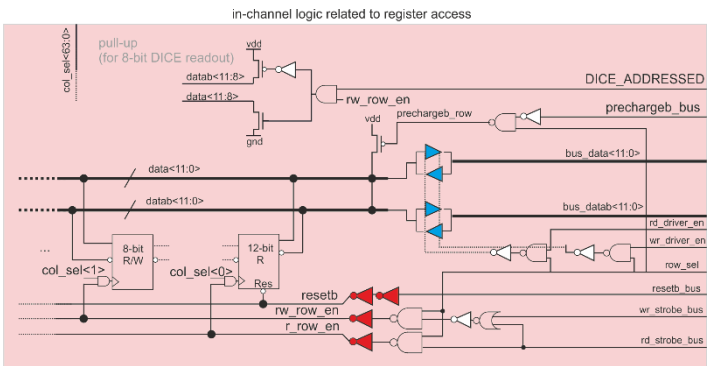
AFE Register access

- 25 MHz clock, full-custom logic interfaced to the semi-custom back-end
- Local (in-channel) bus & global (vertical) bidir bus
- Non-overlapping clock generation & delay control
- Access to 8-bit DICE cells & 12-bit counters
- enclosed layout NMOS & guard rings

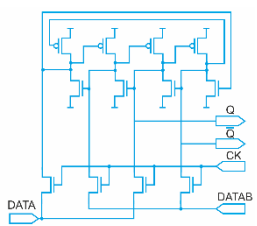


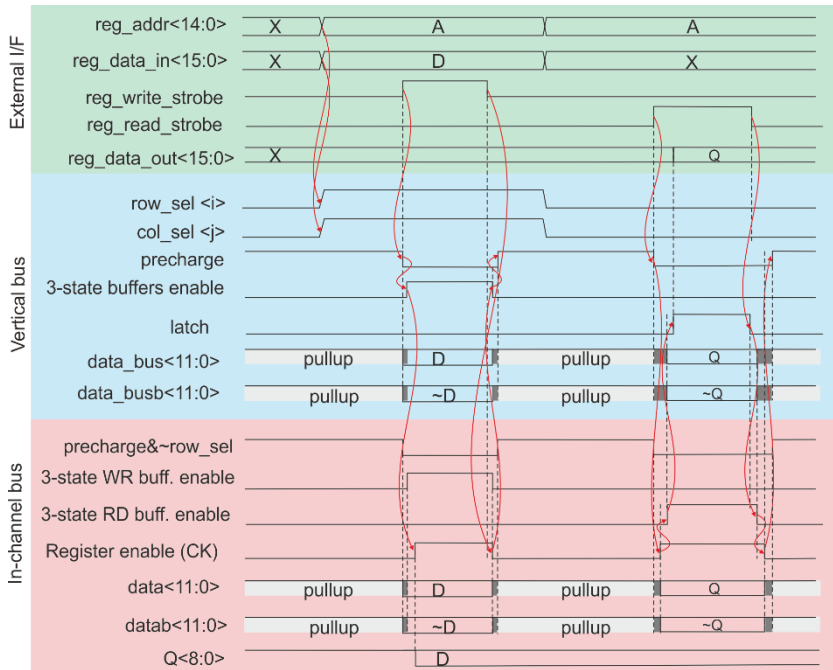




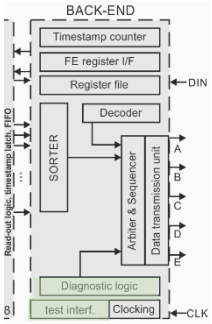


internal, bidirectional, complementary bus, drives the DICE SRAM cells & reads the counters (precharge & pull-up)



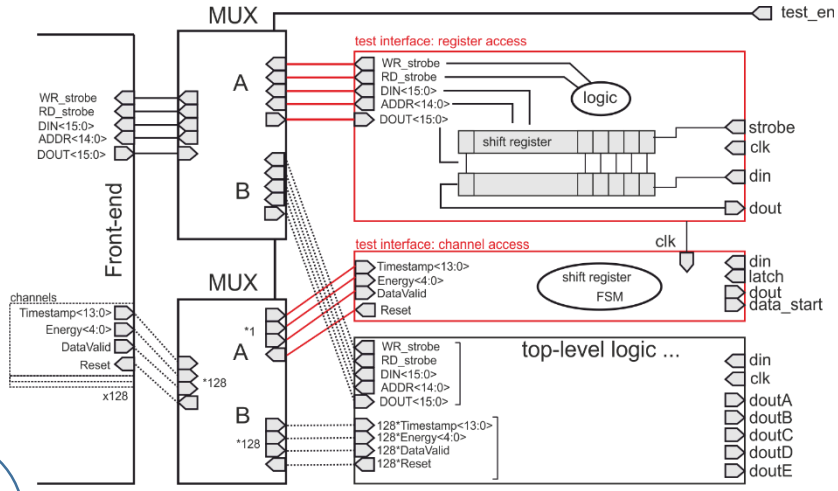


Diagnostic features



Test Interface:
- simple, SPI-like protocol, 20 Mbps
- overrides AFE control of the full back-end
- access to all AFE registers
- read-out of 1, selected channel

Aim:
- **estimate digital-related noise** (small number of resources are clocked, only 20 MHz clock, no 160 MHz)
- simplify initial tests

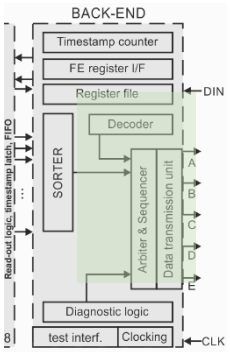


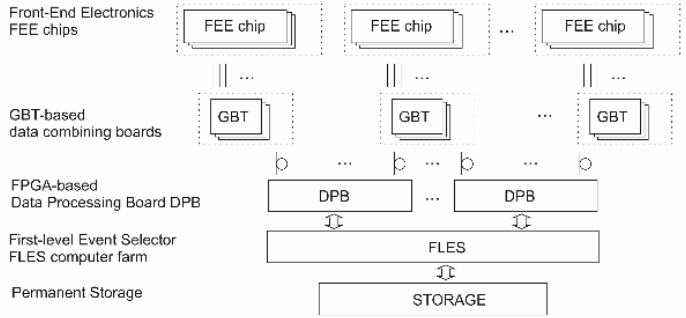
Diagnostic features:
- built-in hit generator (2 modes: via front-end, only-digital), programmable rate (1.6 – 52 Mhit/s/chip)
- test data can be random or deterministic
- test trigger for each individual channel
- multi-level software reset (forensics possible after any failure)
- SEU counter (in synthesized registers)
- Control Parity (in selected DICE Front-end registers)
- General purpose ADC for monitoring external potential (e.g. power supply)
- Link diagnostics (CRC problem, synchronization problems)
- e-fuse based chip identification (traceability database)

Throttling features:
- **Aim:** cure for intensity fluctuations (controllable data drop scheme)

Method:
- decision made by master system (not the ASIC!)
- **Actions possible:** Flush FIFO, DAQ stop, channel mask
- ASIC provides metrics & signaling of incoming problem (alert status)
- Programmable thresholds on FIFO full, FIFO almost-full, event-missed

An STS Hit & Control Transfer Synchronous Protocol (STS-HCTSP)

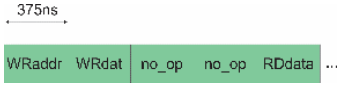




Physical Interface:
- LVDS drivers, receivers
- Can operate with LVDS/SLVS signaling
- AC-coupling via high-voltage >1nF capacitors (data bandwidth)
- built-in biasing resistors > 50 kohm set biasing to 1.2V
- hardware addressing via wire-bonds

- GBTx based DAQ; 8 chips/PCB, AC-coupled links
- shared downlink (2.6 Mframes/s) & clock (160 MHz)
- Frames: 60 bits uplink / 30 bits downlink
- individual uplinks (9.4 – 47 Mhit/s/chip)
- simple design on the ASIC side
- **novel link synchronization method**
- optimization for Hit-data bandwidth
  (no CRC on hits, huffmann encoding, data compression)
- chip addressing via wire-bonding (HW addr)

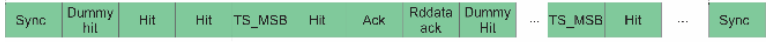
Downlink (to ASIC) 2.6 Mframes/s



Frame type	60 bits after 8b/10b encoding				
	Comma	**Control fields**	**Request type**	**Payload**	**CRC**
No_op	**K28.1**	2-bit chip addr. 4-bit seq. no.	**2'b00**	15-bit Data	15-bit CRC
WRaddr			**2'b00**		
WRdata			**2'b00**		
RData			**2'b00**		

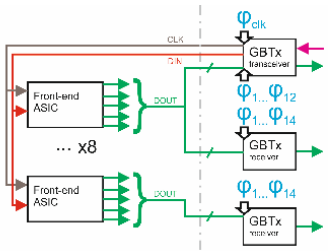
approx. 50 µs

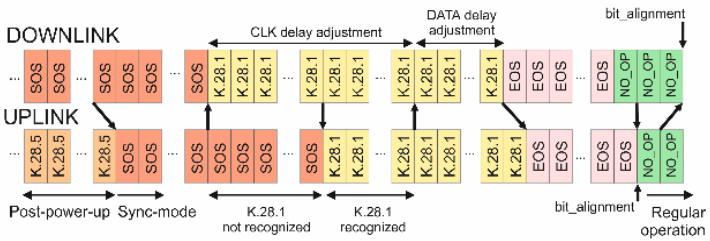
Uplink (from ASIC) 9.41 Mhit/s/link



93.75ns

Type	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Sync	K28.1 comma character								K28.1 comma character								K28.1 comma character							
Dummy Hit	0	7-bit channel address = 0x0							5-bit ADC = 0x0					0x0		0x0								0
Hit	0	7-bit channel address							5-bit ADC > 0x0					TS<10:9> (overlap)		Timestamp<7:0>								EM
TS_MSB	1	1	Timestamp<13:8>						Timestamp<13:8>							Timestamp<13:8>				4-bit CRC				
RDdata_ack	1	0	1	15-bit register content															3-bit CRC			3-bit CRC		
Ack	1	0	0	ACK	4-bit seq number.				CP	4-bit status value						Timestamp<5:0>				4-bit CRC			





SOS & EOS are easily detectible even when link is not synchronized.

K. Kasinski et al. A Protocol for Hit & Control Synchronous Transfer for the Front-End Electronics at the CBM Experiment, NIM-A (soon)