Front-end of the STS/MUCH-XYTER2, full-size prototype ASIC for CBM experiment

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We present a complete design of the analog front-end of the STS/MUCH-XYTER2 ASIC, a full-size prototype chip for the Silicon Tracking System (based on double-sided silicon strip sensors) and Muon Chamber (gas sensors) detectors at the Compressed Baryonic Matter experiment at FAIR, Germany. The charge processing channel includes a charge sensitive amplifier, shaper amplifiers forming two signal paths for timing measurement via a fast discriminator and low-noise amplitude measurement by a 5-bit continuous-time ADC with digital peak detector. Harsh environment, different operating conditions and constraints posed by two target detector applications required flexibility and careful design to meet extended system-wise requirements. The presented circuit implements switchable shaper peaking time, gain switching and trimming, pulsed reset of the amplifier for increased input charge rate and faster recovery from overload, fail-safe measures and diagnostic modes for wafer-level and in-system testing and calibration. The power consumption is scalable (for STS and MUCH modes) but limited to 12 mW/channel.

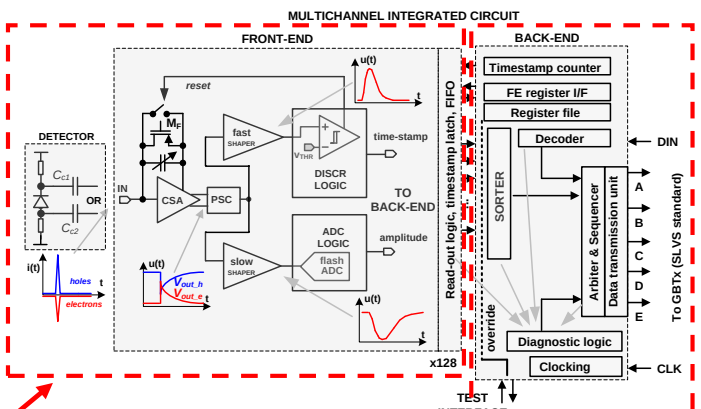

Fig. 1. The simplified architecture of the 128-channel STS/MUCH-XYTER2 ASIC.

This poster is focused on the front-end electronics.

Back-end part is presented in the screen 2.

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Main application requirements:

- multichannel self-triggerred architecture (50 µm pitch),
- deposited charge time and energy measurements,
- average rate of input pulses 250 kHz/channel,
- input charge in the range (electrons and holes):
  - 0.5 fC – 15 fC for the STS mode,
  - 1 fC – 100 fC for the MUCH mode,
- detector capacitance at the order of tens pF,
- low noise ENC < 1000 e^- rms at C_{DET} = 30 pF,
- limited power consumption < 10 mW/channel
- good uniformity of analog parameters between channel,
- radiation-hardness property.

Readout front-end architecture:

- input stage: Charge Sensitive Amplifier + Polarity Selection Circuit,
- fast path:
  - optimized to determine the input charge arrival time with the resolution of the order of few ns,
  - built of: CR-RC shaper with tp = 40 ns, discriminator, time-stamp latch, pulse stretcher,
- slow path:
  - optimized for accurate energy measurement:
  - built of: CR-$(RC)^2$ based shaper with switchable tp = 80, 15, 220, 280 ns, 5-bit flash ADC, digital peak detector.

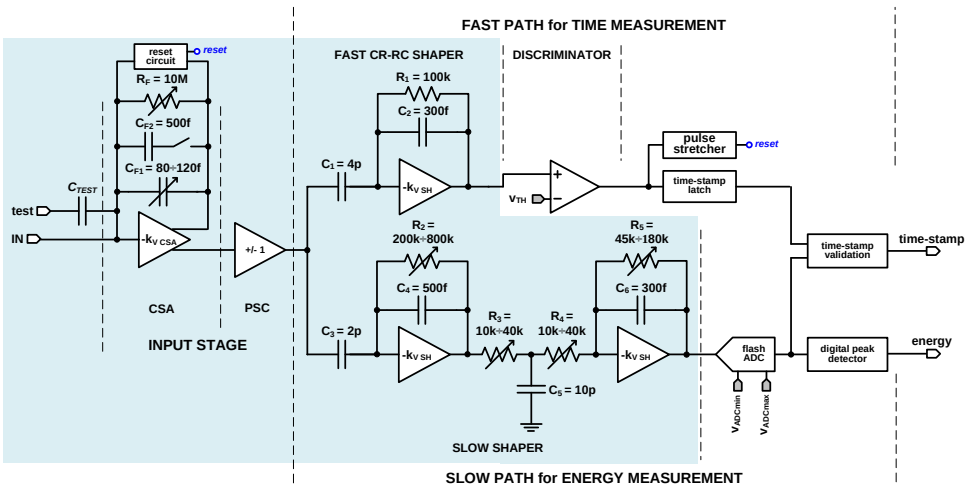

Fig. 2. The simplified architecture of the single readout channel implemented in the STS/MUCH-XYTER2 ASIC.

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Charge Sensitive Amplifier:

- based on the direct cascode architecture:
  - input branch current range 0 – 3.9 mA (def. 2 mA),
  - cascode branch current range 0 – 70 μA (def. 30 μA)
  - parameters for default settings: voltage gain k_V = 4.8 kV/V, GBW = 9.1 GHz, power dissipation P_{CSA} = 2.7 mW,
- charge gain: k_q = 9.4 mV/fC for STS mode and k_q = 1.67 mV/fC for MUCH mode,
- CSA feedback: capacitances C_{FB_STS}, $C_{FB\_TRIM1\&2}$ (gain trimming), C_{FB_MUCH}, resistance $R_F \approx 10$ MΩ and reset circuit,
- features:
  - double polarities operation,
  - fast recovery from overload,
  - spark protection,
  - fail-safe operation (C_C failure)
  - crosstalk-proof.

Polarity Selection Circuit:

- based on differential pair architecture.
- single ended voltage gain k_V = 1 V/V,
- power dissipation P_{PSC} = 0.5 mW

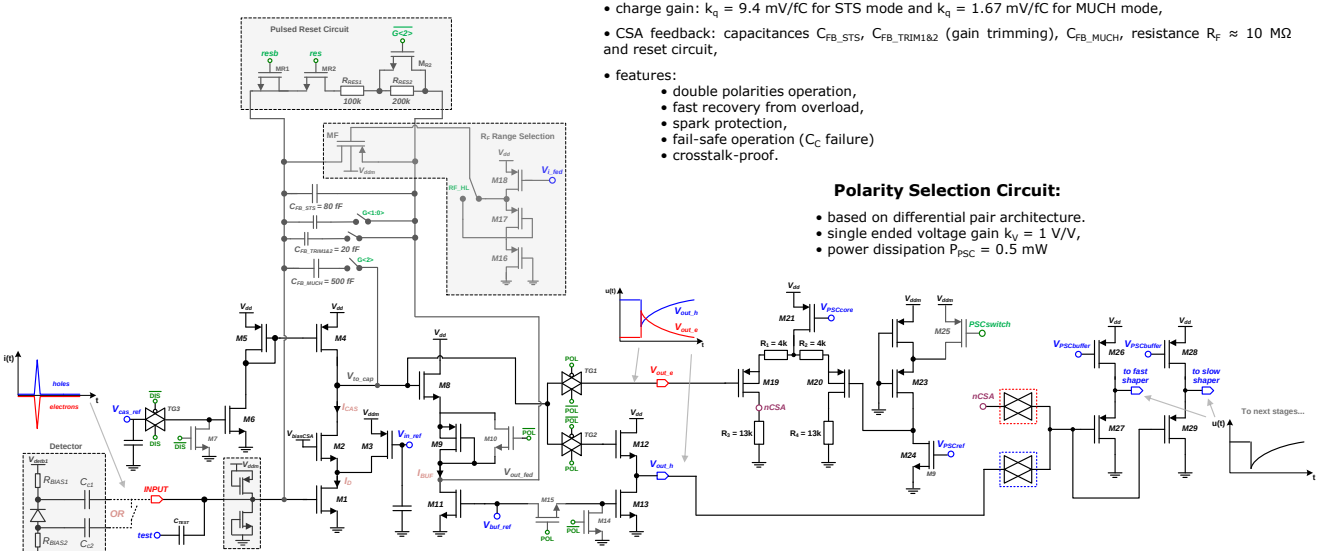

Fig. 3. The input stage architecture details: Charge Sensitive Amplifier (CSA) + Polarity Selection Circuit (PSC).

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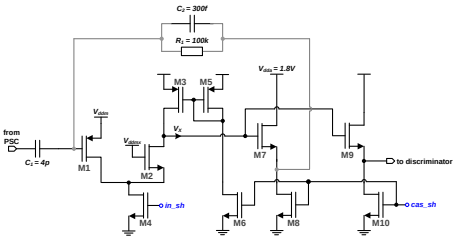

Fig. 4. Shapers' core voltage amplifier architecture.

Shapers' core voltage amplifier:

- based on folded cascode architecture.
- voltage gain k_V = 2.5 kV/V,
- GBW = 1.3 GHz,
- power dissipation P_{SHcore} = 0.4 mW.

Fast shaper*:

- peaking time t_p = 30 ns,
- charge gain k_q = 84 mV,
- ENC = 778 e^- rms.

Slow shaper*:

- peaking time t_p = 80 ns,
- charge gain k_q = 40 mV,
- ENC = 510 e^- rms.

* schematic level simulation, pure detector capacitance model C_{DET} = 30 pF.