GOETHE UNIVERSITÄT FRANKFURT AM MAIN

# Read-Out Resilience in Radiation Environments

DPG-Frühjahrstagung
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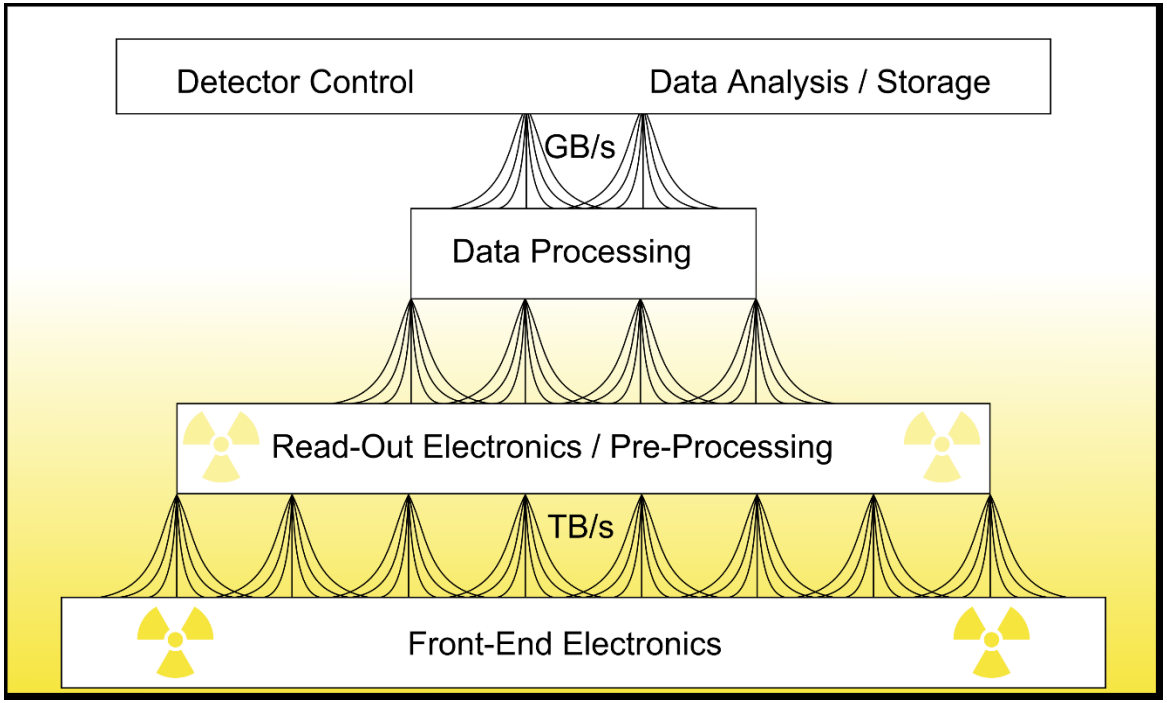
05P12RFFCM

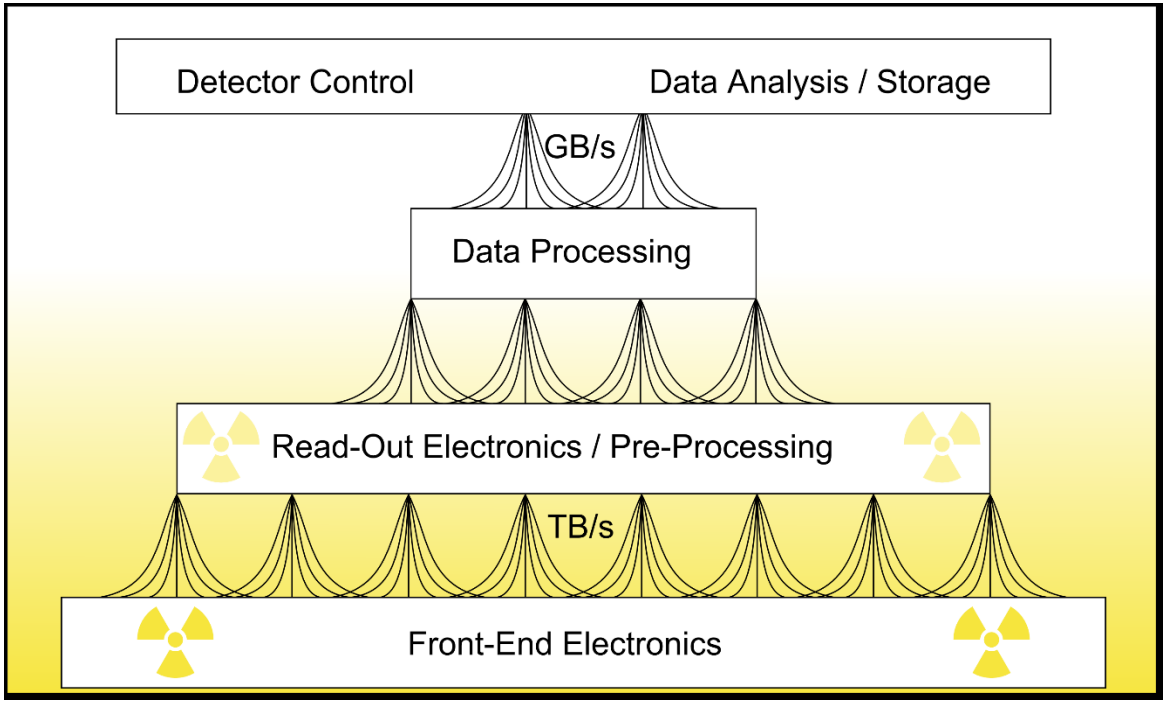
HGS-HIRe for FAIR
Helmholtz Graduate School for Hadron and Ion Research

# Motivation



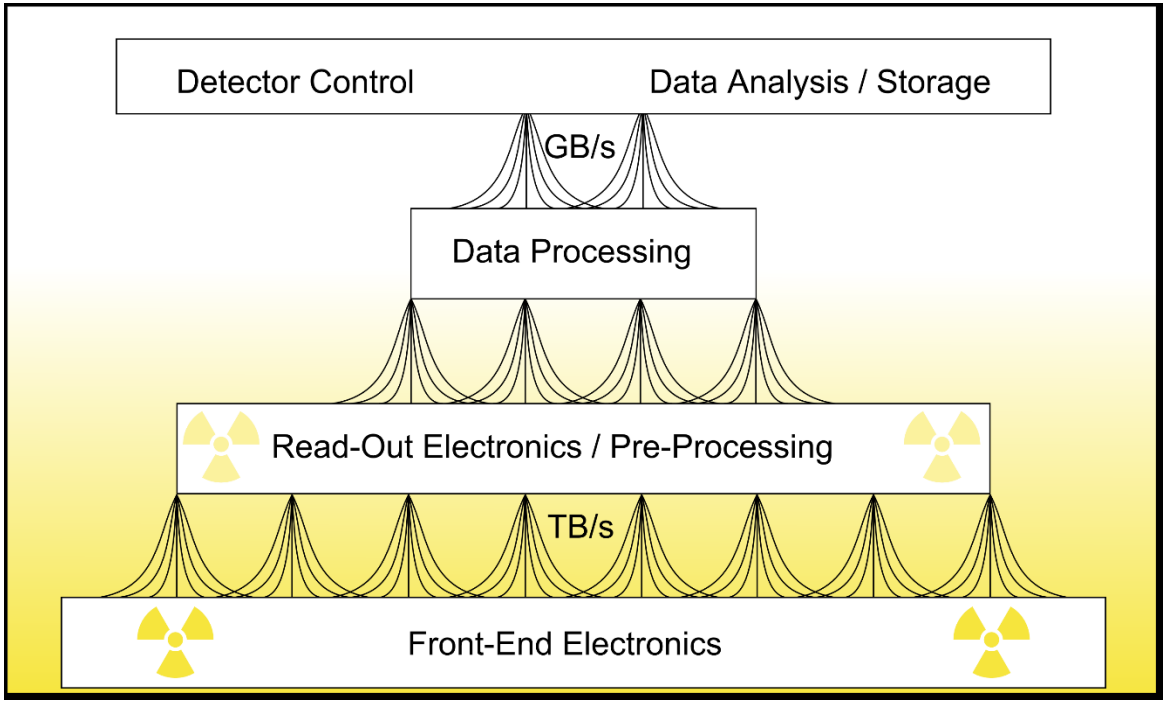

- General task: Transport data from front-end to back-end reliably
- Two main challenges:
  - Data reduction/compression from TB/s to to GB/s
  - Keep read-out chain running despite radiation effects

# Motivation



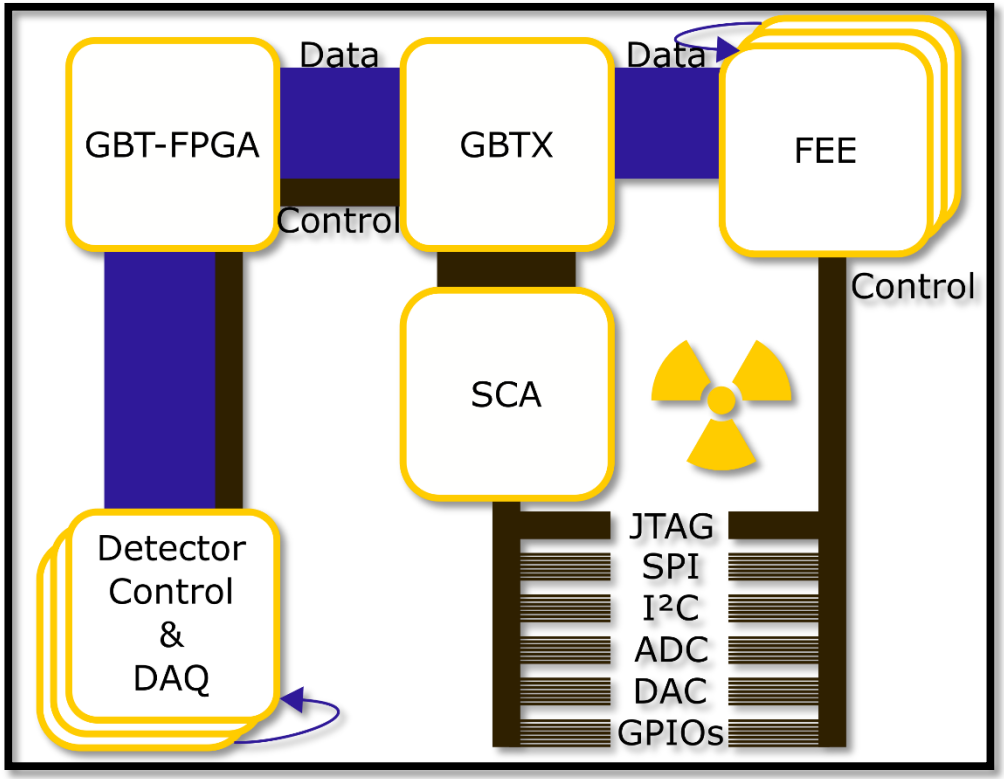

- Read-out electronics in radiation
- **FPGAs** advantageous but prone to **soft-errors**
  - **Pre-filtering**, simple data compression, status, logs, etc.
  - **Flexibility**: Firmware is adaptable to changing demands
  - Configuration destroyed by **single-event effects**

# Motivation



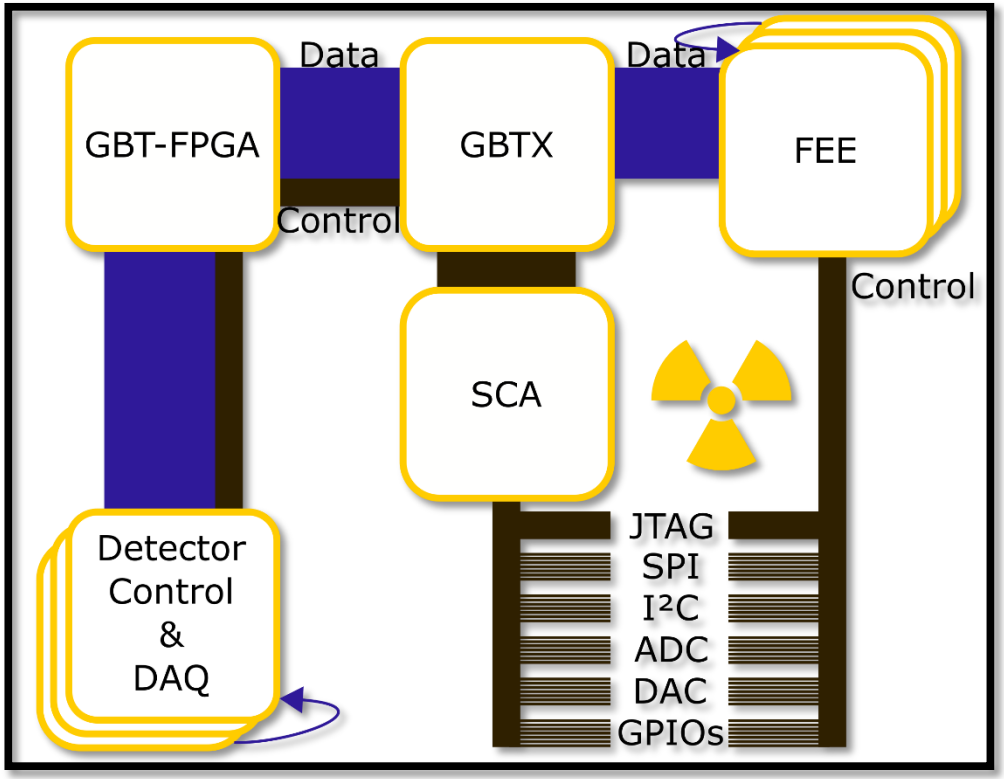

- FPGAs need soft-error mitigation
  - Fault-tolerant and autonomous **Flash free** concept needed
  - Xilinx offers Soft Error Mitigation IP-Core (**SECDED**)
  - **GBTX** offers **SCA** (Slow Control Adapter ASIC)
    - JTAG interface
    - Interrupt-capable GPIOs for fast reactions to upsets

# Achieving Resilience



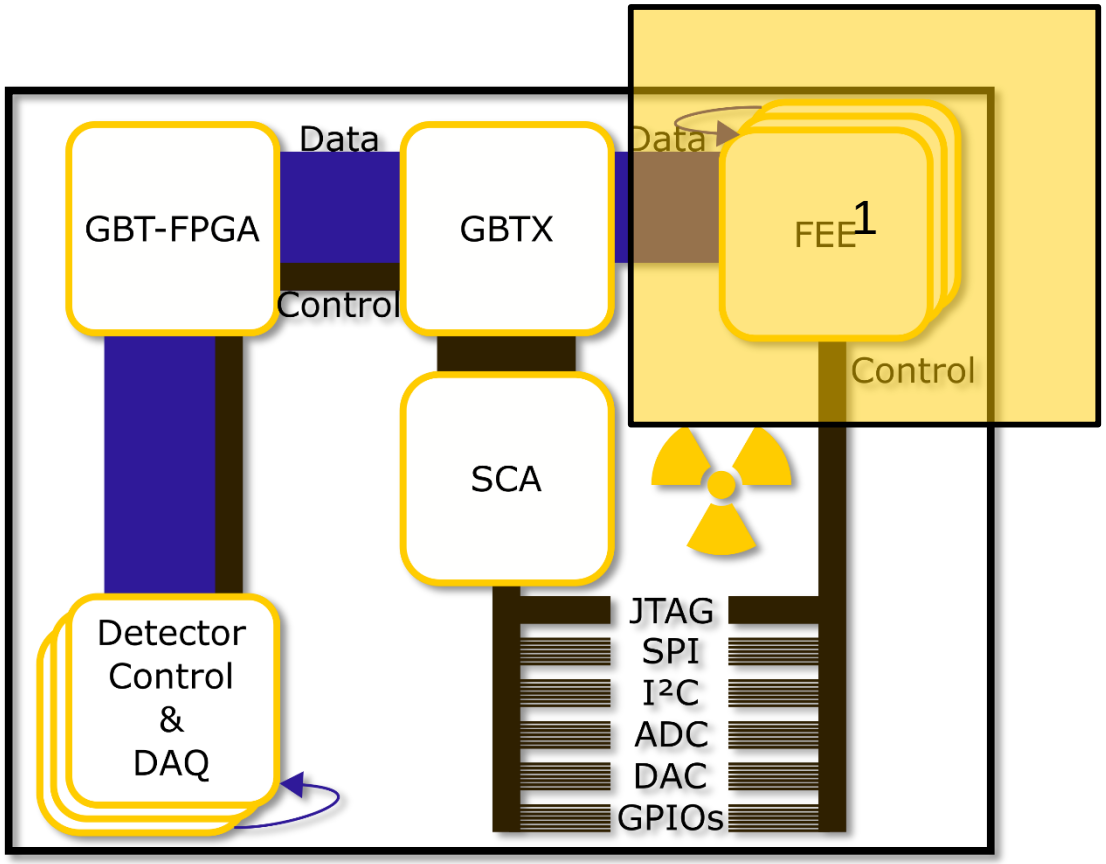

- FPGAs and Front-end ASICs need **control**, **monitoring** and **configuration**
- **Resilient data path** via GBTX (CERN)
- **Resilient control path** via GBT-SCA
- Resilient FPGAs via **hybrid scrubbing approach** for Xilinx SRAM-based FPGAs
- **Low TID of Flash** memory is problematic in the medium and long term

# Achieving General Usability




- **FEE and Back-end can be changed**
- GBTX is **data-agnostic**
- **Back-end is software** and therefore easily adapted

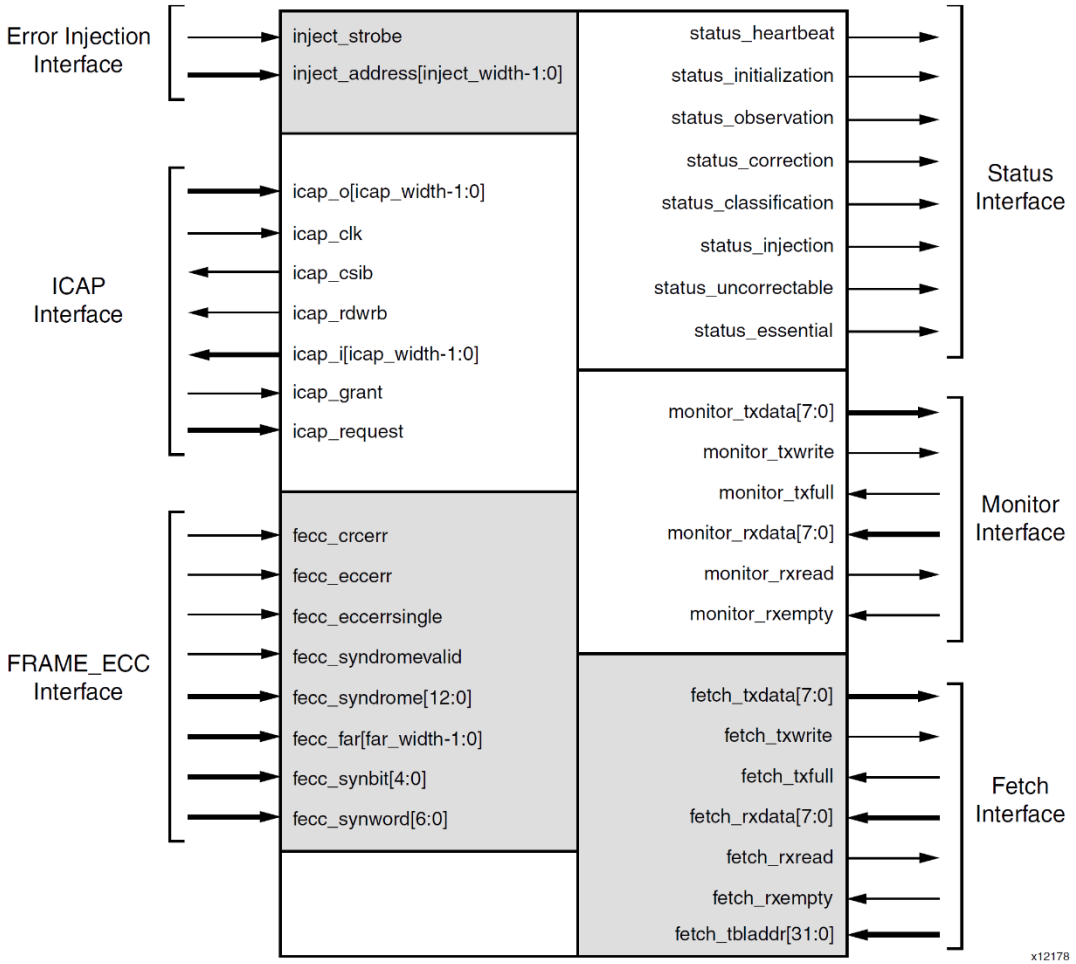
# Resilience Concept



# 7 Series Scrubbing

## Soft Error Mitigation Controller

- Automatically corrects one-bit-errors (SECDED)
- FRAME_ECCE2 for readback CRC
- ICAP for configuration
- Monitor Interface for control commands
  - Status
  - Start / Stop
  - Error Injection
  - Watchdog



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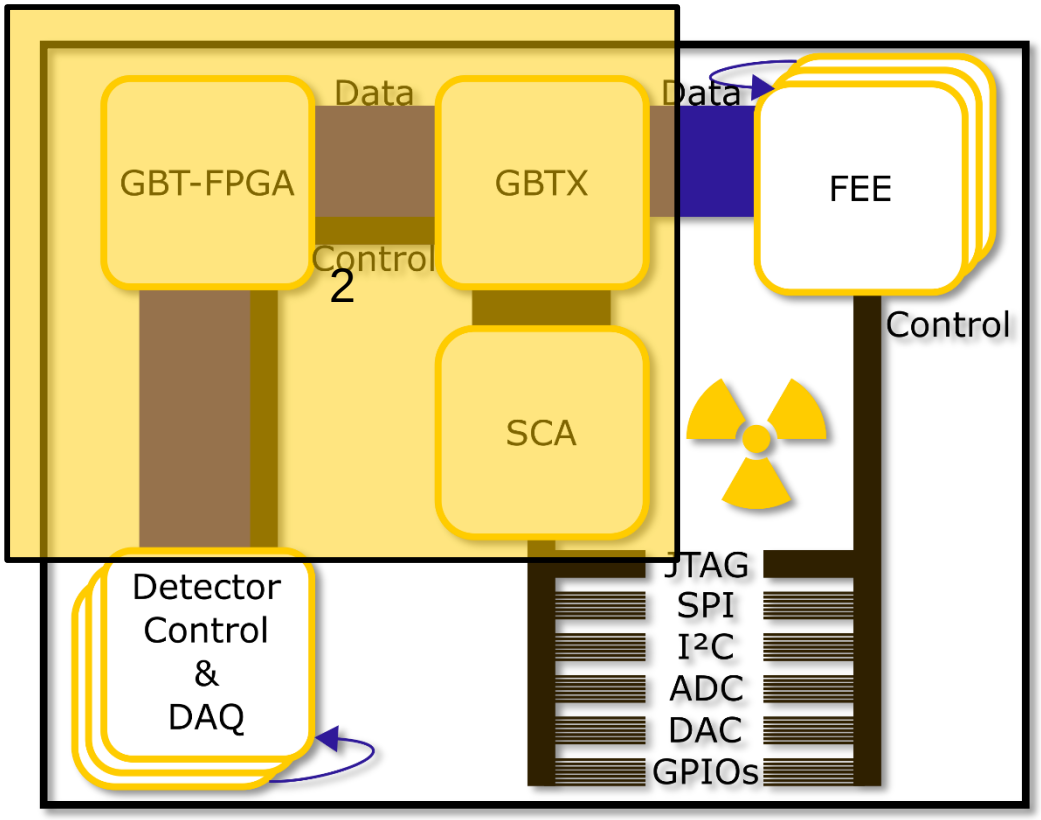
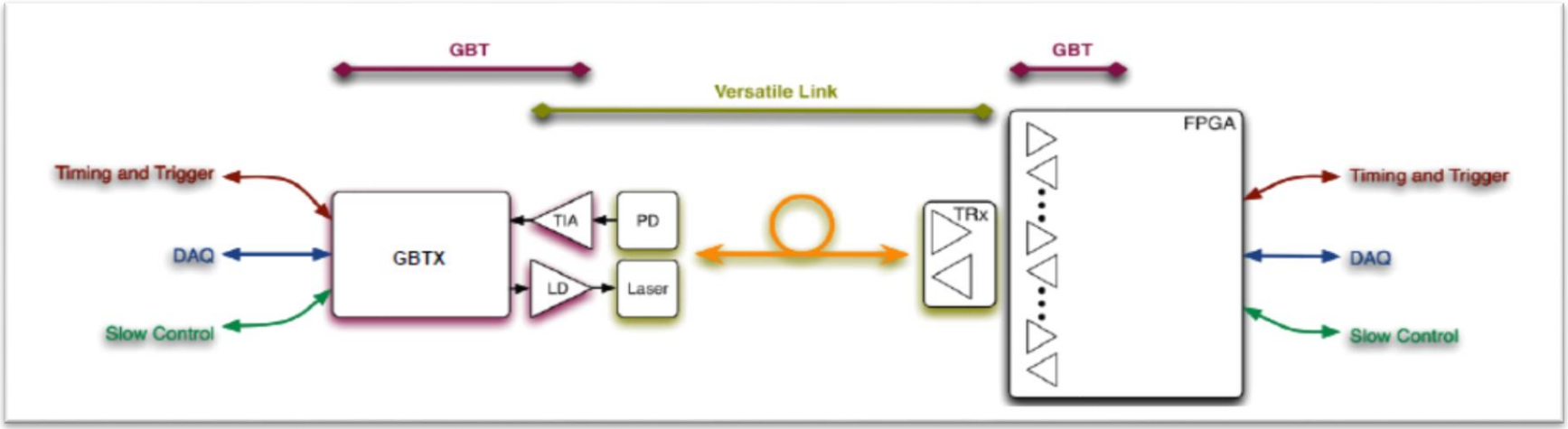


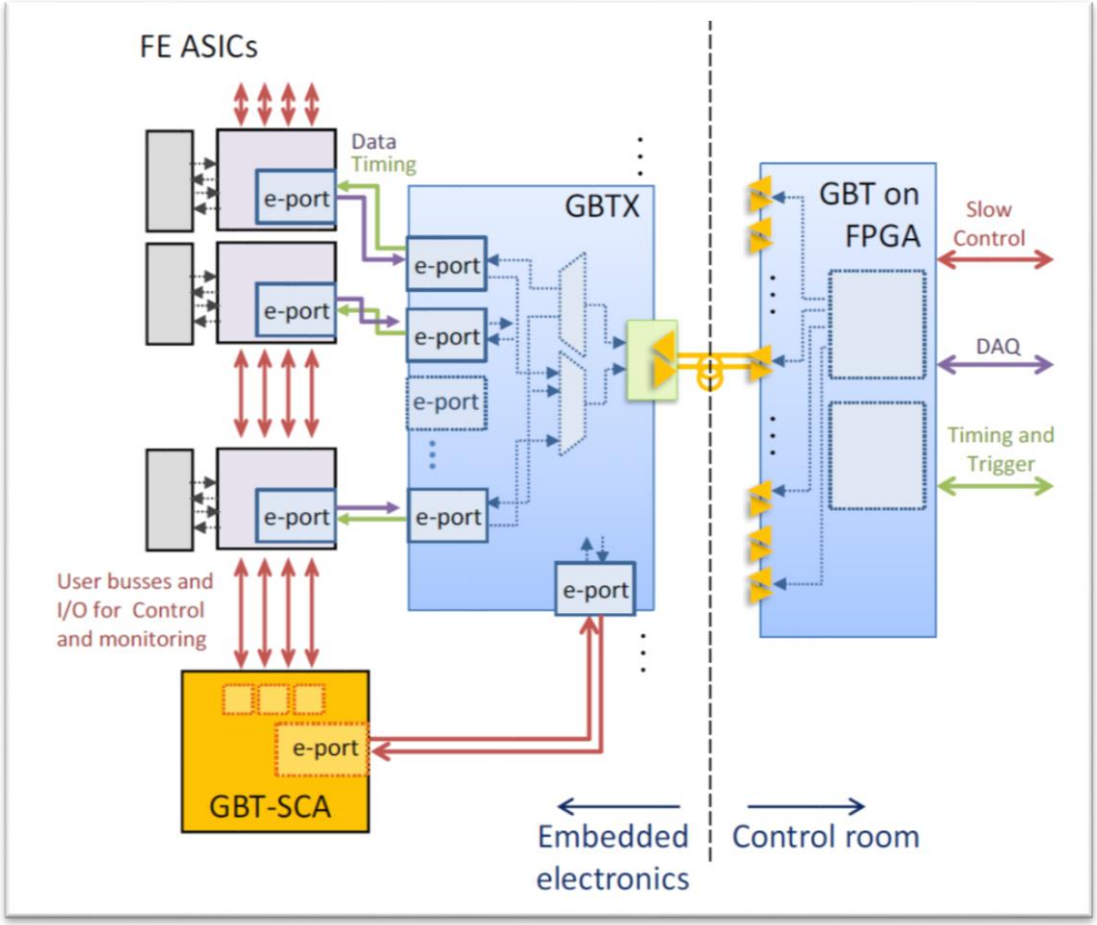
# The GBTx

- Multi-purpose high speed optical link
- Radiation tolerant
- Firmware handled by GBT-FPGA project (CERN)
- IP Core available for Link layer
- Sample designs available for various FPGAs:
  - Virtex 6, Kintex 7, Virtex 7, Kintex Ultrascale
  - StratixV, CycloneV, Arria10
- GBT-SCA for slow control



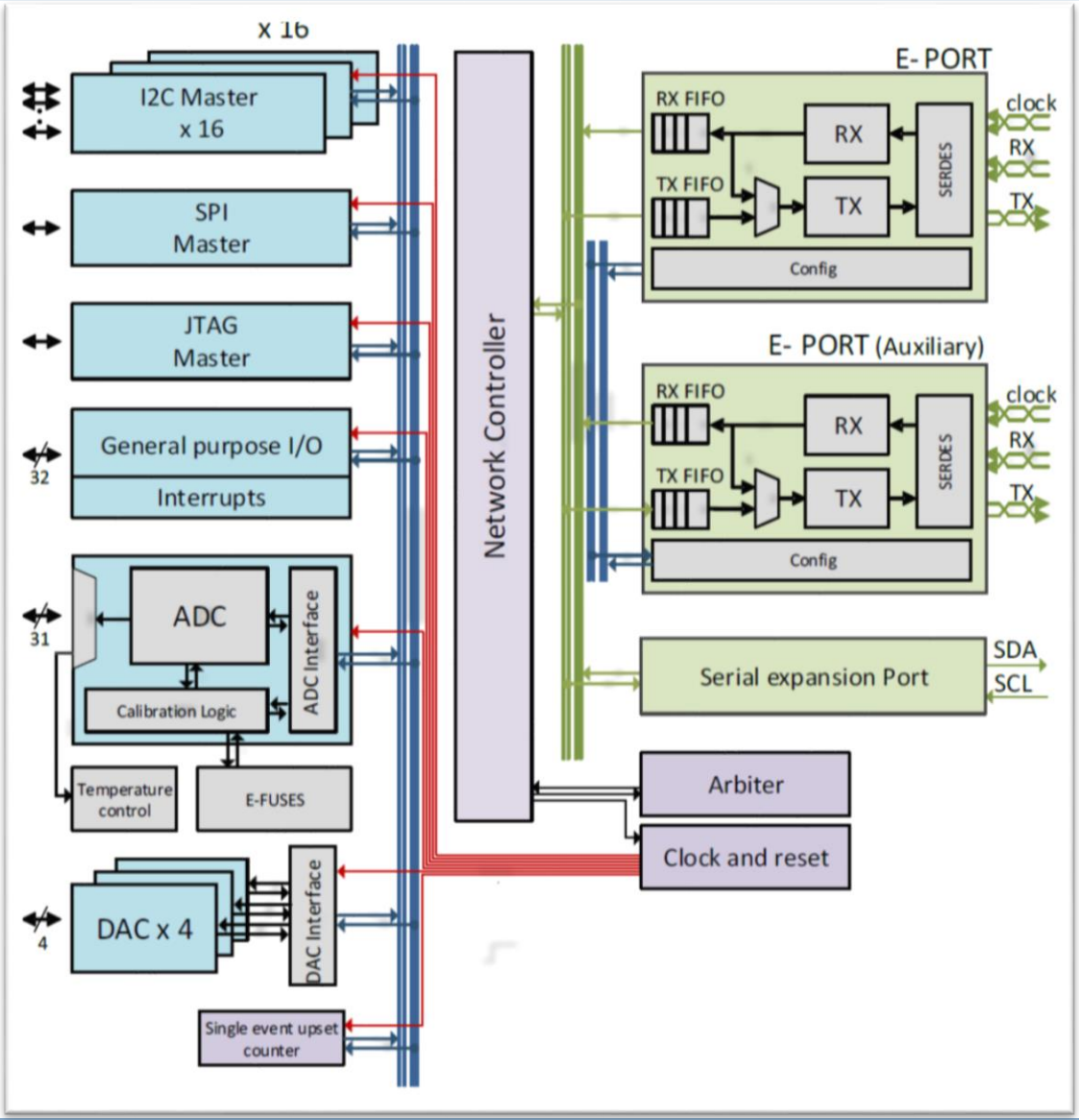
# The GBT-SCA

- **ASIC dedicated to slow control**
- **Offered features include:**
  - JTAG master player
  - $I^2C$
  - GPIOs
  - SPI
  - DAC
  - ADC
- **IP Core for SCA in pipeline**



# The GBT-SCA

- **Transparent communication with modules**
- **Every module is accessible to the user as a channel**
  - Channel address determines module
  - Every channel has a set of commands
  - Commands are acknowledged



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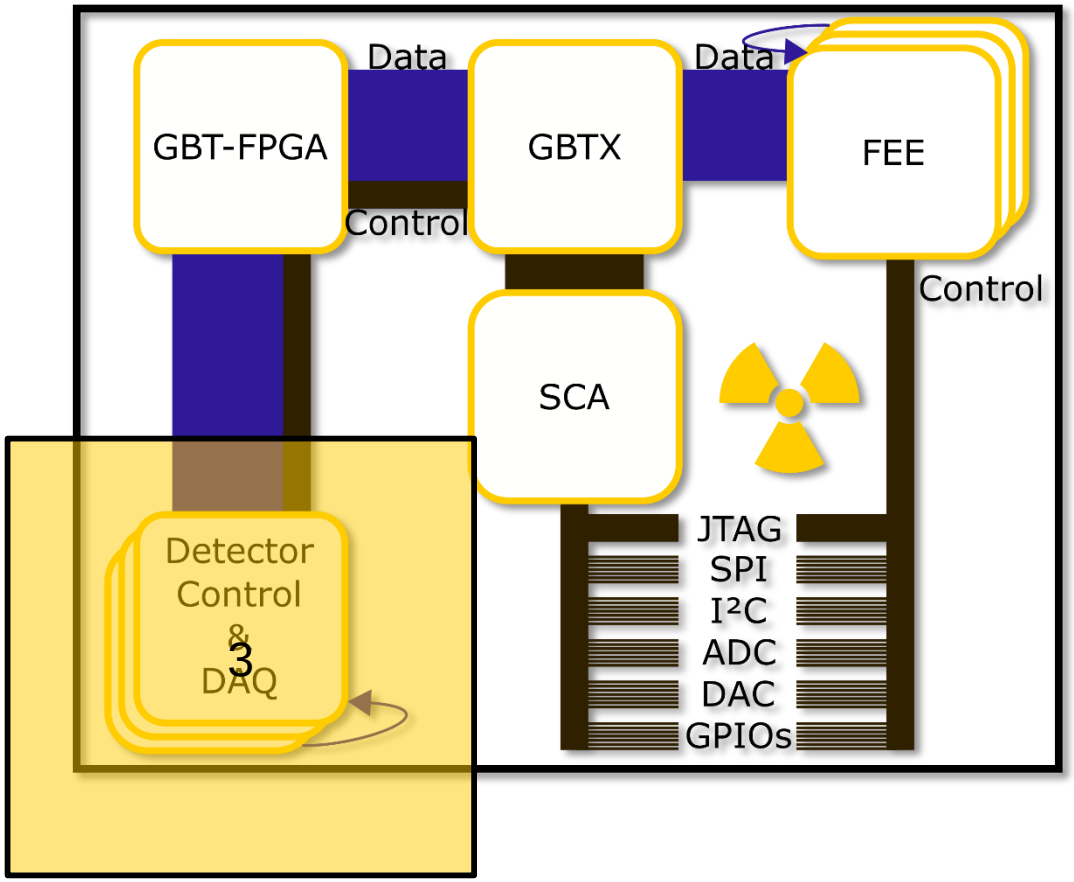
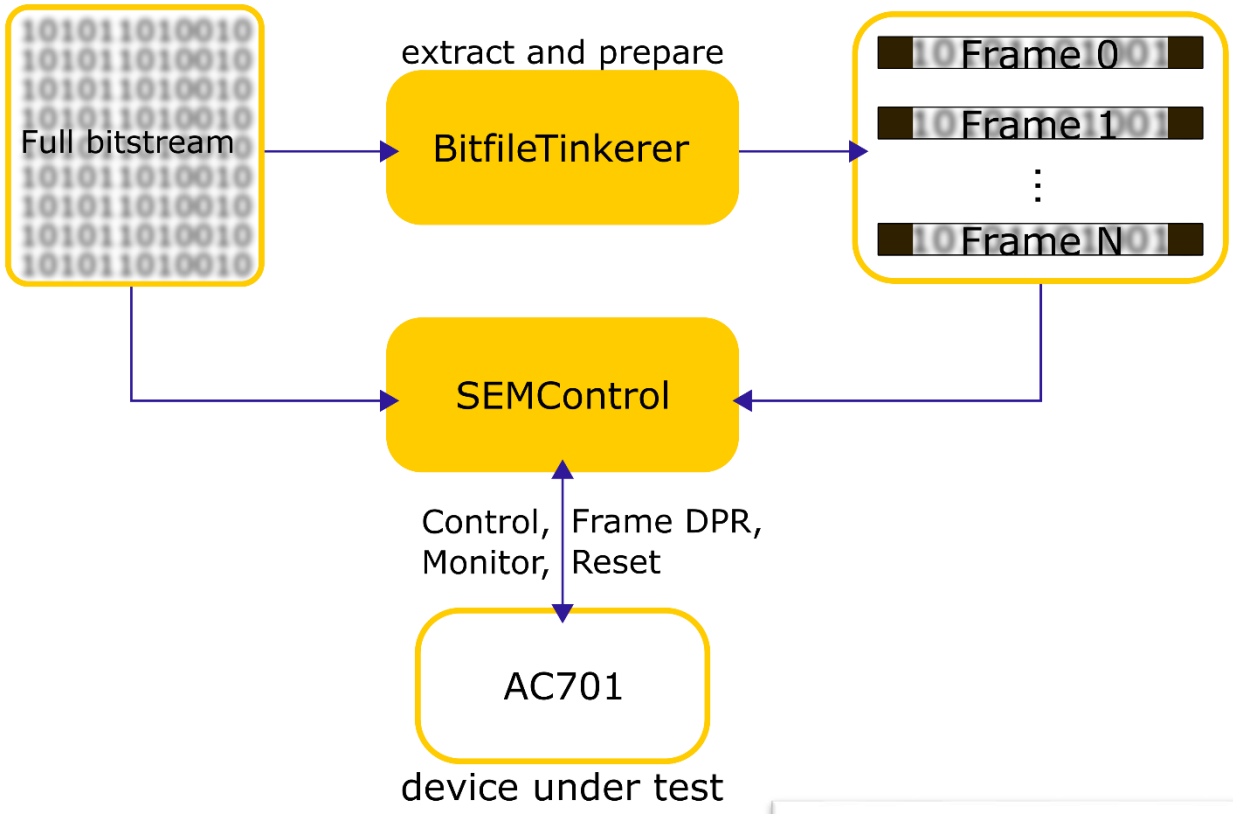


# Scrubbing Strategy




•Concept is validated and published:
A resilient, flash-free soft error mitigation concept for the CBM-ToF read-out chain via GBT-SCA
FPL 2015
doi: 10.1109/FPL.2015.7293999

A Resilient, Flash-Free Soft Error Mitigation Concept for the CBM-ToF Read-Out Chain via GBT-SCA

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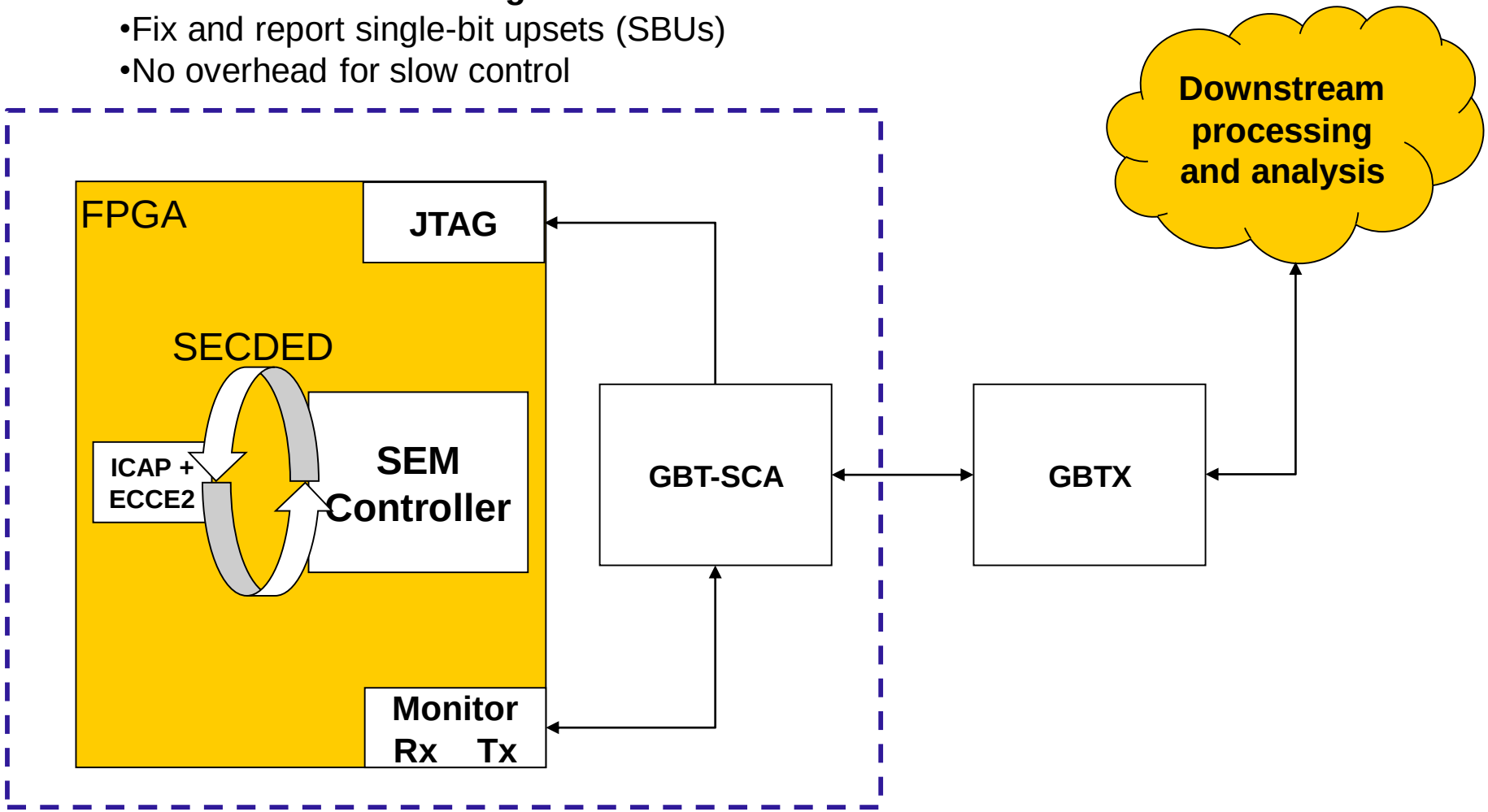
*Abstract*—The ToF detector read-out chain of the upcoming CBM experiment at FAIR will be equipped with FPGA-based

be taken in order to keep the ROBs, and thereby the DAQ chain, up and running. The developed approach implements

# Scrubbing Strategy

- **Continuous readback through ICAP**
  - Fix and report single-bit upsets (SBUs)
  - No overhead for slow control



# Scrubbing Strategy

- **Continuous readback through ICAP**
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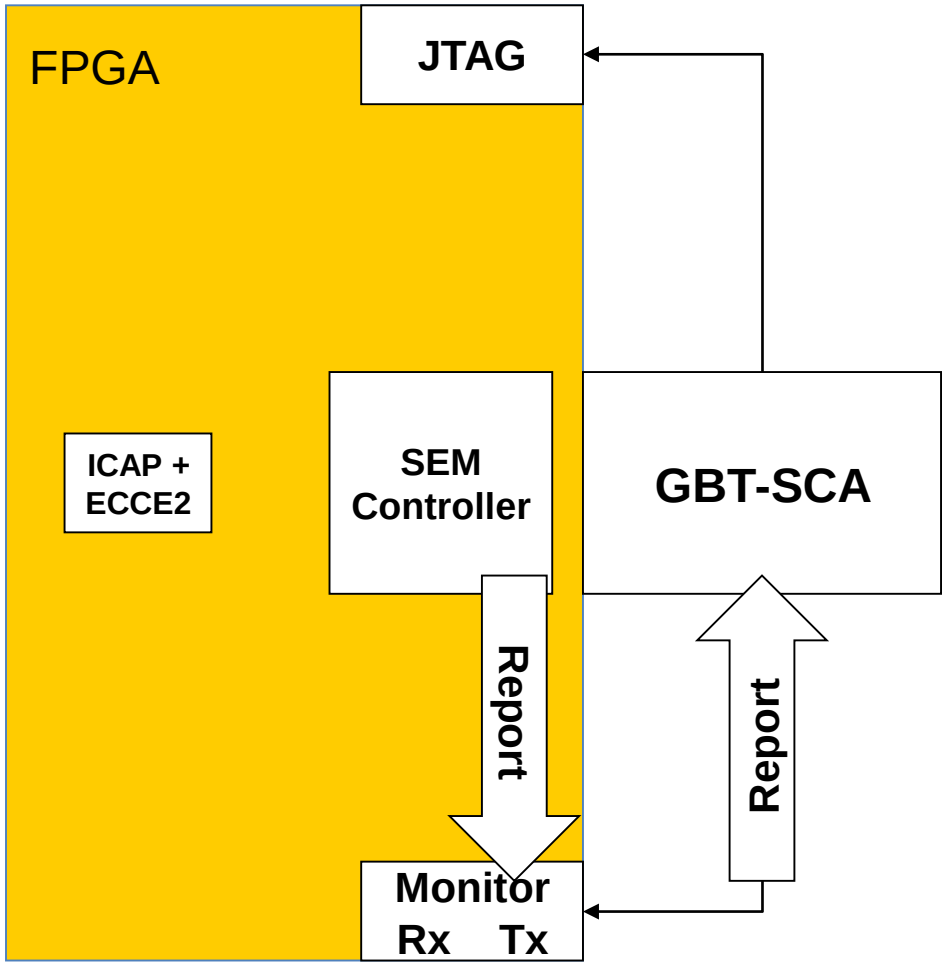
- **On multiple-bit upset (MBU)**
  - report and stop



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  - Fix error
    - ECC error: Reconfigure frame
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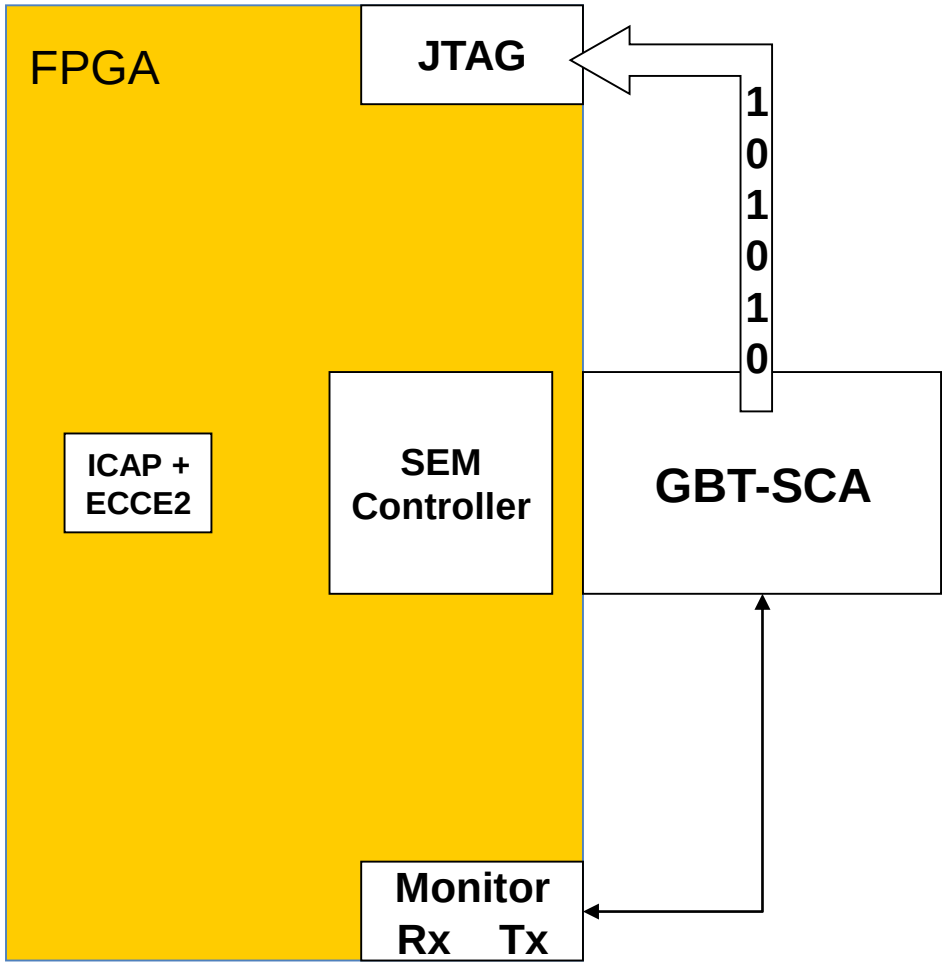

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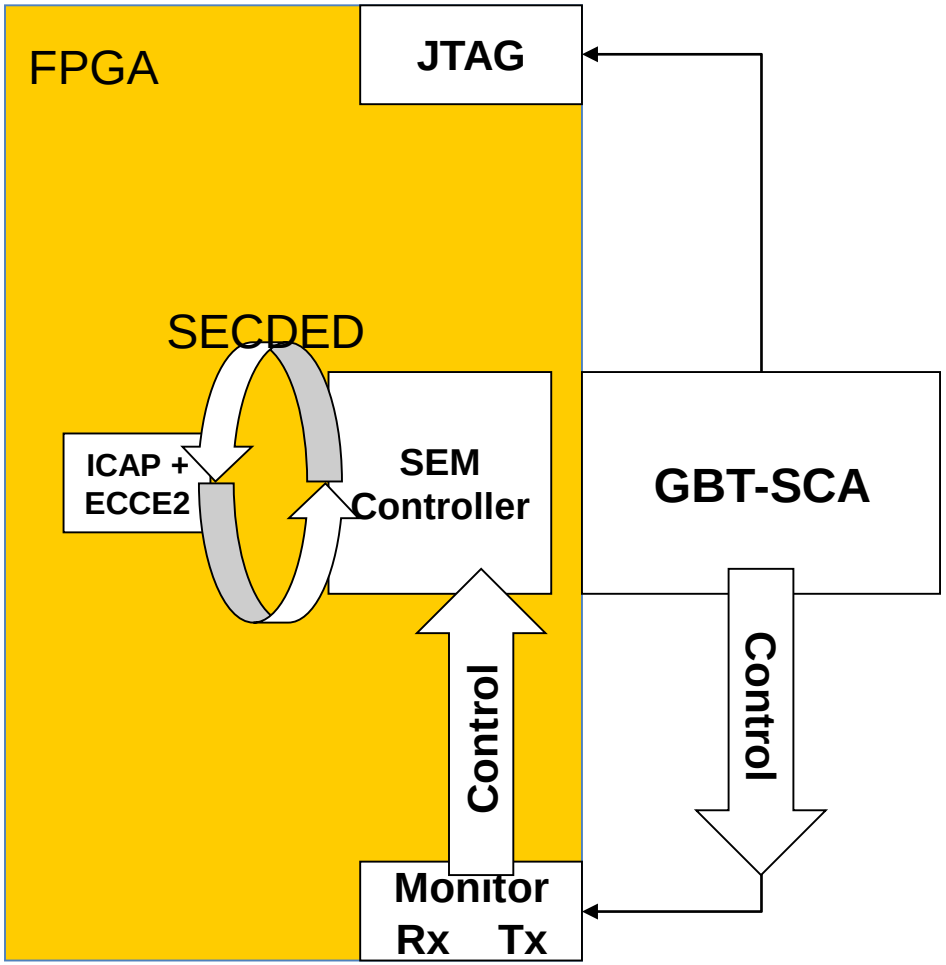
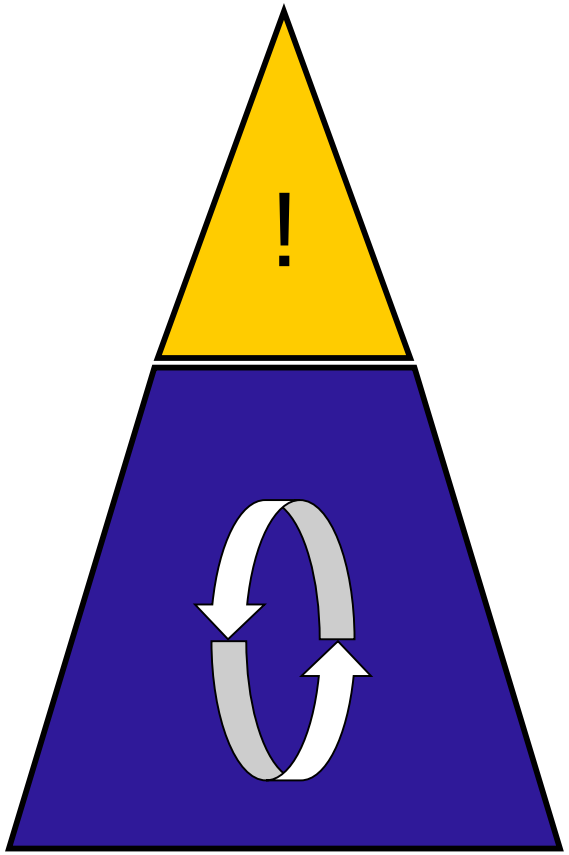
  - report and stop
  - Fix error
    - ECC error: Reconfigure frame
    - CRC error: Reconfigure device
  - Fix and restart continuous readback



# Recap

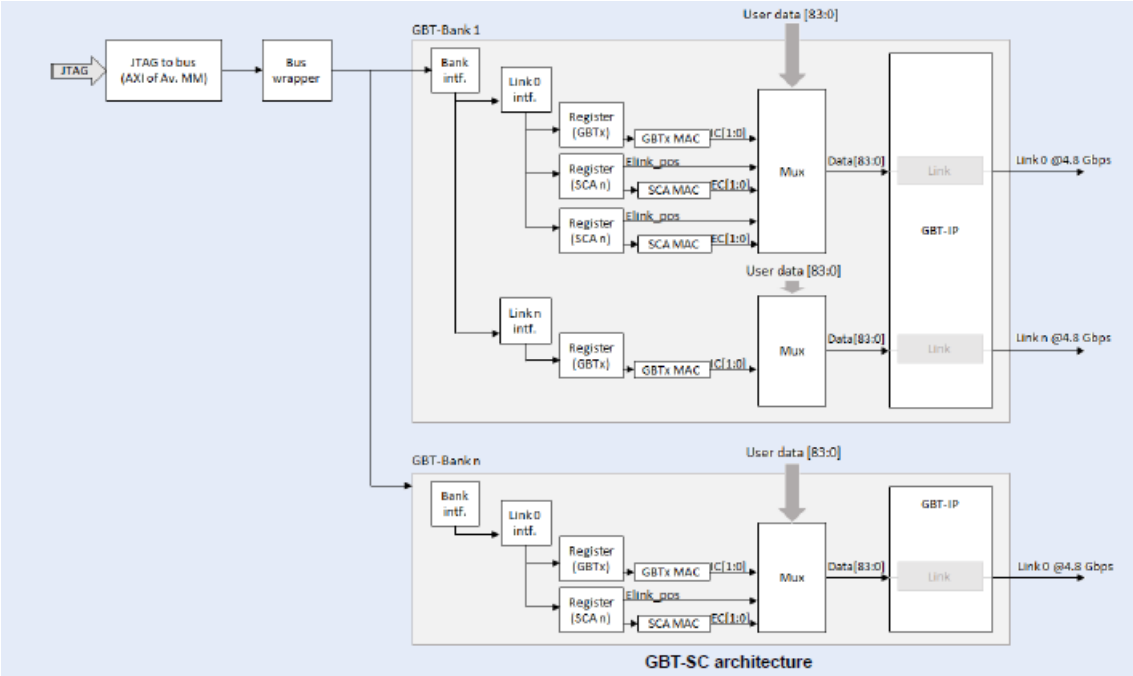
Hybrid scrubbing architecture

- Upper layer
  - Triggered
  - Event-driven Frame reconfiguration
  - Watchdog
  - Logging
  - Configuration management
- Lower layer
  - Running continuously
  - Single-bit upset correction
  - Multi-bit upset detection



# Current State

- **Channel layer development in collaboration with CERN BE-Group**
- **System-level approach will be developed together**



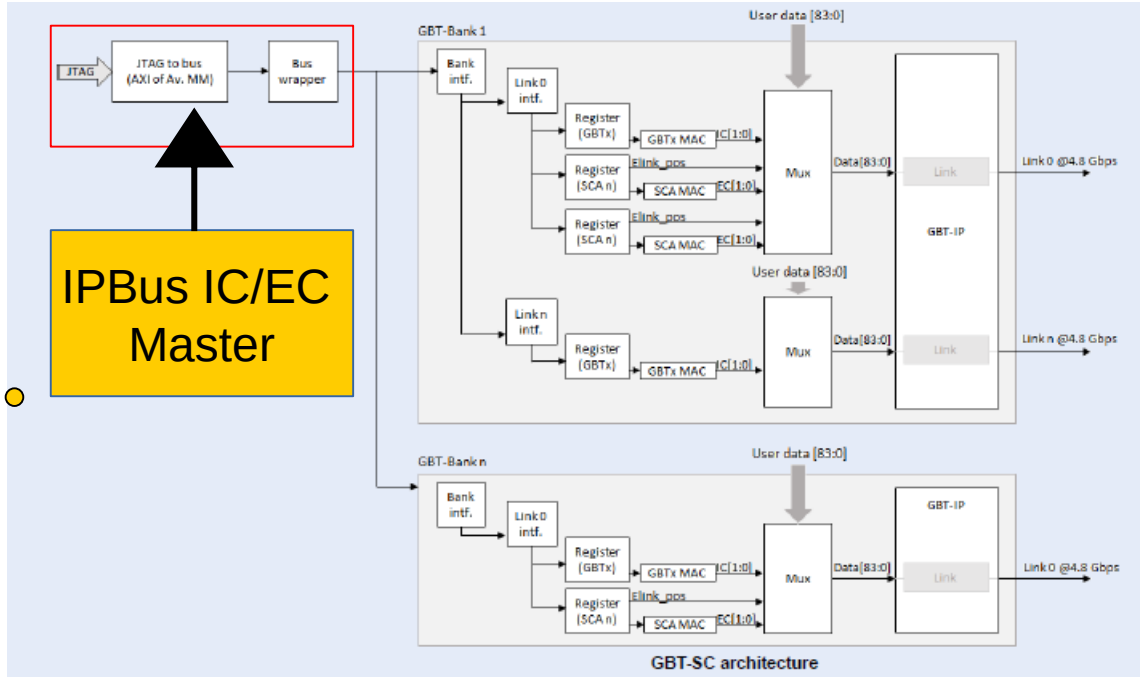

From: Status update and future plans for the GBT-FPGA project at CERN, J. Mendez, S. Baron, M. Barros Marin, ACES 2016 , CERN

# Current State

- **JTAG-to-AXI bus available from Xilinx (Avalon-MM from Altera)**
- **Needs to be adapted and integrated into IPBus architecture for CBM**

IPBus Back-End

IPBus IC/EC Master

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# The Lab Setup

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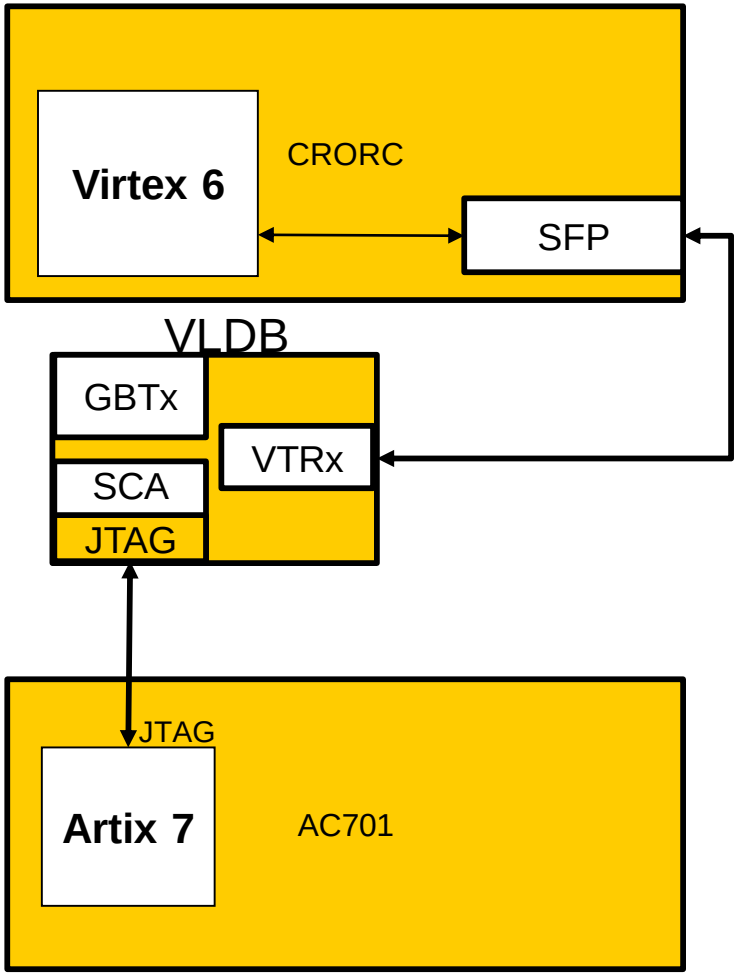
- External power supply
- Level converter for JTAG
- Development: KC705 as downstream board for slow control
- Testing: AC701 as Target board for JTAG programming



# Summary

- **FPGA needs soft error mitigation techniques to operate in proximity of the detector**
- **Soft error mitigation concept is validated**
- **Concept is being migrated to GBT-SCA-based chain**
- **Script-based Configuration Management Unit will be used in future beam test for implemented validation**

# Thank you!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Bundesministerium
für Bildung
und Forschung
05P12RFFCM


## Sources

•GBT-SCA User Manual V 8.0
•GBT-FPGA User Guide V 1.4
•Status update and future plans for the GBT-FPGA project at CERN, J. Mendez, S. Baron, M. Barros Marin, ACES 2016 , CERN

## Acknowledgements

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