# The Common GBTX Based Prototype Readout Board for CBM


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*for the CBM Collaboration*


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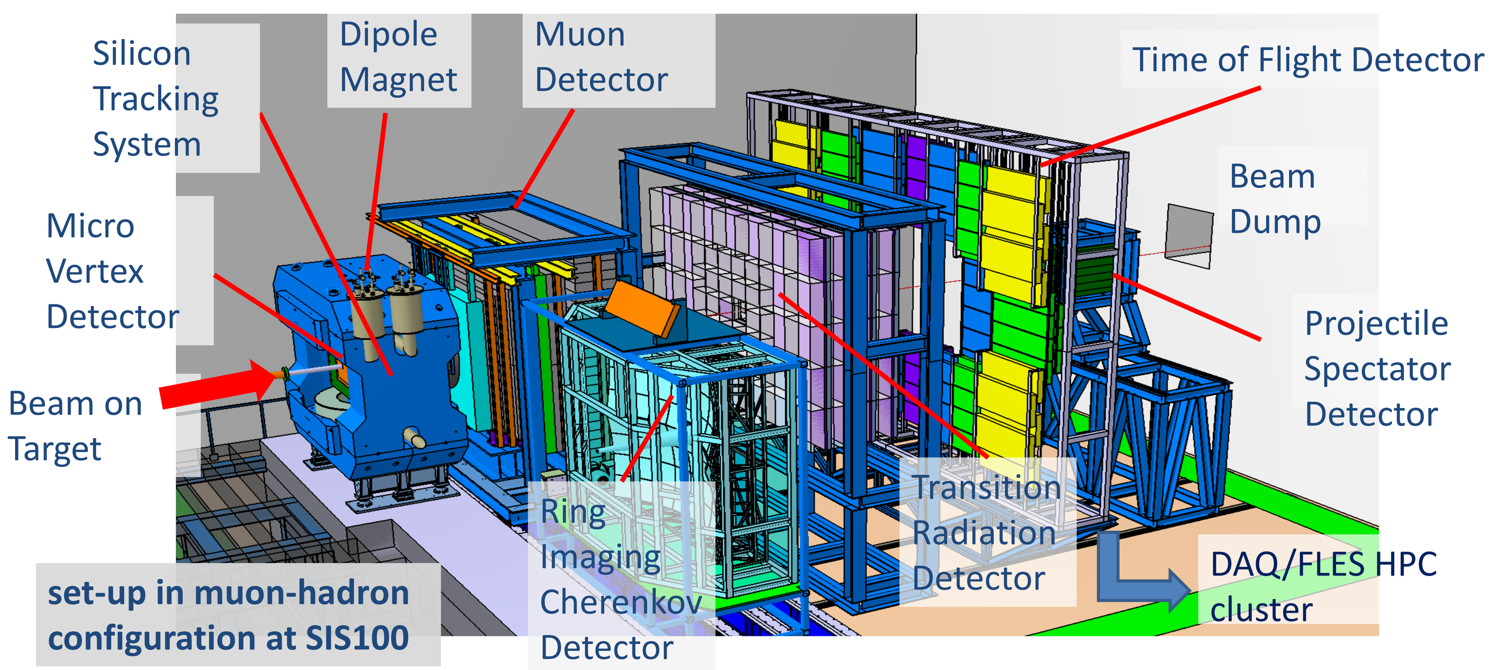
## The Compressed Baryonic Matter (CBM) experiment at FAIR



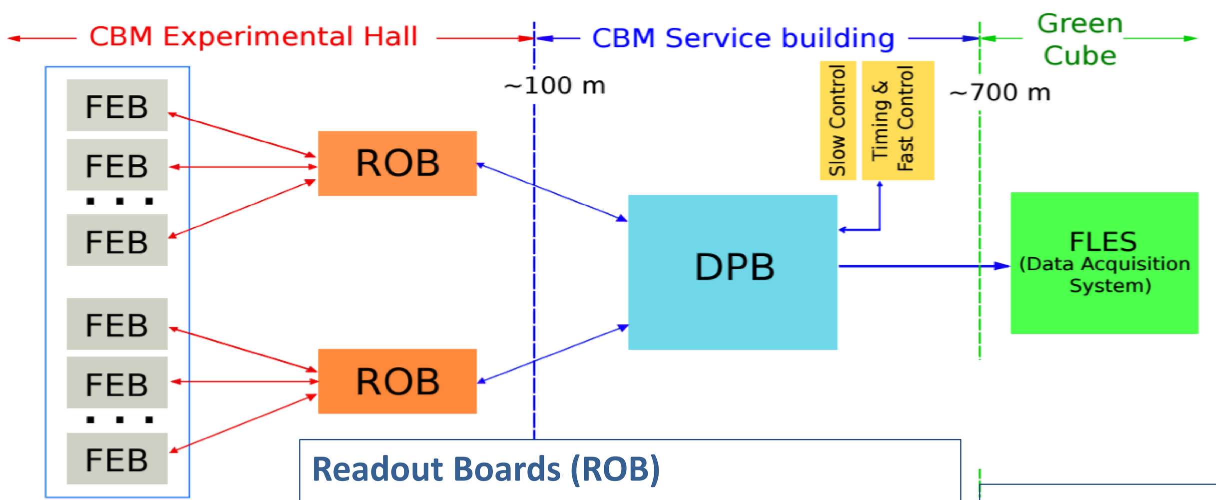

### Physics aim

- Exploration of the QCD phase diagram at high net baryon densities and moderate temperatures at FAIR SIS100:
  - 2÷11 GeV/nucleon / $\sqrt{s_{NN}}$ = 2.7÷4.9 GeV,
  - protons up to 29 GeV

### Challenges

- $10^5$ - $10^7$ Au+Au reactions/sec
- determination of displaced vertices (σ ≈ 50 μm)
- fast and radiation hard detectors
- self triggering frontend electronics
- free-streaming readout system
- high speed data acquisition and high performance computer farm for online event selection
- 4-D event reconstruction

## The CBM Readout Scheme




**Frontend Boards (FEB)**
*detector specific* functionality and designs of ASICs and boards

Integrated with or located close to detector elements

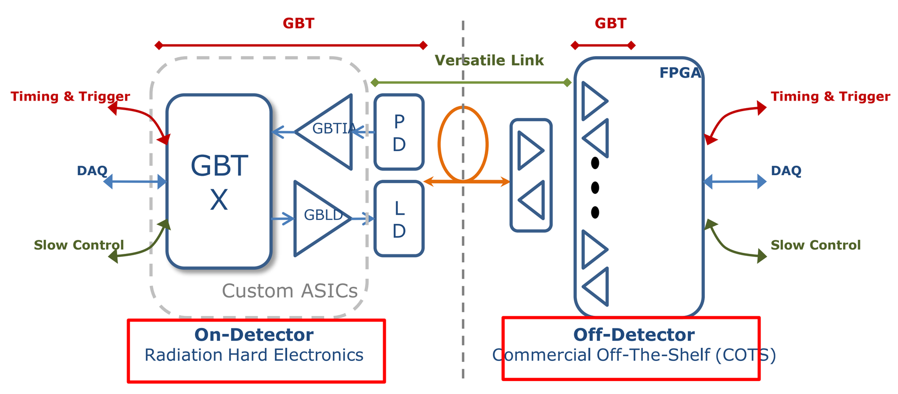
**Readout Boards (ROB)**
*Similar functionality for all systems*
- ***data aggregation of*** up to 30000? FEB electrical links
- data readout: ***optical readout interface***
- FE ASIC control path
- clock distribution and synchronization

→ *CERN GBTX / Versatile Link*

**Data Processing Board (DPB)**
CBM *common hardware platform*:
- FPGA based data formatting and preprocessing
- timing and control interfaces
- interface to FLES (FLIB)
- in CBM building (surface)

## CERN GBT and Versatile Link Components

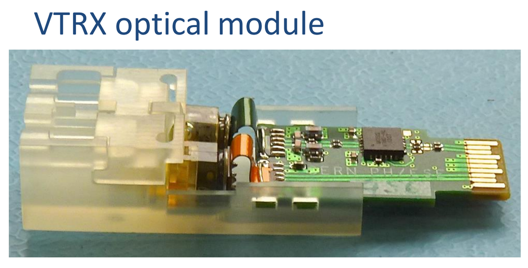
### GBTX and Versatile Link Concept




Two CERN projects to provide radiation hard On-Detector Electronics:
**GBTX ASIC** – GigaBit Transceiver
**GBT-SCA ASIC** - Slow Control Adapter
**VTRX/VTTX** – Versatile Link Transceiver and Twin Transmitter
**GBT IP:** e.g. FGPA implementation of GBT transceiver, SLVS receiver, driver, e-Link port adapter,

GBTX ASIC

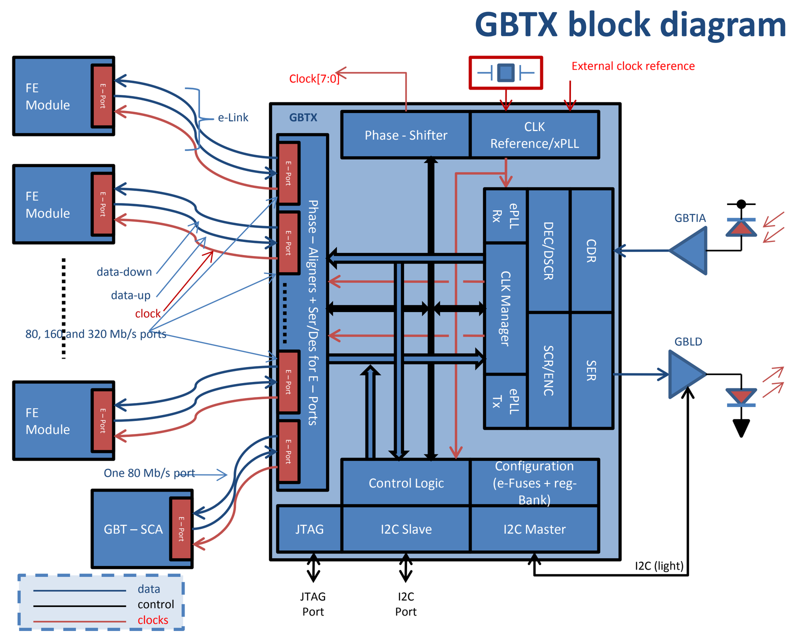
VTRX optical module



### GBTx

- **3.2 Gbps** user bandwidth ( GBT frame mode)
  - 80 bit payload per GBT frame at f_LHC = 40.0798 MHz
- **40/20/10** differential electrical frontend links (SLVS "**E-Links**") at **80/160/320 Mbps** each
  - IN/OUT/CLK
- Uplink: alternative frame mode (widebus) without **forward error correction** (FEC)
  - payload: 112bit/widebus frame → **4.48 Gbps**
- **phase adjustable user clocks**:
  - 320/160/80/40 MHz; 50ps phase adjustment

GBTX block diagram

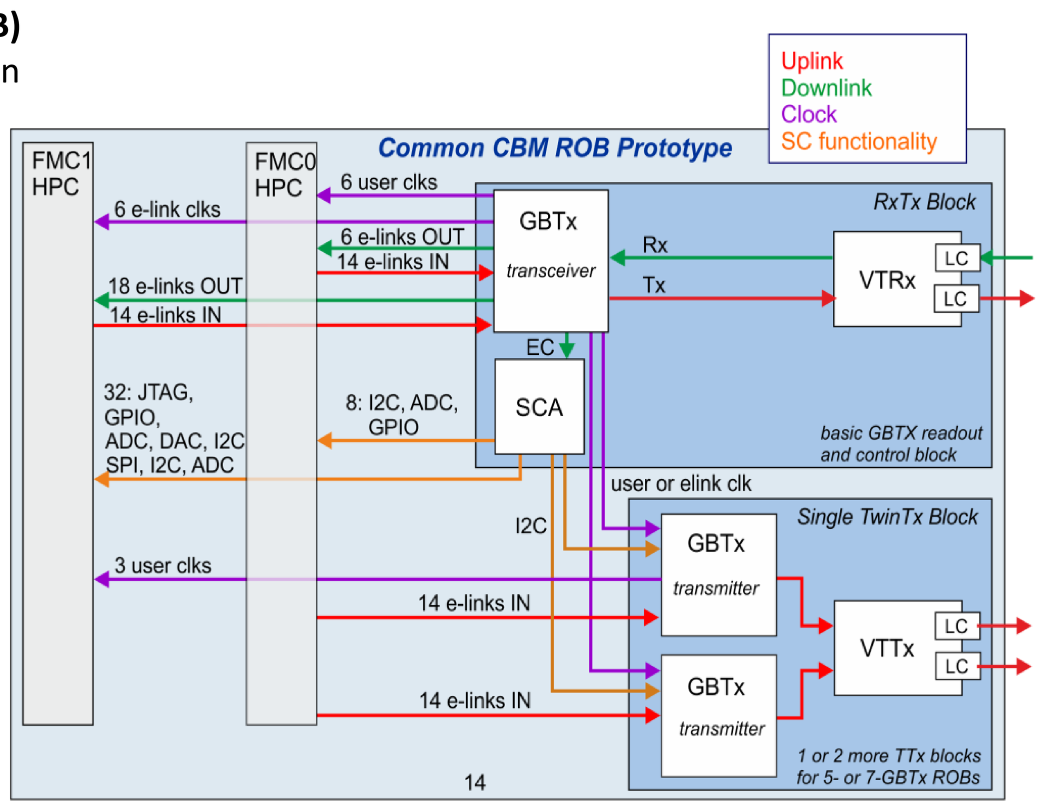


## CBM Common Readout Board Concept & Features

**Common CBM prototype Readout Board (CROB)**
for prototyping of all GBT based readout chains in CBM

**Full** GBTx, SCA and Versatile Link **functionality** required for readout and control of all participating subsystems

**3 GBTx ASICs**
connect up to 40 frontend ASICs at 320 Mbps:
hit readout, control responses
6 x Clk and downlink for control
alt: 24 x bidirectional link at 80Mbps ( single GBTX)
1 Optical Transceiver (**VTRx**) and
1 Twin Transmitter (**VTTx**)
3 optical uplinks each at 4.48 Gbps
1 optical downlink at 3.2 Gbps for control
1 GBT **SCA**
I2C interface for control of slave GBTx
additional multi purpose SCA functionality

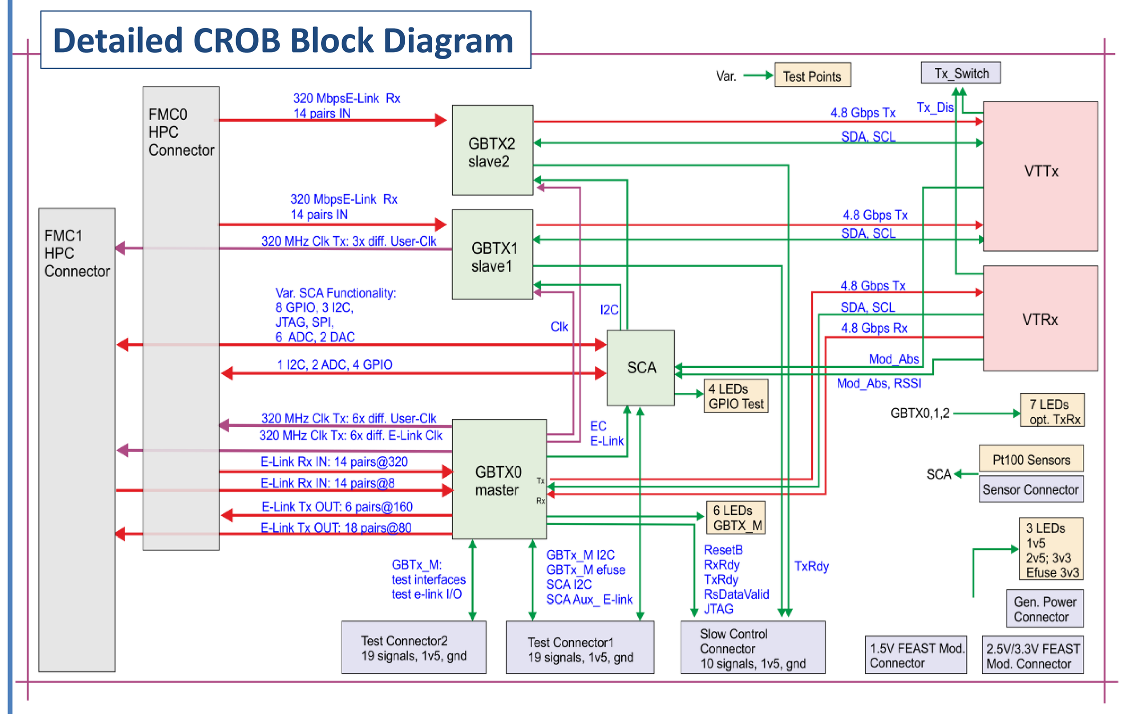



**FMC connectors** with **frontend connectivity**
→ flexible connection of various FEE prototypes
each system develops new or reuses existing FMC mezzanine board as FEE interface
*FMC0* – sufficient for STS, MUCH, TRD
subset of downlinks, clocks; all 320MHz E-Up-Links
small subset of SCA functionality
*FMC1* - additional 80MHz E-Links (TOF); more SCA

Misc features:
- Optional I2C configuration, compatible with CERN USBtoI2C dongle
- various external configuration settings
- Device test features available
- "slow control" connector with resets, link status (RxRdy, TxRdy's, TxDataValid), power control ( FEAST enable, power good)
- Powering: 2 FEAST_MP (1.5V and 2.5/3.3V)

## CROB Design

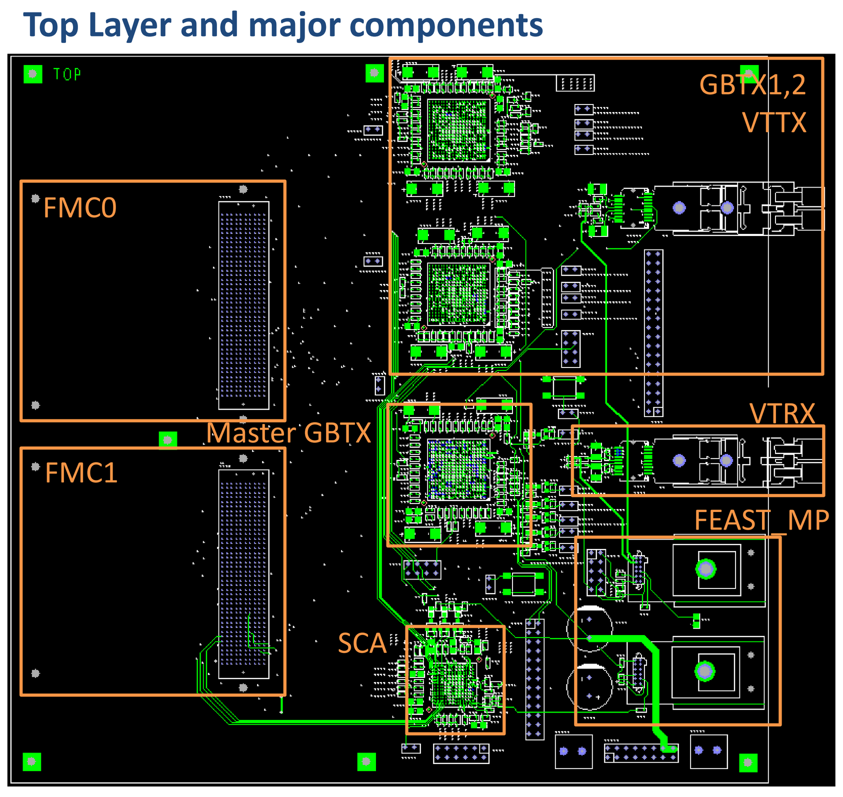
### Detailed CROB Block Diagram



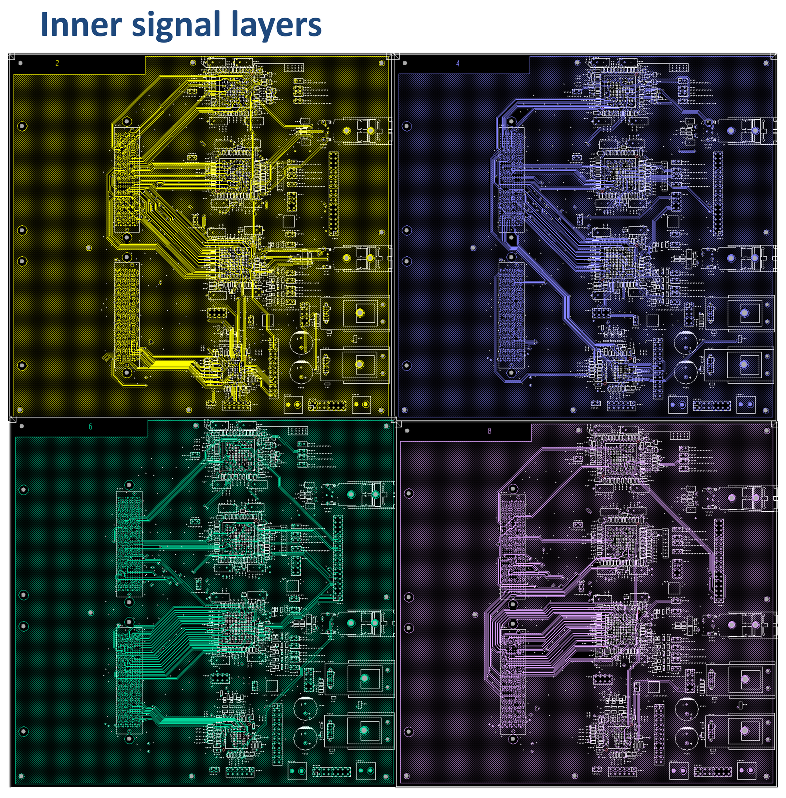
### Features and Status

- Design ready (D. Gottschalk, PI Heidelberg)
  - schematics and layout done
  - final review ongoibng
- Features
  - 12 layer
  - 100um /125um
- Production
  - submit PCB in next few weeks
  - assembly of first prototypes at GSI EE
- 40.000MHz CBM-GBTX available for assembly
- Initial boards
  - functional testing
  - Preparation of eTOF setup

### Top Layer and major components




### Inner signal layers



## CROB Usage in CBM

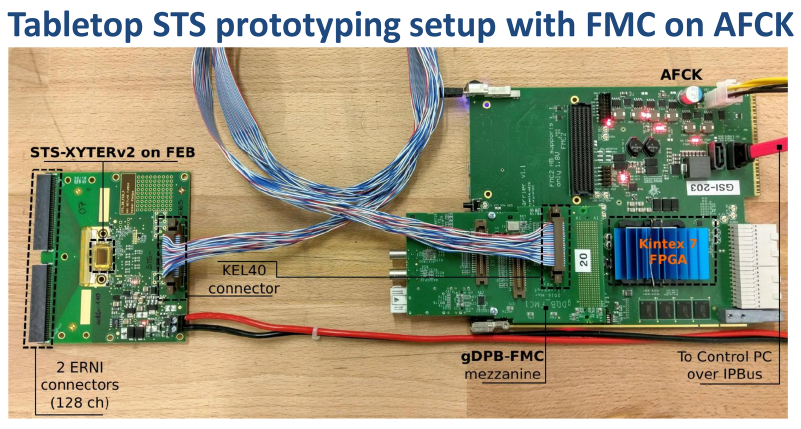
### Systems

| | STS | MUCH (Station 1&2) | TOF | TRD |
|---|---|---|---|---|
| **Frontend ASIC** | **STS**/MUCH-XYTER 128 channels *AGH Cracow* | STS/**MUCH**-XYTER 128 channels *AGH Cracow* | GET4 4 channels *GSI* | SPADIC 32 channel *ZITI Univ. Heidelberg* |
| **Readout** | 1 to 5 E-Links (configurable ) at 320MHz | 2 links at 320MHz | 1 E-Link (compatible) at 80 MHz | 2 E-Links at 320MHz |
| **Configur-ation & SC & FC** | DL: dedicated E-Link shared by ASICs UL: all E-Links, shared with data | | DL: control UL: control in data stream | DL: shared E-Link UL: single E-Link shared with data |
| **Clock** | Phase adjustable clock@160MHz | | Dedicated distribution of 160MHz clock(tbc) | Phase adjust. Clk at 160MHz |
| **Channels** | 1.8 million | 249k | 100k | 280k |
| | ROB-3 | ROB-3 | ROB-1 | ROB-3, ROB-5 |

### Applications

- Prototype full readout chains for STS, MUCH, TRD, TOF from 2017 on
  - Modular setups using FMC on CROB or AFCK
  - Development of full control functionality
  - Readout of medium sized detector setups
- Readout of eTOF (FAIR Phase0 experiment: BESII at START@RHIC) in 2018-20
  - 3 full TOF modules ( approx. 10% of CBM)
- Readout of miniCBM: full system CBM setup at SIS18@GSI in 2018-21
  - Mini versions of all subsystems

Tabletop STS prototyping setup with FMC on AFCK




## From CROB to Detector Specific ROBs

### Modifications for System ROBs

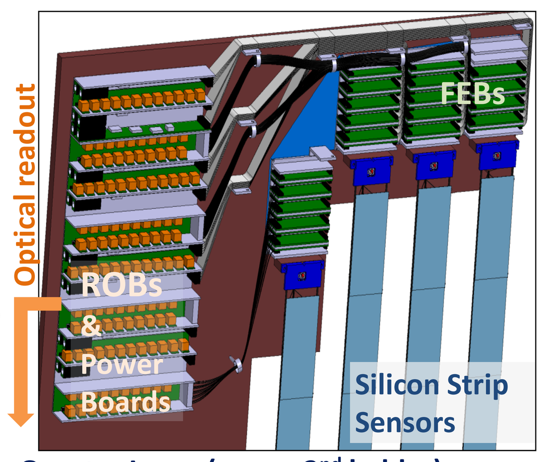
- FMC → system specific FE connectors
  - Reduced PCB space
- required subset of E-Links
  - 24 SLVS pairs instead of 64 for most systems
  - simplified GBTx layout
- required subset of GBTX
  - Identical for STS, MUCH, TRD ROB-3
  - Only master GBTX for TOF
  - Add 2xGBTX+VTTx for TRD-ROB-5
- Remove misc. test and configuration functionality

### Example: STS-ROB

**Space**
ROB size: approx. 83mm between side cooling plates of adjacent units

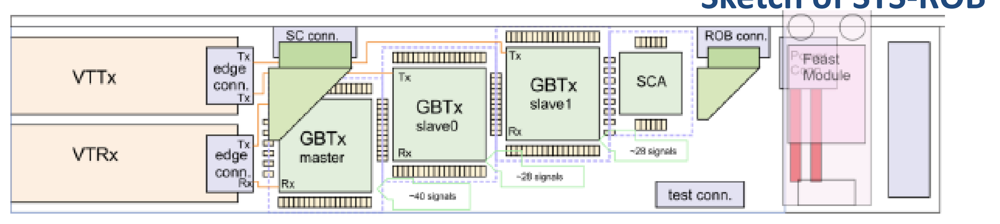
**Cooling**
sensors operated at <= -5° Celsius

**Powering Scheme**
FEBs operated at individual sensor bias potentials
→ AC coupling of FEB-ROB e-links




Quarter Layer ( every 2nd ladder)

Sketch of STS-ROB





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- J. Lehnert et al., *GBT based readout in the CBM experiment,* proceedings of TWEPP 2016, *JINST*