Test of the STS-XYTER2 frontend ASIC for the CBM Silicon Tracking System

Adrian Rodriguez Rodriguez for the CBM Collaboration



Muenster, March 31st, 2017



- $1 \rightarrow$ Introduction to the CBM Silicon Tracking System
- 2 → STS-XYTER v2 first tests summary.
- $3 \rightarrow$ Develop and test an ADC trim calibration procedure.
- 4 \rightarrow Test beam results evaluating SEU in the STS-XYTERv2 at COSY beam time.
- 5 \rightarrow Towards noise studies with the STS-XYTERv2.
- $6 \rightarrow$ Summary & outlook

The Compressed Baryonic Matter experiment (CBM) at FAIR

Exploring the QCD phase diagram at high net baryon densities



- \rightarrow 10⁵-10⁷ A+A collisions/s
- \rightarrow Fast and radiation hard detectors
- \rightarrow Self-triggering electronics
- \rightarrow 4D event reconstruction.

Wednesday, March 29th, 2017, 16:45-17:15, HK30.1 The Compressed Baryonic Matter experiment at FAIR

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The Silicon Tracking System (STS) of the CBM experiment





Requirements:

- → High detection efficiency.
- \rightarrow Spatial hit resolution: 25 μ m
- \rightarrow Momentum resolution: <2%
- \rightarrow Tracking up to 1000 charged particles/collision.
- \rightarrow Low material budget 0.3%-1.0% $\rm X_{o}$ per station.
- \rightarrow Radiation hard sensors: 1 x 10¹⁴ 1 MeV n_{eq}/cm²
- \rightarrow lonizing dose at the electronics place ${\sim}200$ krad/yr.
- \rightarrow Heat dissipation \sim 40 kW.

Design:

- \rightarrow 8 tracking stations inside 1T magnetic field.
- → Geometrical acceptance: $2.5^{\circ} \leq \theta \leq 25^{\circ}$
- \rightarrow Based on \sim 900 double-sided Si sensors with 4 different sizes:
 - 2x6 cm², 4x6 cm², 6x6 cm², 12x6 cm².
 - 7.5° stereo-angle for the p-side strips
- \rightarrow 1.8 millions of channels::~14 000 ASICs.
- \rightarrow Built as a functional module:
 - 1 Si sensor + microcables + 2 FEB.
 - 1 FEB carry 8 ASICs (1024 channels).



Olga Bertini for the CBM collaboration

The **STS** readout chain



- → Front End Boards: Part of a functional module; it carries 8 STS-XYTER ASIC/FEB
- \rightarrow Read Out Board: Based on CERN-GBTx and Versatile links components.

Tuesday, March 28th, 2017, Poster session The common GBTx based prototype board for CBM

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→ Data Processing Board: FPGA based, interface for Timing and Control and data preprocessing

The **STS-XYTER** ASIC

STS+X,Y coordinate, Time and Energy Resolution

Low power, self triggering ASIC dedicated for reading out the double-sided Si sensors.

STS-XYTERv2 available since fall 2016 Designed by AGH University of Science and Technology Cracow, Poland. (Scziegiel, Kasinski et al)



Features:

- \rightarrow 128 channels + 2 test channels.
- \rightarrow CSA with variable gain (STS/MUCh detectors)
- \rightarrow Time resolution: ~ 5 ns.
- \rightarrow 14 bit Time stamp.
- \rightarrow 5 bit in-channel flash ADC.
- \rightarrow ADC linearity range up to 15 fC.
- \rightarrow Radiation hard layout.
- \rightarrow Power consumption: <10 mW/ch
- \rightarrow Digital backend compatible with the CERN-GBTx.





The STS-XYTERv2 test setup at GSI



Test setup estblished at GSI and 3 other research institutes: AGH, Poland; VECC, India; JINR, Russia

Digital backend implemented in the Kintex7 FPGA. Firmware developed by W. Zabolotny (Warsaw University)

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ASIC functionalities test:

- \rightarrow Links synchronization & masking.
- \rightarrow ASIC addressing.
- → Register access R/W.
- \rightarrow Hit generation by using test modes implemented in the ASIC.
- \rightarrow ADC trimming calibration.
- \rightarrow Single Event Upset (SEU) tests at COSY beam time.

STS-XYTERv2 tests

Evaluating ADC by acquisition of S-curves with dedicated counters using the analog test-pulse generator .



STS-XYTERv2 tests

Evaluating ADC by acquisition of S-curves with dedicated counters using the analog test-pulse generator .

Number of counts Discriminator threshold [a.u.] Not calibrated ADC Calibrated ADC Trim correct. from typical value 200 220 240 Pulse amplitude [au] Discriminator number ADC linearity (before and after calibration) S-curves from a typical calibrated channel Blue curve \rightarrow typical trim value (128)

Pulse amplitude scan in the range 50-220 au

Redo process with external pulser

STS-XYTERv2 SEU test

Two different architectures:

→ DICE cells:31744 bits (ADC trim DACs)
→ Flip-flops: 47616 bits (ADC disc counters)

25°

 \rightarrow 3 ASICs under test.



Beam features:

- \rightarrow 1.6 Gev/c momentum (Info from AT).
- \rightarrow 18 s duty cycle.
- \rightarrow 4 5 s spill length.
- \rightarrow Average intensity per spill > 4 x 10⁹ p
- \rightarrow Effective irradiation time: \sim 45 hours.
- \rightarrow Integral intensity: ~ 3.7 x 10¹³ p.

Beam monitoring:

- \rightarrow lonization chamber (IC) for beam intensity.
- \rightarrow Gafchromic films for beam position and beam profile.





STS-XYTERv2 SEU test

SEU in DICE cells (8 bits).



Findings: → Improvement in the radiation hardness of the DICE cells architecture relative to the STS-XYTERv1 as expected.
→ Hint for further enhancement (cells 4 to 7)

Sensor readout setup using the STS-XYTERv2



INSIDE SHIELDING BOX

 \rightarrow Si sensor: 64 connected strips.

→ STS-XYTERv2 ASIC in prototype FEB (80 connected channels)



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Summary and Outlook

- → Experimental setup to evaluate STS-XYTER ASIC functionalities have been set up at GSI and other research institutes (AGH, Poland, VECC, India, JINR, Russia)
- \rightarrow ADC trim calibration procedure has been developed and tested.
- \rightarrow Successful test-beam campaign at COSY in February 2017.
 - ASIC has shown an improvement in terms of SEU for the DICE cells architecture.

Towards sensor readout and noise studies with the STS-XYTERv2

- \rightarrow Sensor read out using the STS-XYTER v2.
 - Investigate and reduce noise sources and ground loops contribution.
 - First look into the system noise levels using (6x6 cm² sensor, sensor module).
 - Detector response to radioactive sources.
- → Preparation of a standalone sensor readout for the beam time campaign (May 2017).

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Thanks for your attention!