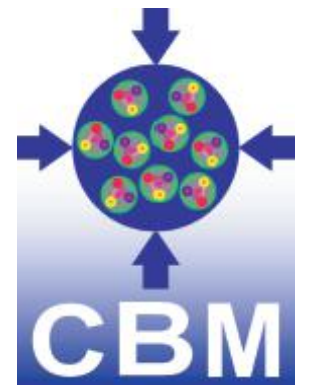




Online data pre-processing for the CBM MVD

Qiyang Li
for the **CBM-MVD Collaboration**

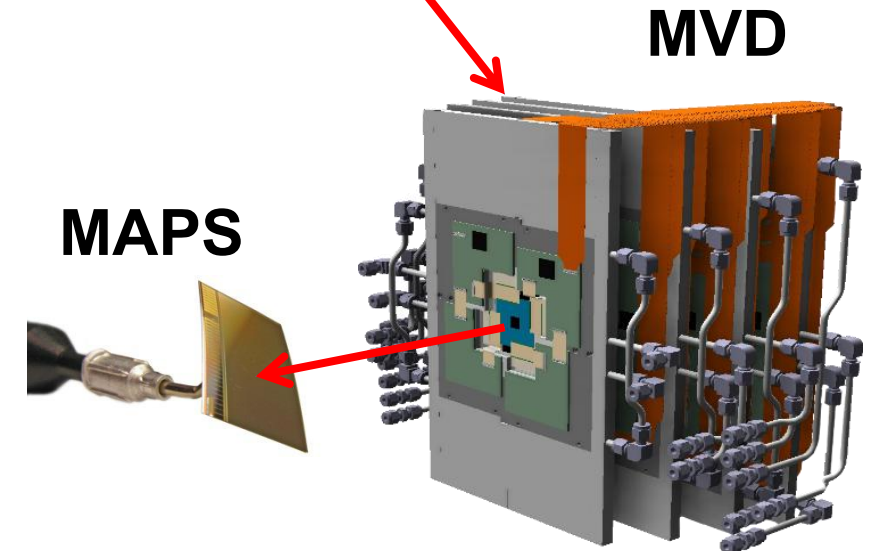
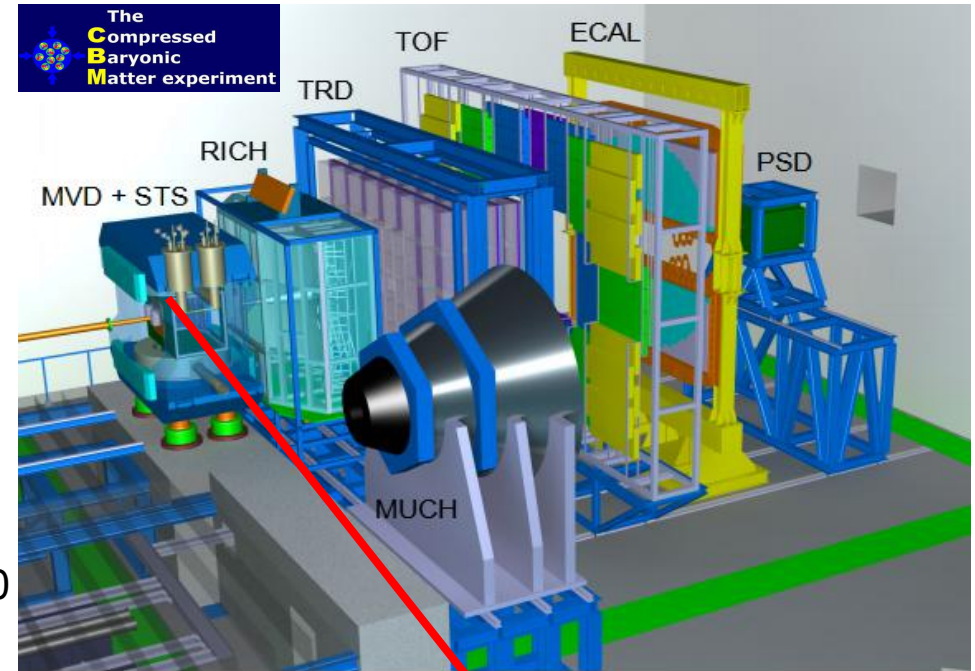


Outline

- ◆ **Strategy and requirements**
- ◆ **Implementation on FPGA**
- ◆ **Results in real time test**
- ◆ **Summary**

Introduction

- ◆ **CBM: high rate experiment**, collision rates of 10^7 Au+Au coll/s, 10^9 p+A coll/s
- ◆ **Micro-Vertex-Detector (MVD)**
Requires high spation resolution: $5\mu\text{m}$, 0.3% X_0
Operates at high particle fluxes (70 MHz/cm^2)
--> High radiation dose
--> High data rate
- ◆ **CMOS Monolithic Pixel Sensors(MAPS)**
are used for the CBM-MVD
MIMOSA-26 is the sensor for the MVD prototype

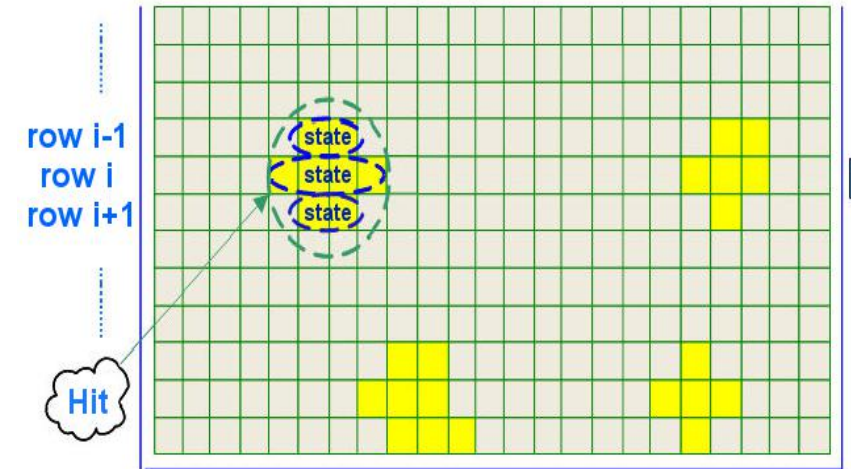


Question and approach

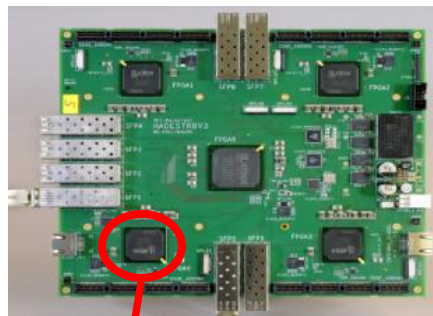
◆ Charge sharing on MAPS

=> One particle hit creates 2-dimensional cluster

=> Cluster finding is needed



Readout Control Board



Raw data



Cluster data



CPU cluster finding

Computer farm: FLES

Clusters



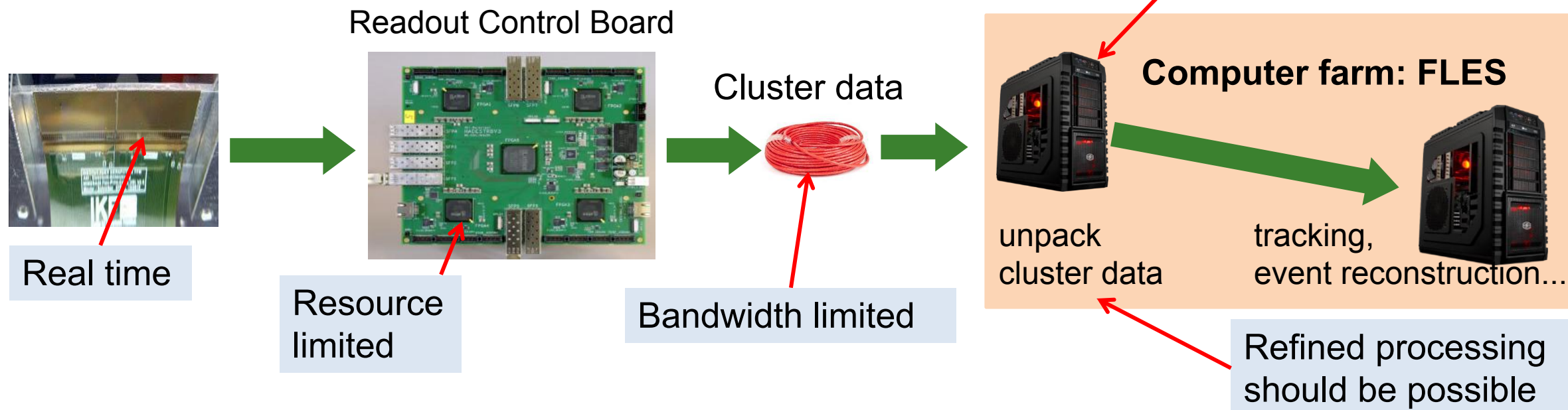
tracking,
event reconstruction...

Benchmark of software (CbmRoot):
uses sizable fraction of the
computing time

**On-chip electronic:
0-compression and
1-dim cluster finding**

**2-dim cluster finding on the FPGA
of MVD-ROC with it's un-used
resource to reduce CPU-time**

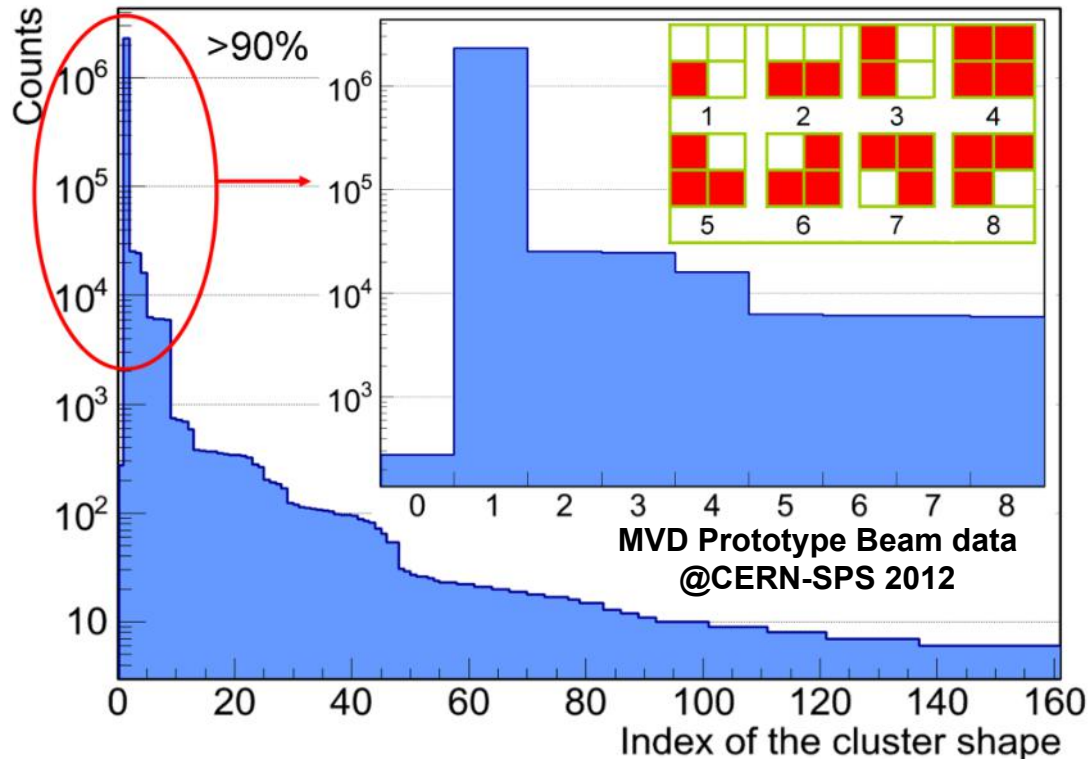
Requirements



Requirements:

- ◆ Real time operation
- ◆ Cluster data encoding must not lose information and be feasible on FPGA
- ◆ Data volume must not be expanded
- ◆ Cluster data decoding must be efficient on CPU

Basic strategy

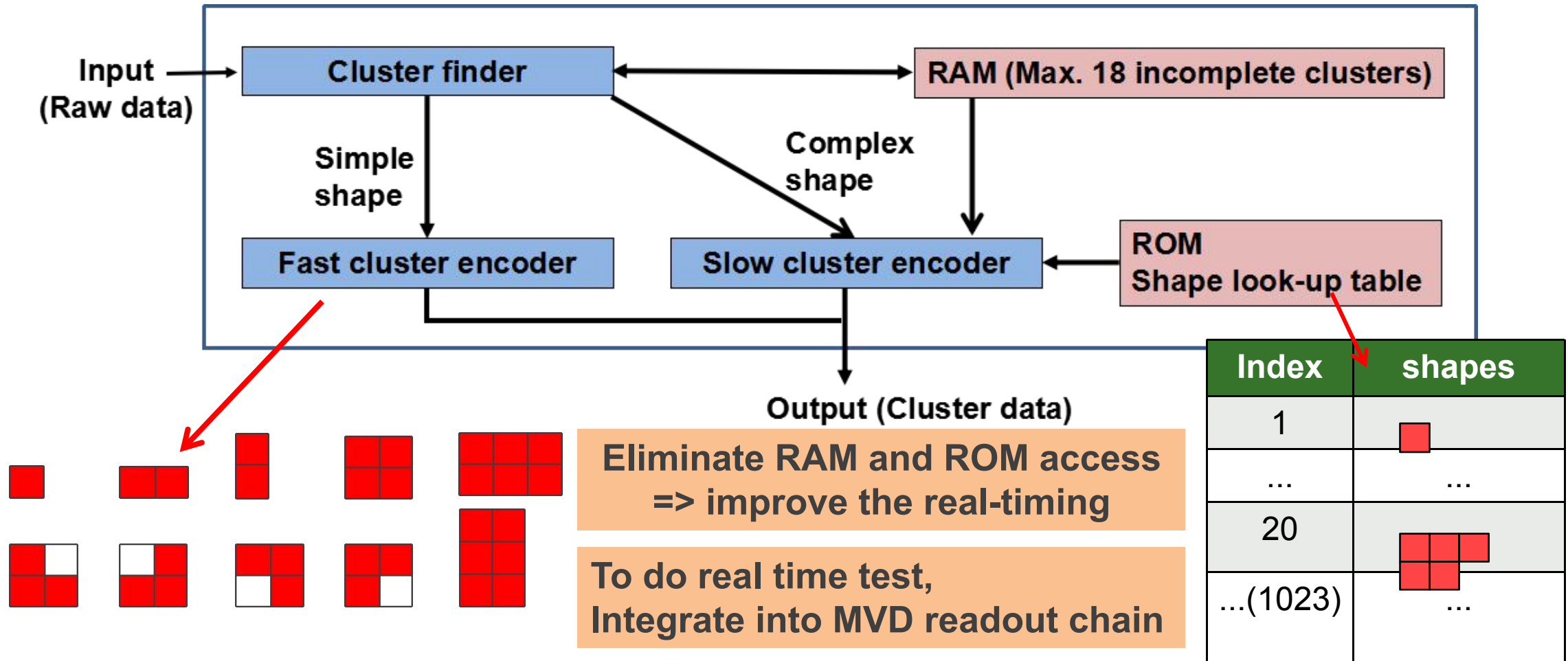


- ◆ **Study the cluster feature based on MVD prototype**
- ◆ **Observation:**
 - Only a limited number of different cluster shapes
- ◆ **Idea:**
 - ◆ Associate an **index** to each cluster shape.
 - ◆ Send cluster index instead of shape information
 - ◆ Decode cluster index with look-up table.
- ◆ **Encoding way:**
 - ◆ 21 bits for cluster position
 - ◆ 10 bits for shape information
 - => 32 bits per cluster is needed

| | | | |
|-----|----------------|------------|----------|
| 31 | Bit(21-30) | Bit(10-20) | Bit(0-9) |
| OVF | Index of Shape | Addr_Col | Addr_Row |

Implementation on FPGA

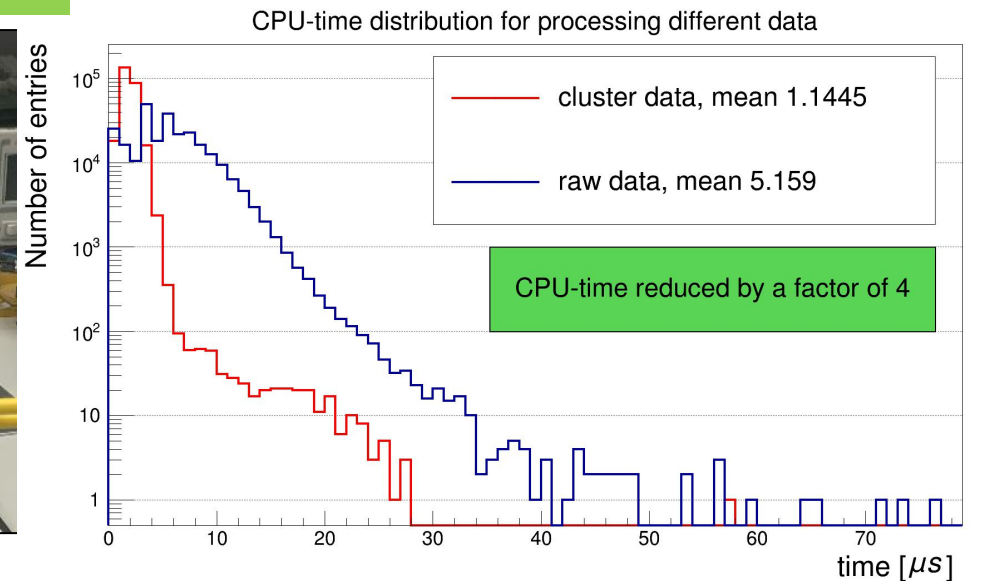
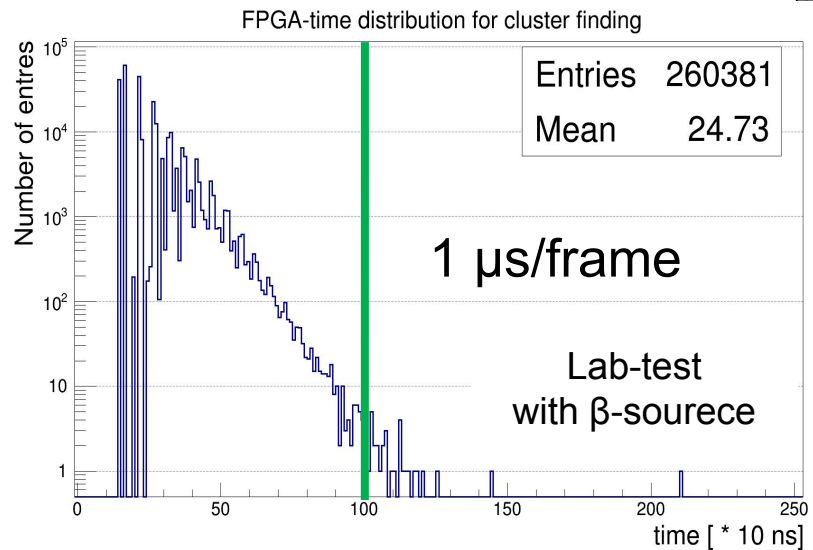
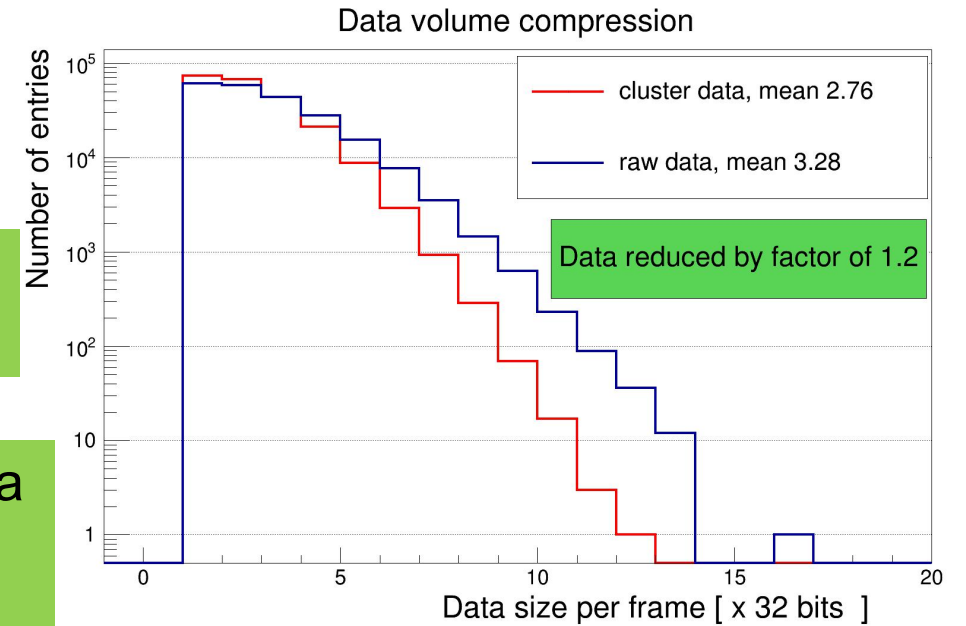
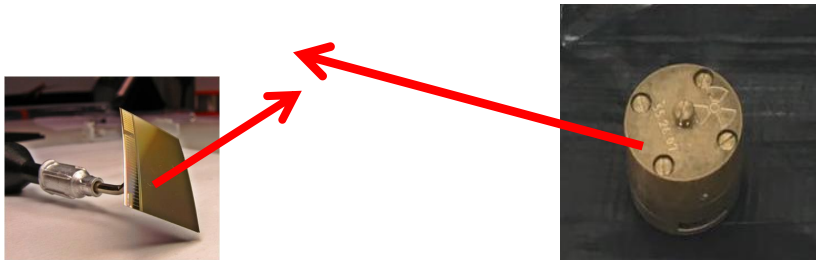
◆ FPGA cluster finding logic structure



Result in Lab test

MIMOSA26,
illuminated with ^{55}Fe

Cluster data vs Raw data
260K frames
No data loss

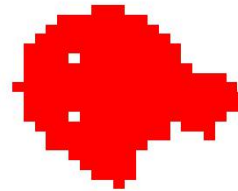


Robustness test with heavy ion experiment data

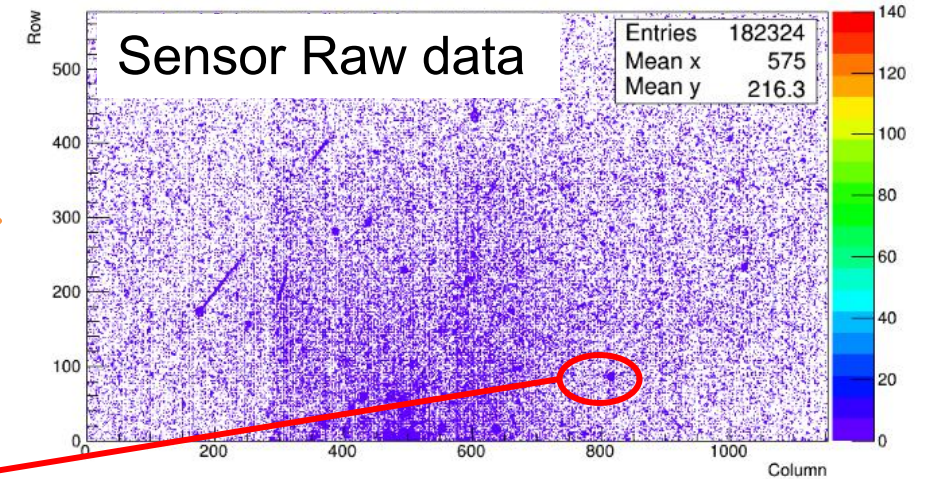


Courtesy NA61/SHINE

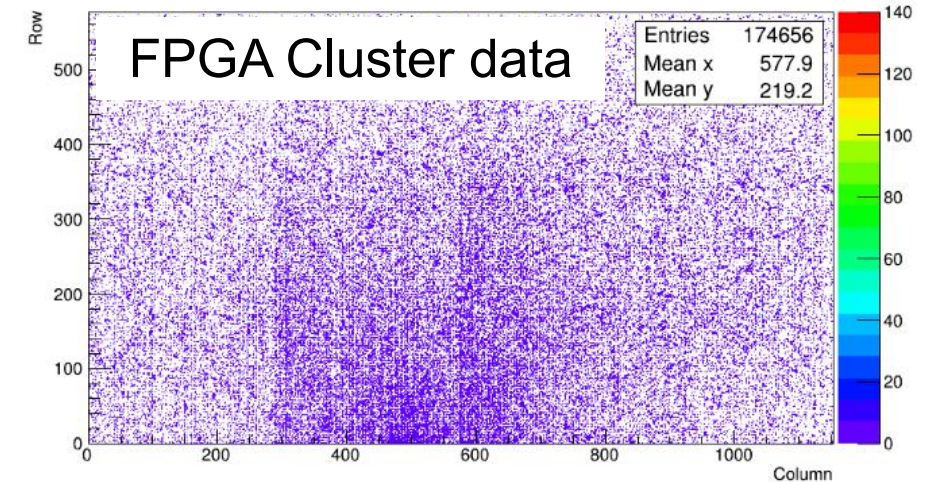
156 AGeV Pb+Pb in 2016



Fired pixel matrix of Sensor_output

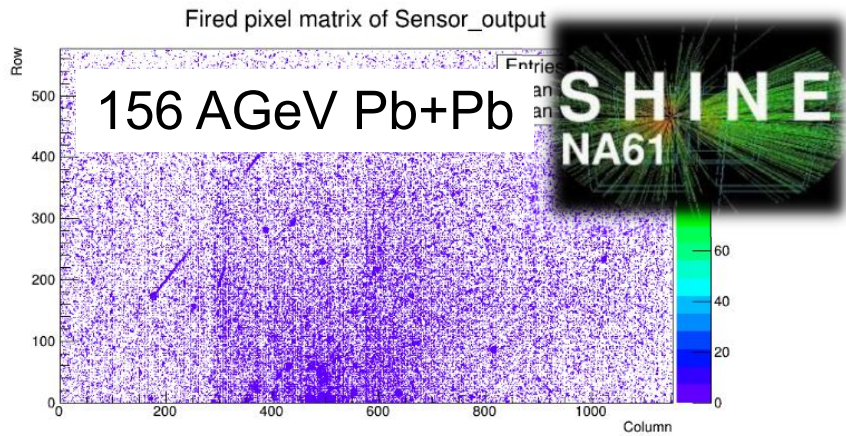


Fired pixel matrix of LimitedCF_VHDL

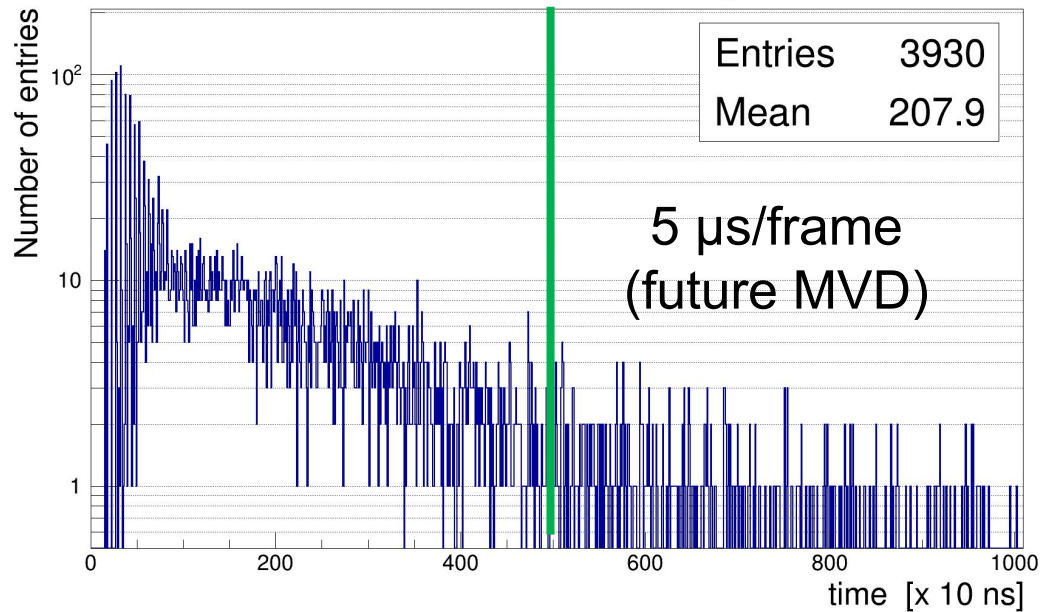


- ◆ 3% data loss in 4K frames
 - ◆ big clusters can not be encoded
 - ◆ broken line, overflow
 - ◆ Background of physics case, acceptable
- ◆ Works reliably

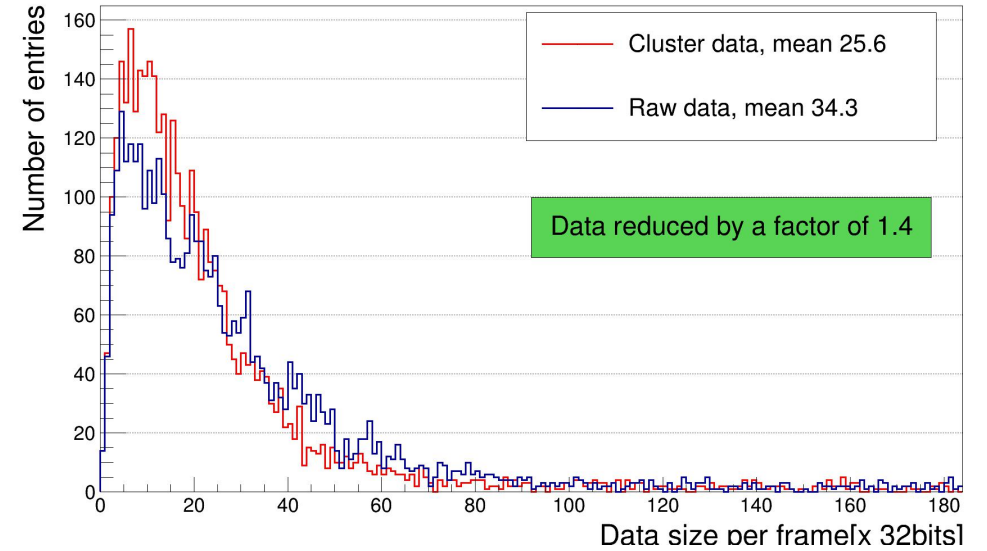
Result in Robustness test



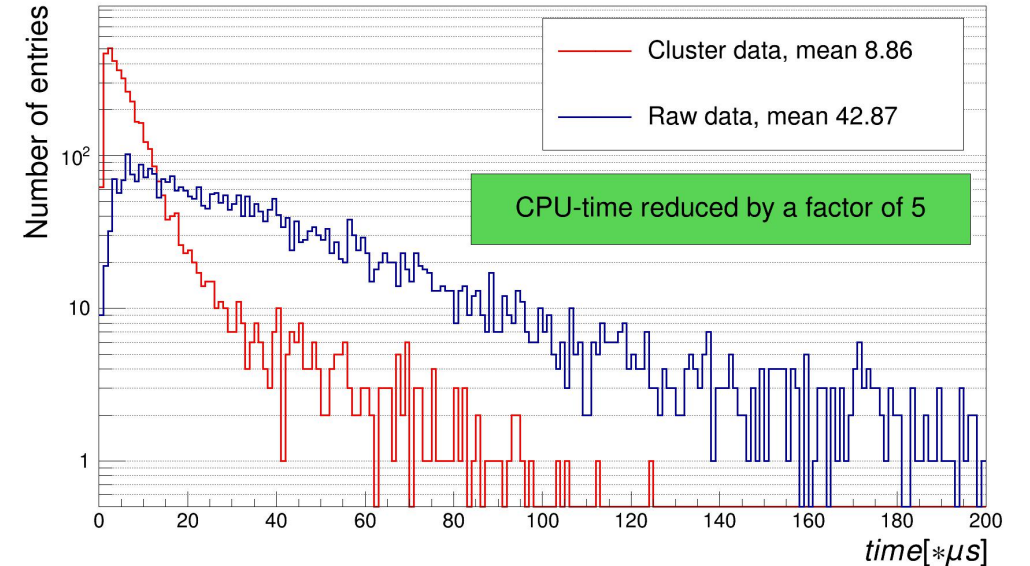
FPGA-time for cluster finding



Data volume compression



CPU time distribution for processing different data



Summary

- ◆ FPGA Cluster finding is designed and implemented in the MVD-ROC
- ◆ Real time is demonstrated by operating with MIMOSA26 in Lab-test
- ◆ The robustness is checked with heavy ion experiment data (NA61/SHINE Pb+Pb)
=> Works reliably, CPU-time reduced ~ 5, Data volume slightly reduced

**Successfully demonstrates the potential and need
of pre-processing the MVD raw data!**

Thank you for your attention!