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DiRich Readout Electronics
for HADES, CBM and PANDA

GOETHE UNIVERSITÄT FRANKFURT AM MAIN

3 similar detectors

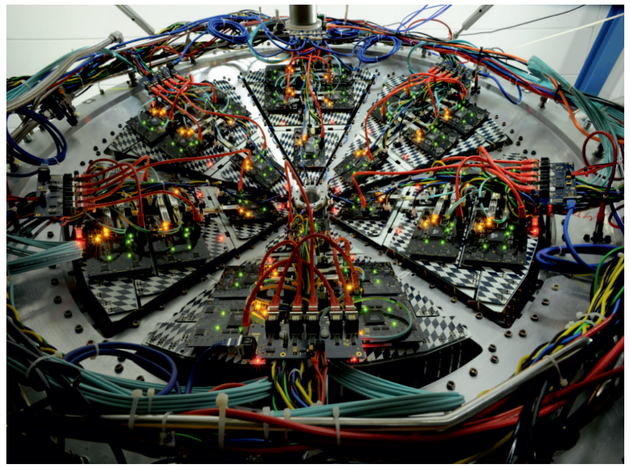
The RICH detectors

HADES RICH

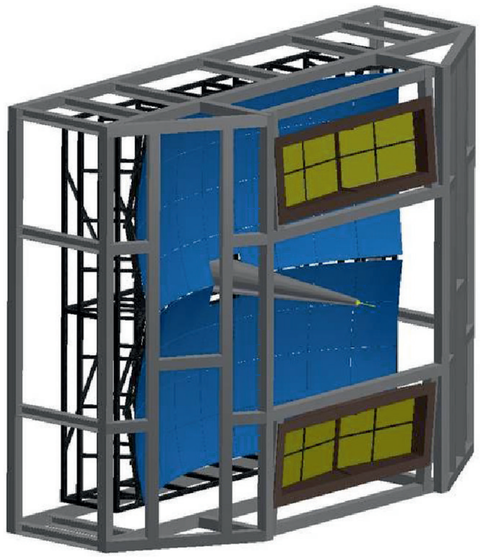
- 1.2 m² detector surface
- 28,000 channels
- CsI cathode to be replaced by PMT

CBM RICH

- 2.8 m² detector surface
- 60,000 channels
- 10 MHz collision rate
- up to 200 GBit/s



The current read-out plane of the HADES RICH with electronics

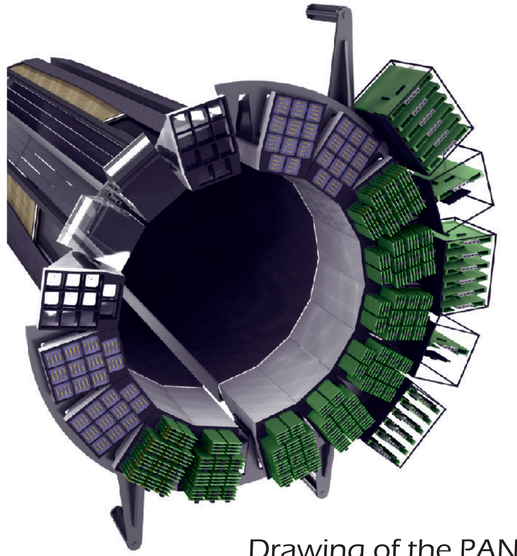


CAD model of the CBM RICH height 5 meter

Panda DIRC

Same scheme is planned for the Panda Barrel DIRC

- MCP-PMT (better timing, magnetic fields, 2x smaller signal)
- 11,000 channels
- similar rates to CBM



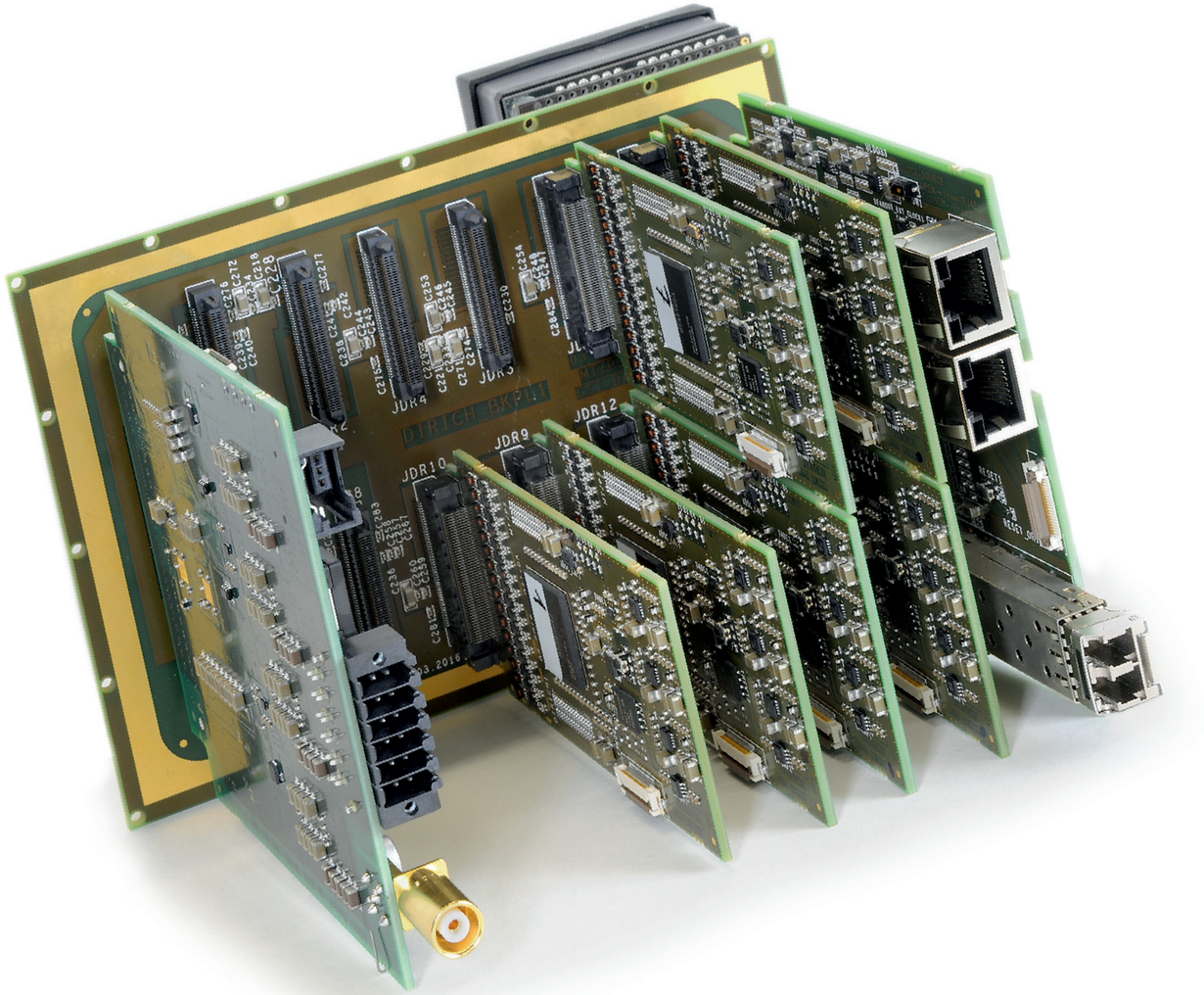
Drawing of the PANDA Barrel DIRC including electronics

Design Ideas

Design Policy

all electronics fit to back of PMTs
small modules for flexibility
use dedicated, discrete amplifiers
in-FPGA time measurement
low power to ease cooling
modular design to separate functions
use space efficiently
as few cables as possible
versatile to fit to all experiments

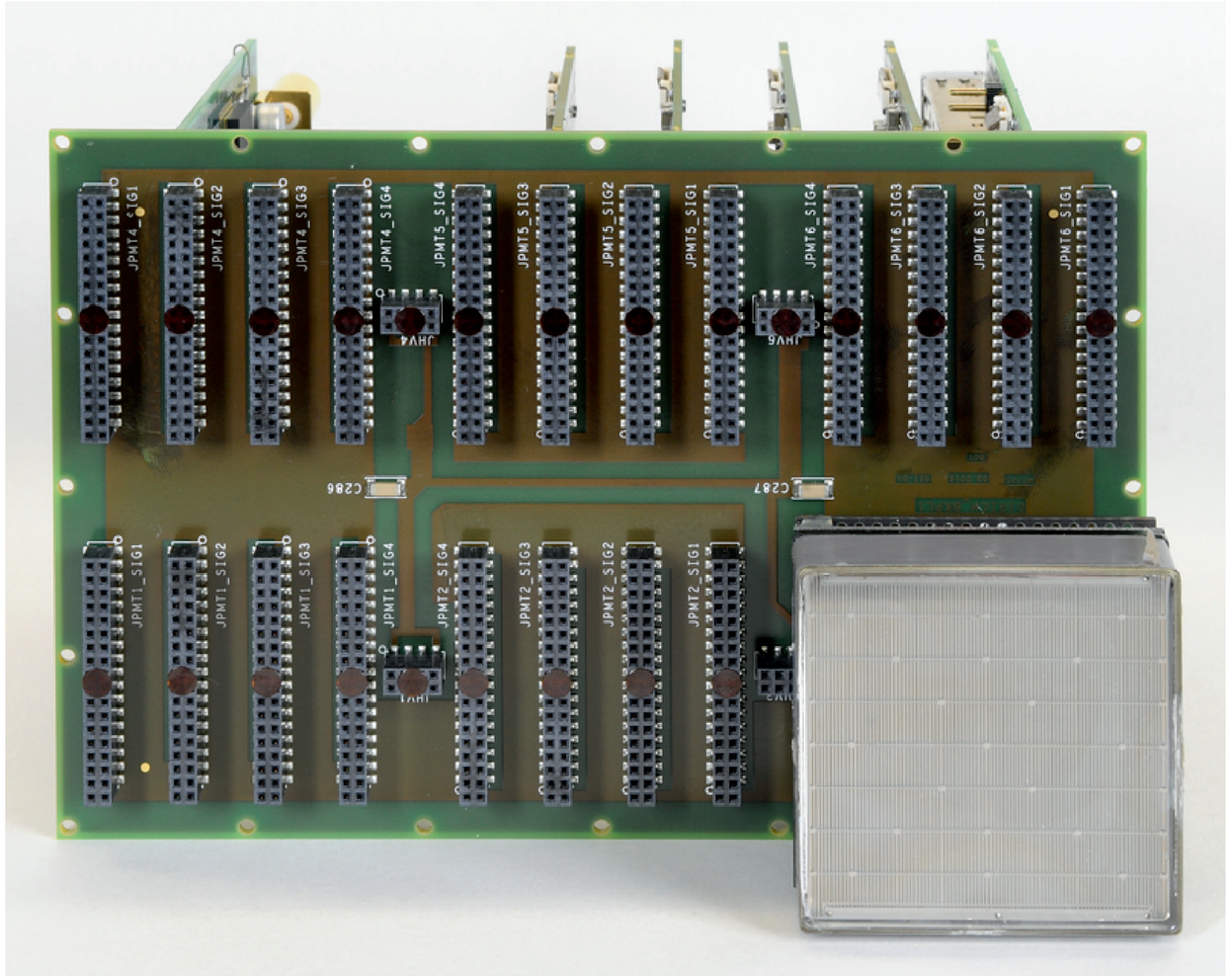
1 solution



Backplane

Combines 6 PMT with all electronics to one read-out module

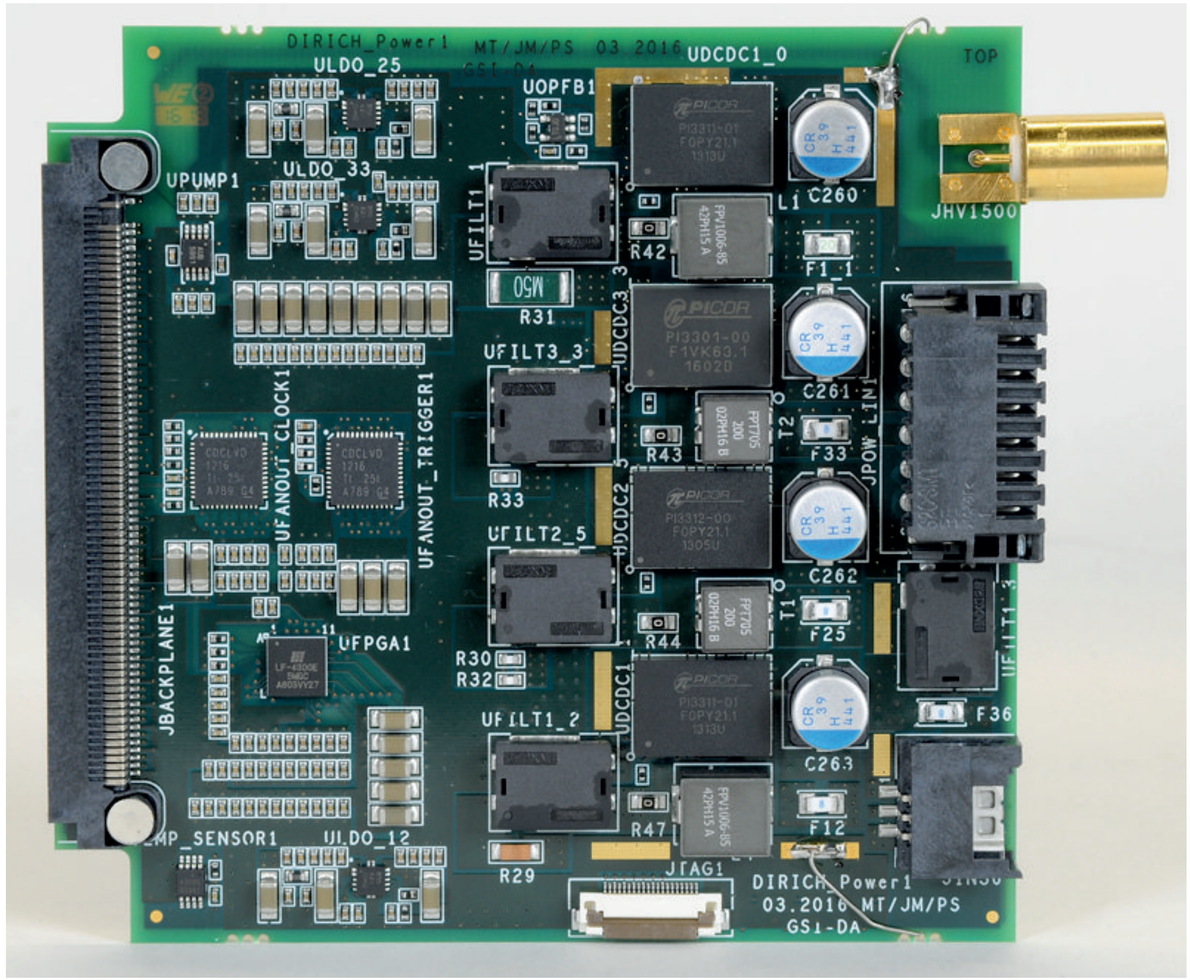
- all electrical connections, no active components
- light & gas-tight shield
- complex design due to number of connections
- mix of analog and digital signals



Power Board

- DC/DC converters to produce all required voltages
- Option: direct supply without converters for noise reduction (to be quantified)
- Voltage and current monitoring
- Feedthrough for HV

- Power dissipation: about 25 W per module
- Total power consumption: about 2 kW (HADES)

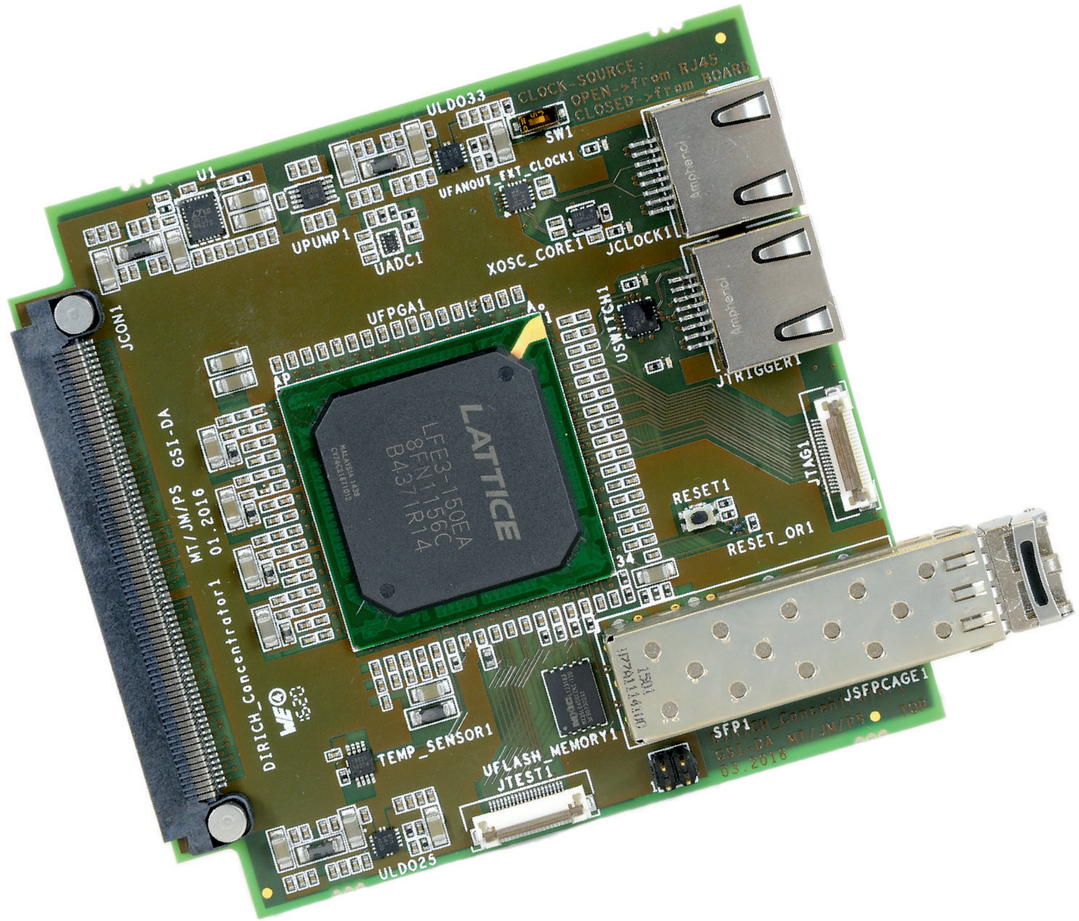


Concentrator Board

- Lattice ECP3-150 FPGA
- Bi-directional links to all 12 front-ends
- Event data is merged into one packet
- Optical link to central DAQ 2.4 GBit/s
- Inputs for external clock and reference time
- Output for trigger signal to run DAQ on any coincidence or pixel multiplicity

Rate Capabilities

- Electronics > 5 MHits/channel
- Data links > 20 MHits/module
  - optional trigger windows



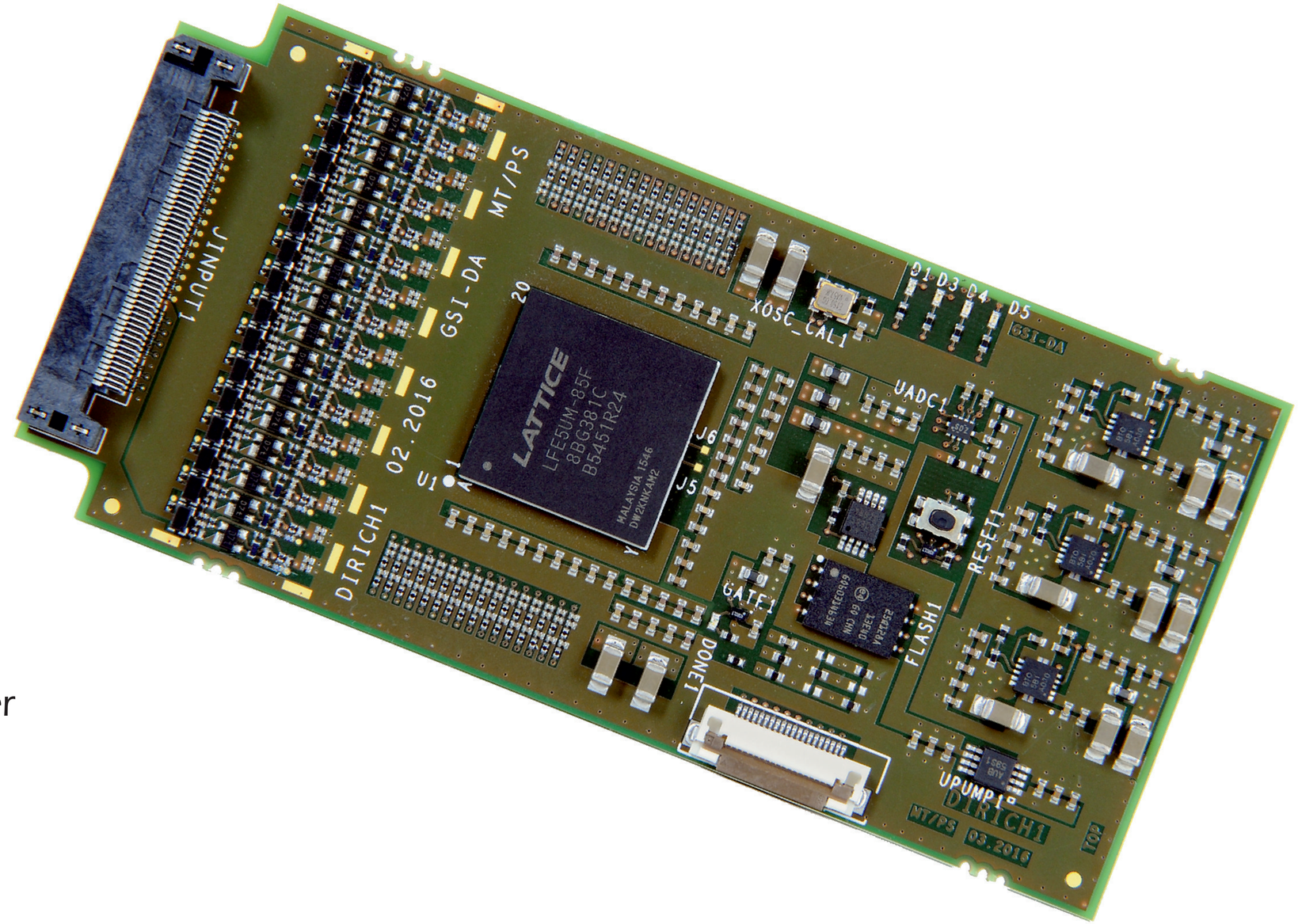
Higher Rates in CBM / PANDA

- CBM: up to 200 kHits/channel or 60 MHits/module
- data rates exceed 5 GBit/s per module in central parts
- Concentrator replaced independently with new module with 1/2 4.8 GBit/s links

DiRICH Board

Front-end Board

- Each PMT is read out by two front-end cards
- 32 analog channels
- Local linear voltage regulators
  - ultra-low drop (< 40 mV)
- 47 x 100 mm

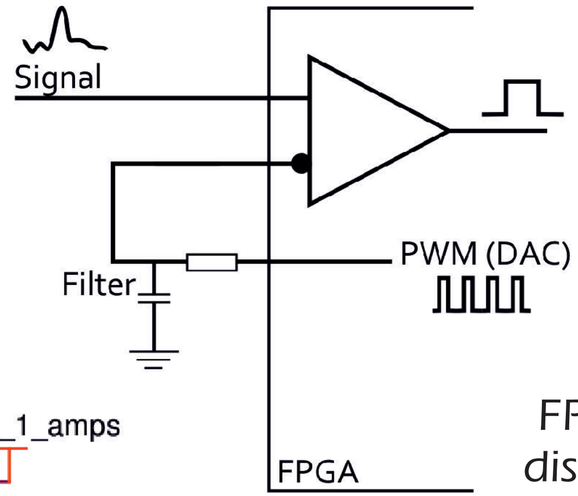


FPGA (Lattice ECP5-85)

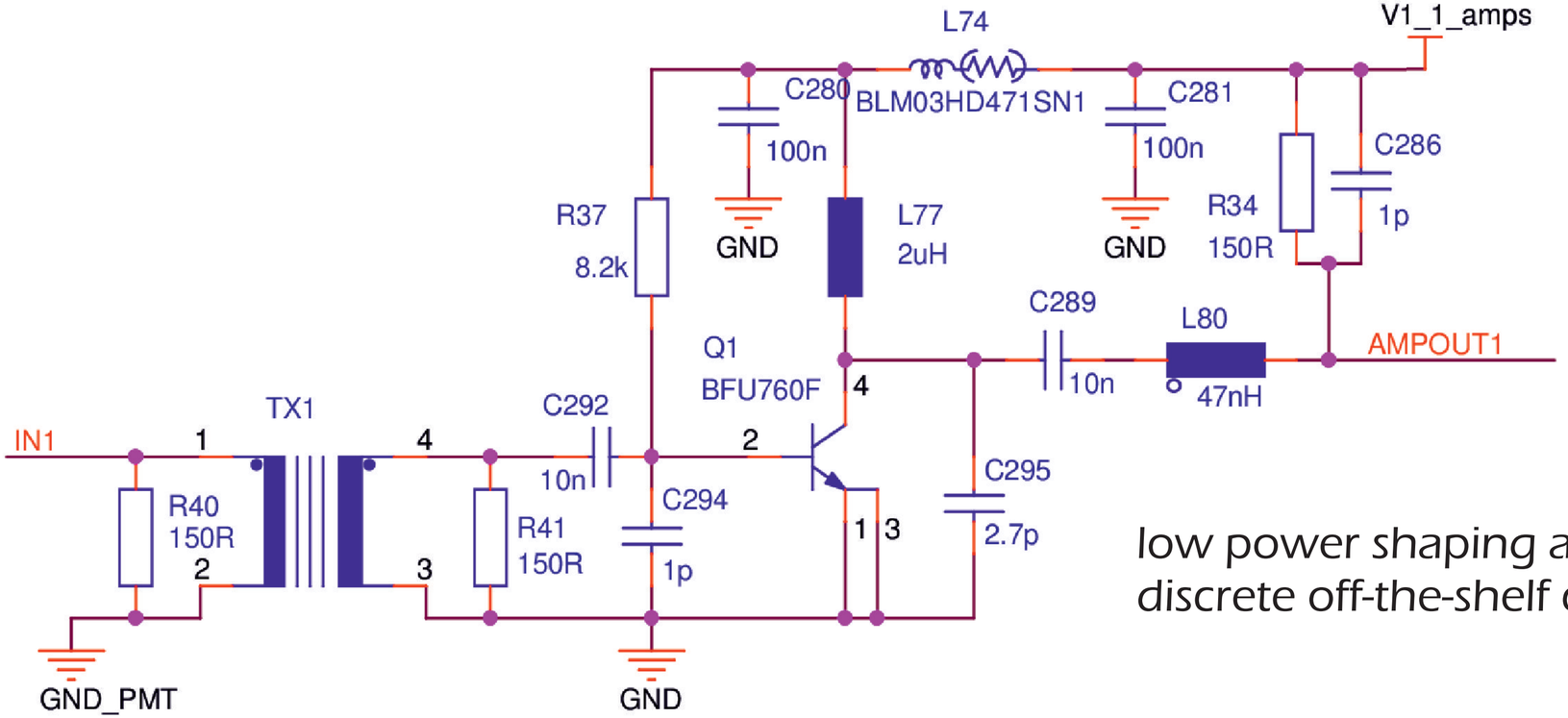
- Thresholds
  - internal Delta-Sigma-DAC + Filter
- Discrimination
  - comparator in LVDS receivers
- Time Measurement
- DAQ logic - Read-out, Triggering

Analog Stage

- small footprint: 12 x 2.7 mm²
- mostly 0201 components
- 12 mW @ 1.1 V
- amplification ~ 20 - 30 amplitude dependent
- channels galvanically isolated
- threshold ~ 1 mV of input

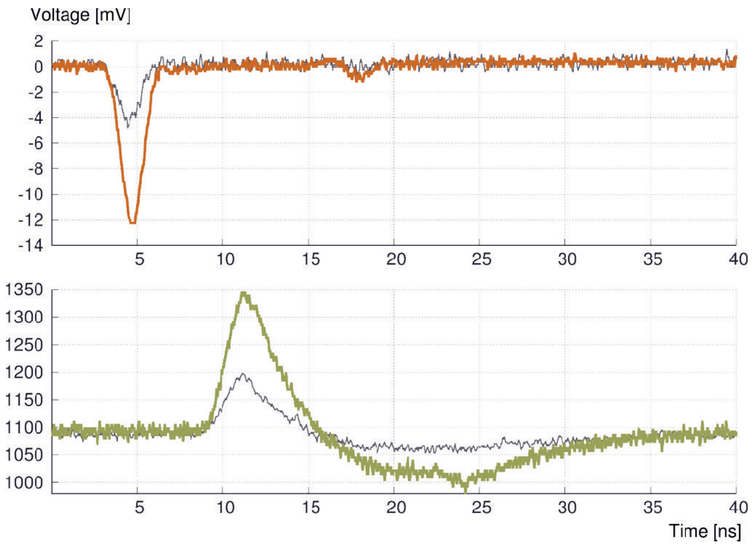


FPGA-based discriminator

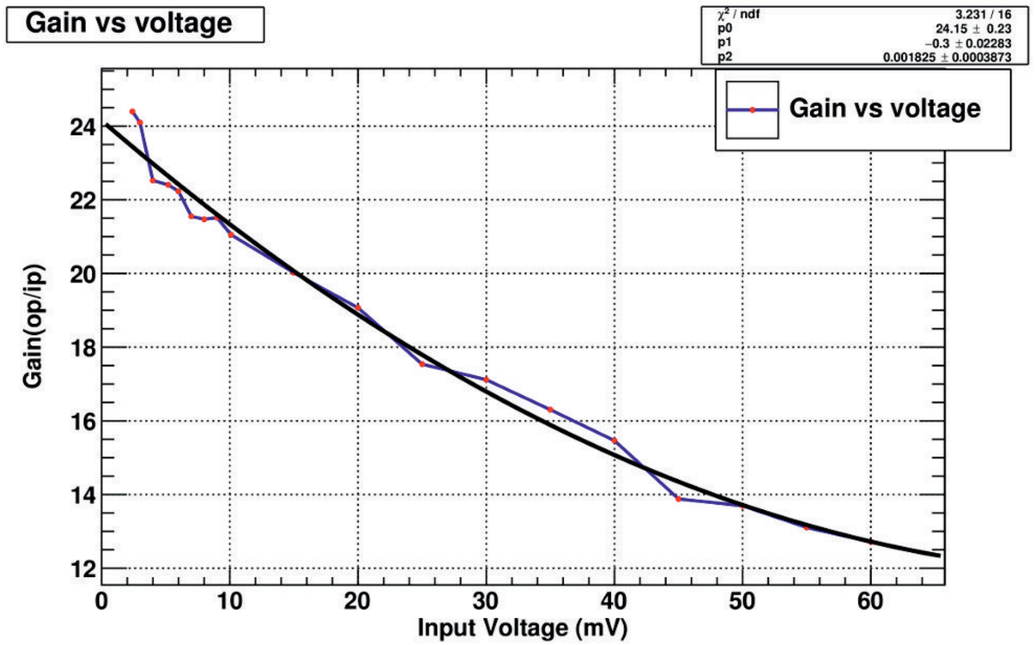


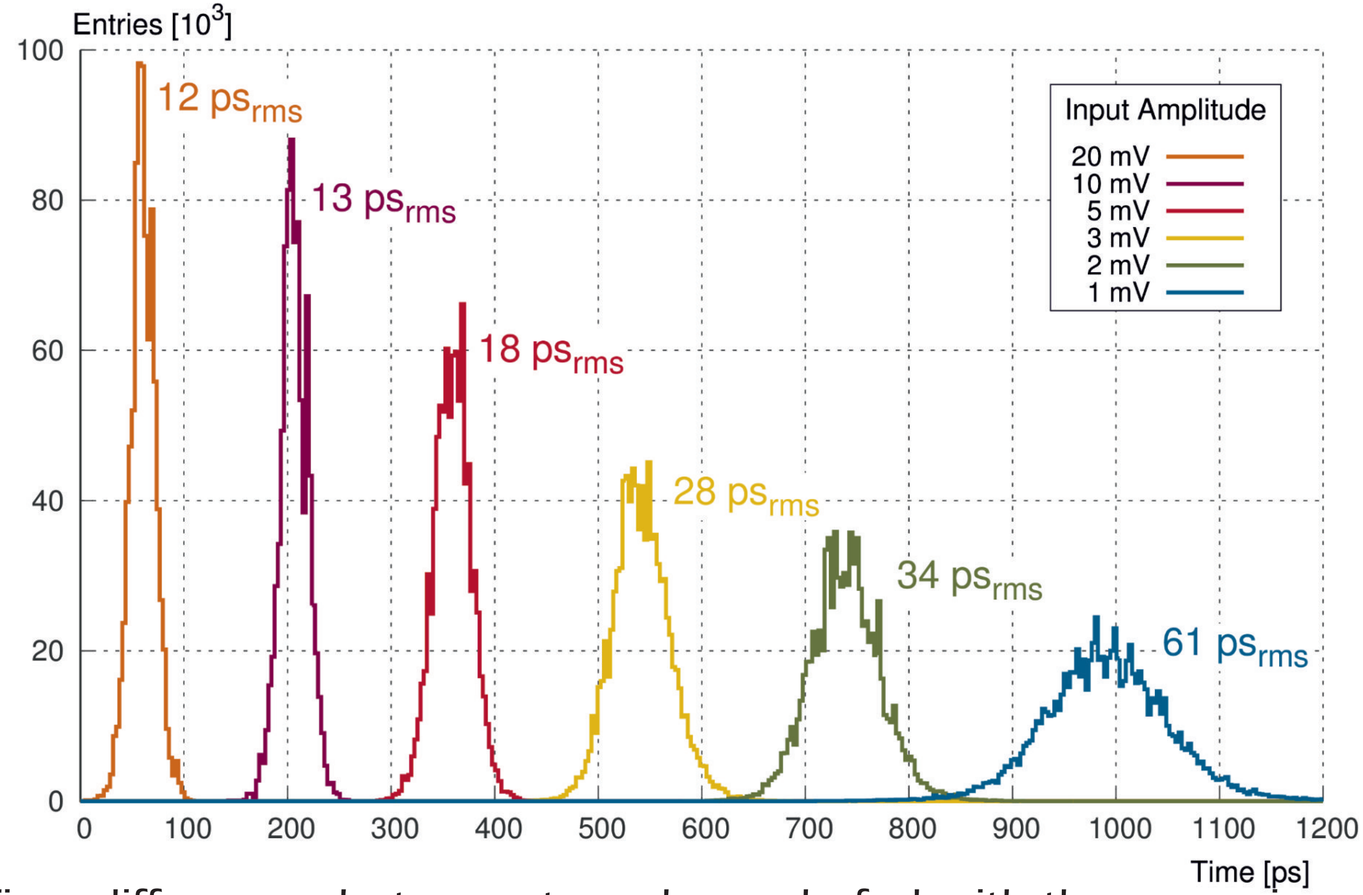
low power shaping amplifier
discrete off-the-shelf components

Performance



Typical input signal:
5 - 40 mV amplitude
2-4 ns width

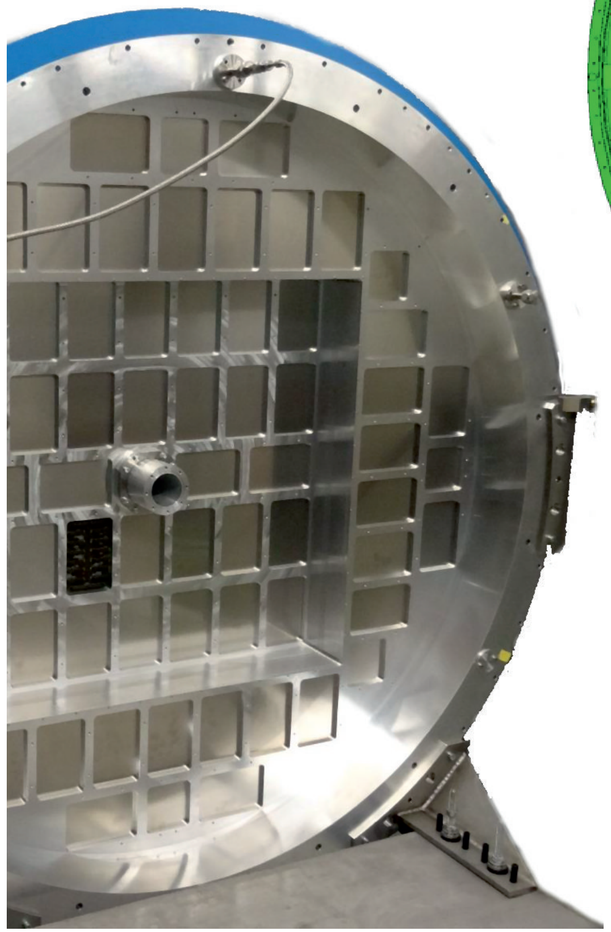


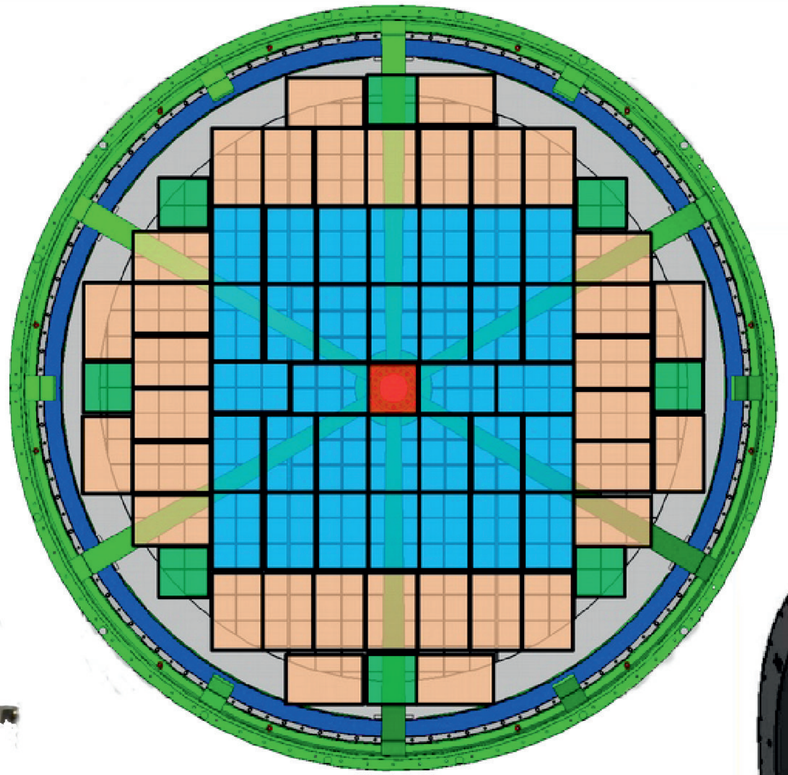


Time differences between two channels, fed with the same signal - varying input signal amplitudes

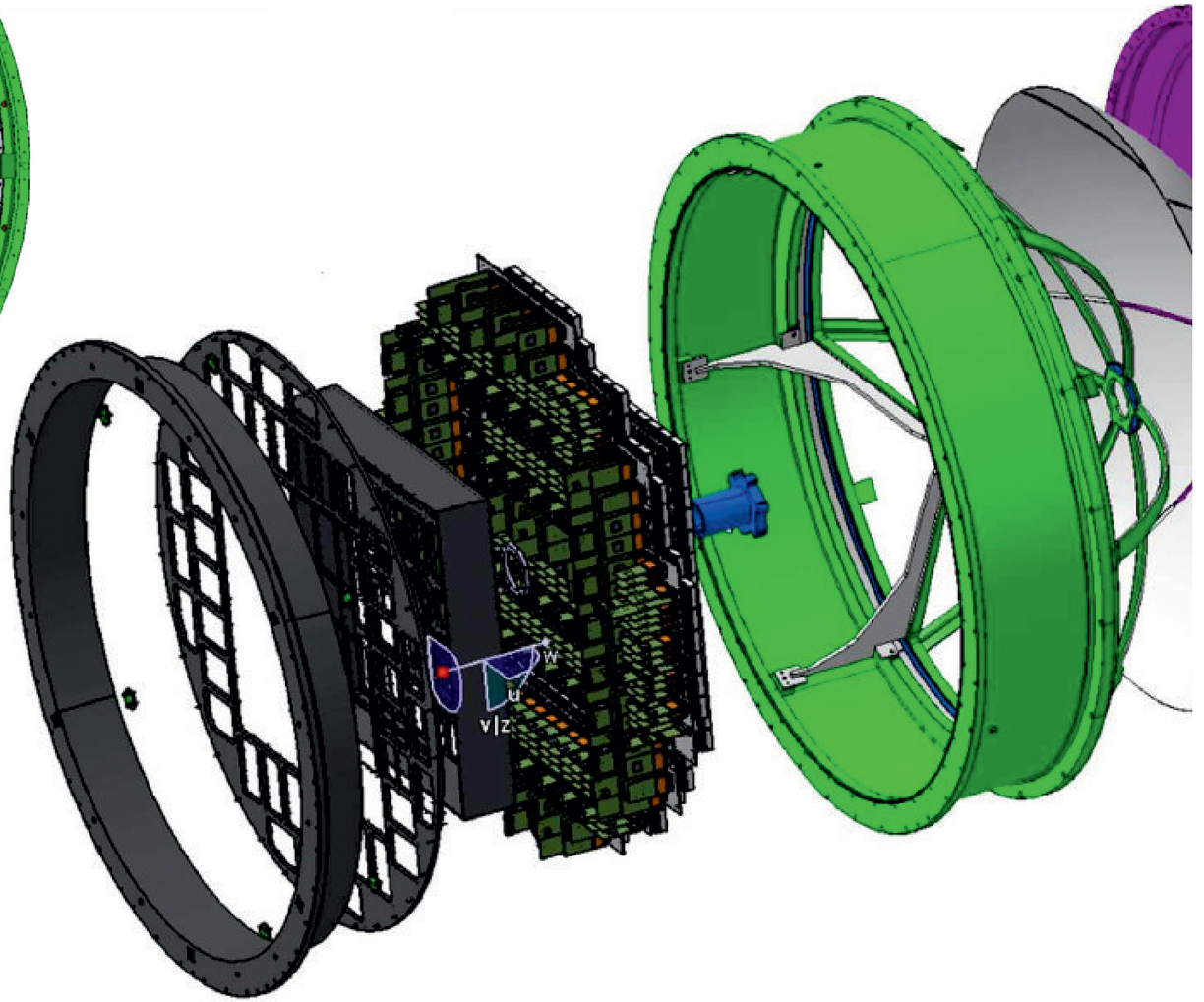
Integration

The new HADES RICH backplane fitted with 74 read-out modules

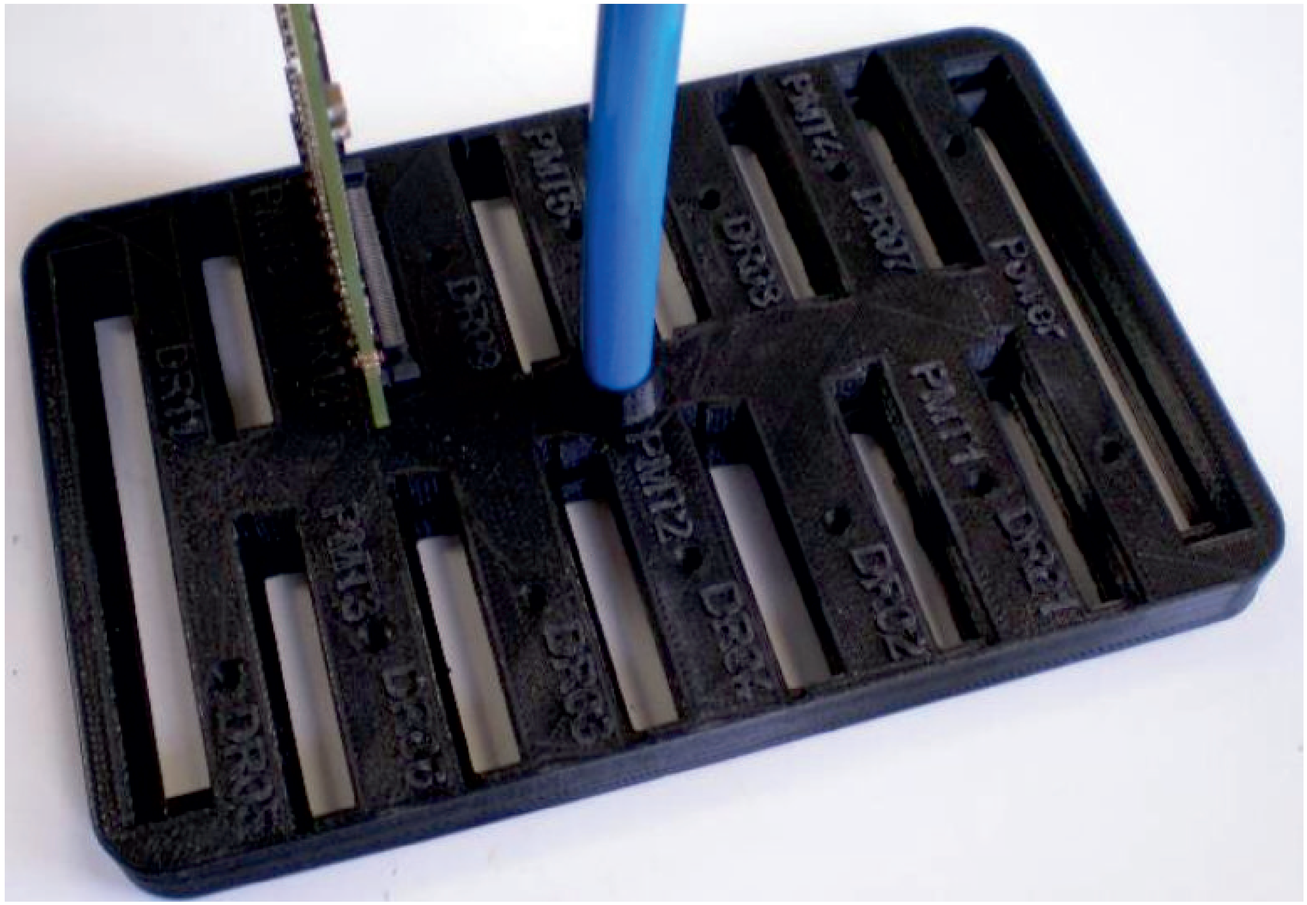


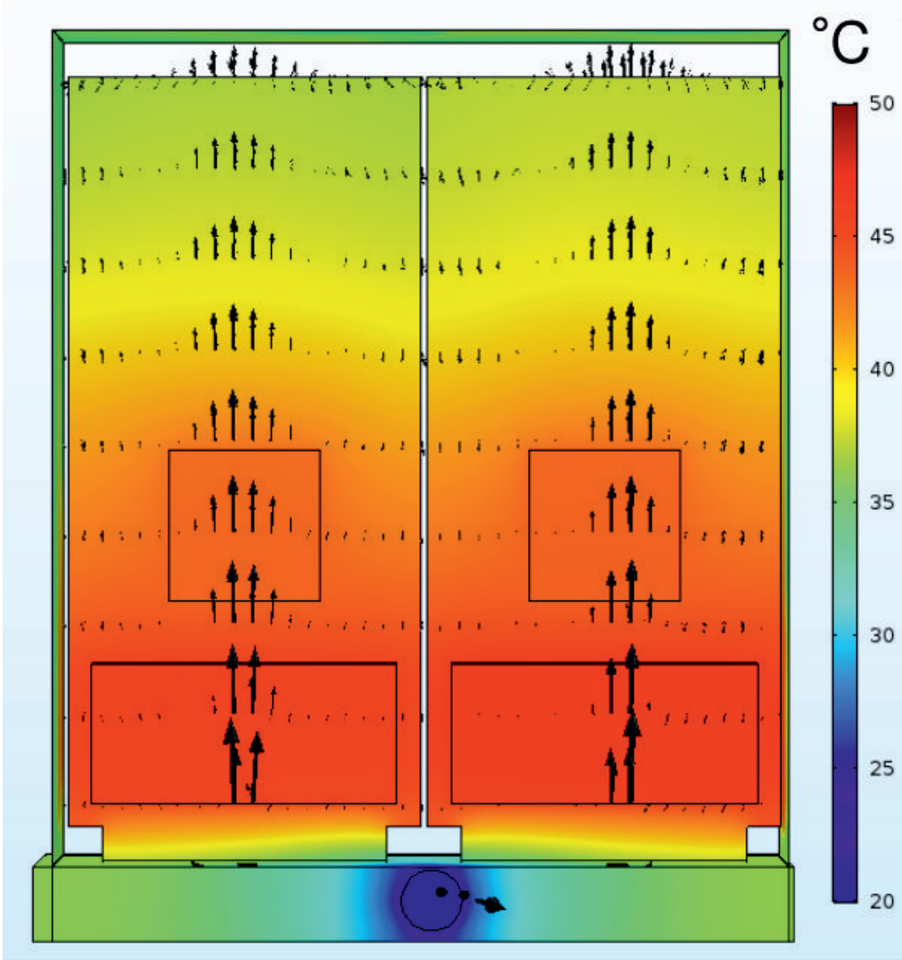


27000 channels on ~ 1.3m²



Cooling


PMT5
DRV5
DRS5
PMT4
DRV4
POWER
PMT3
DRV3
DRS3
PMT2
DRV2
DRS2
PMT1
DRV1
DRS1


°C
50
45
40
35
30
25
20

Summary

Electronics for the RICH and DIRC detectors at FAIR
applicable with small modifications for the
HADES, CBM and PANDA experiments

small, low-power discrete amplification and shaping stage has been designed

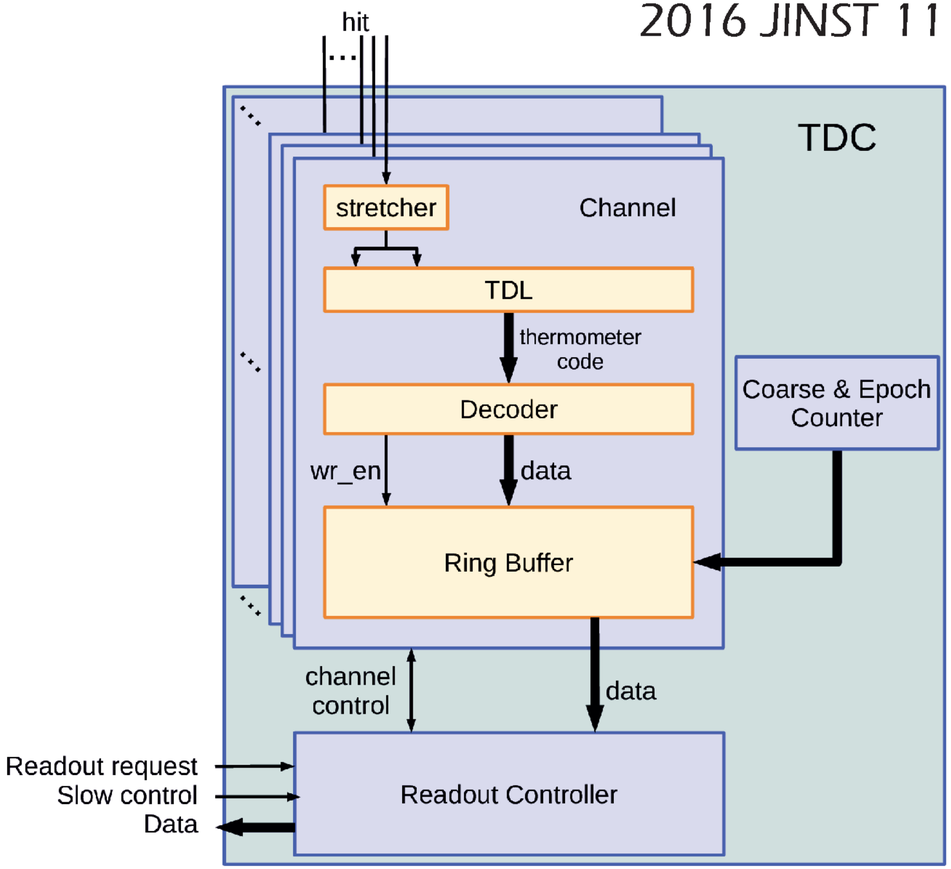
First in-system tests have been done, large scale and in-beam tests to be done in next months

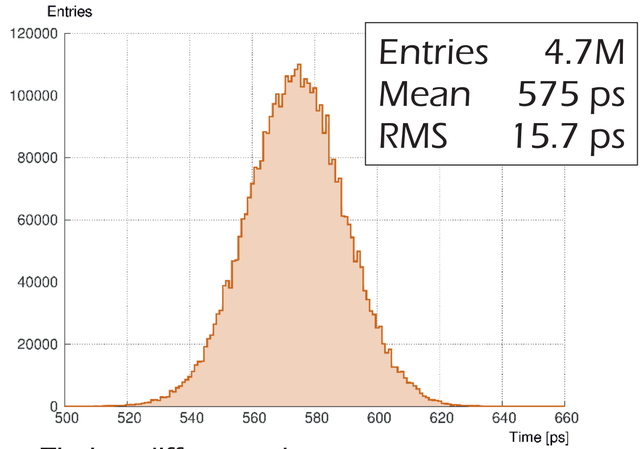
All read-out, control, software and TDC functions are based on developments made within the TRB community by various people and institutions.

http://trb.gsi.de

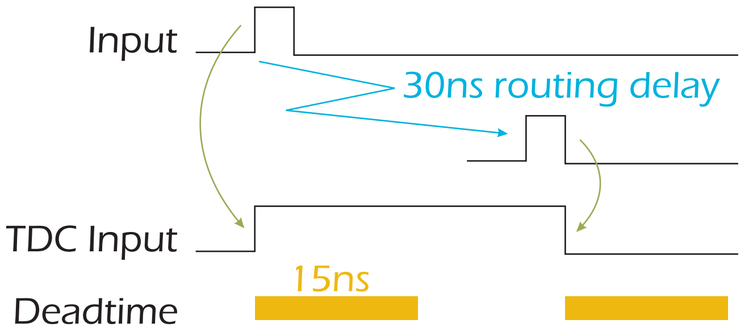
Time Measurement

- Timing precision ~ 20 ps
  - PMT timing ~ 300 ps
  - high precision needed for ToT (amplitude, e.g. double hits)
- Measurement of both edges in same TDC channel using internal stretcher method (see 2016 JINST 11 C01046)





Timing difference between two channels of the same front-end module



The falling edge of the input can not be detected due to the intrinsic dead-time of the TDC. Instead, routing is used to delay the falling edge until the TDC is ready again.