

# Data acquisition and synchronization for CBM experiment

mgr inż. Marek Gumiński  
ISE PW

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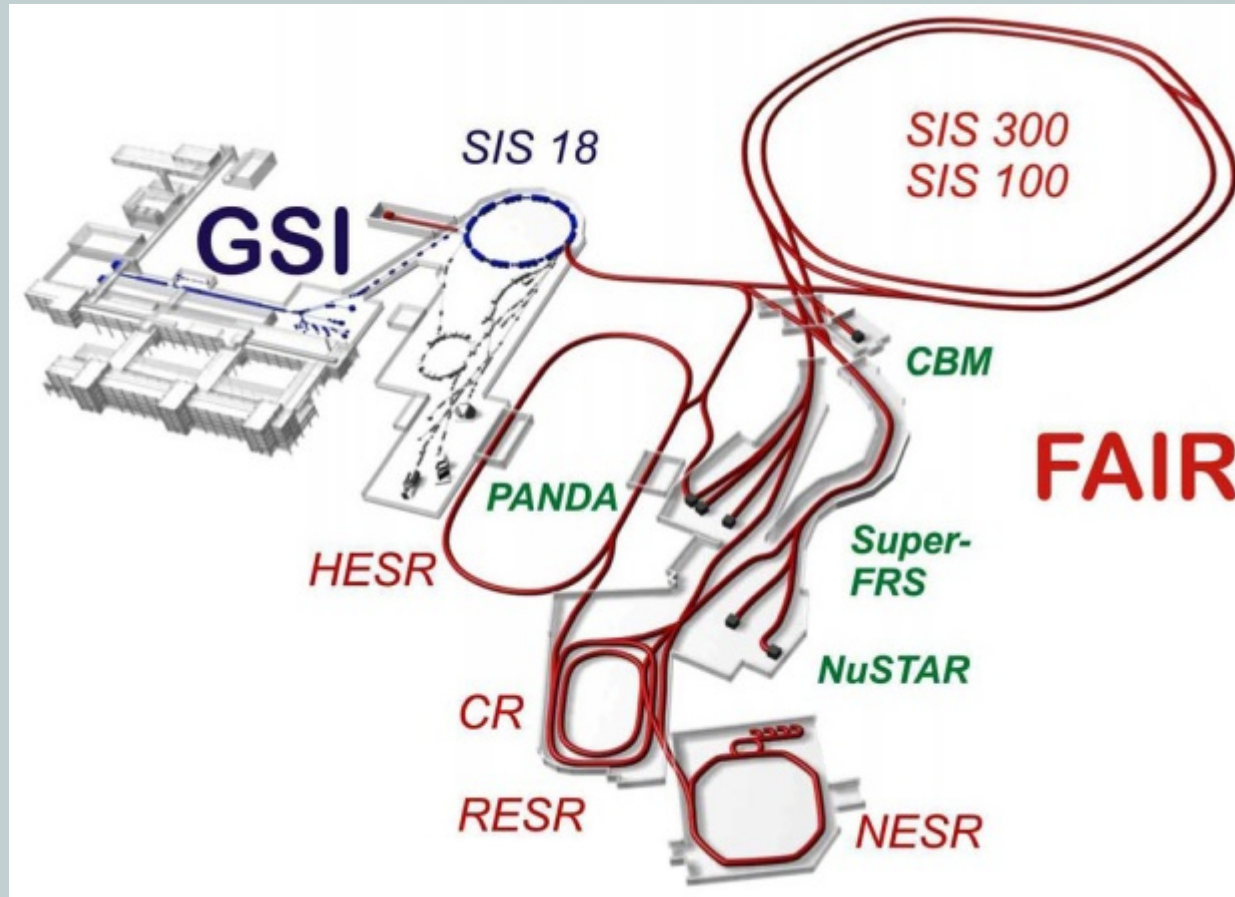
# FAIR



30.05.17



# Experiments at FAIR



# CBM experiment

- Impact of heavy nuclear nuclei with energies ranging from a few to about 35 GeV
- Investigation of matter properties in environment unexplored in other experiments.
- Conditions reminiscent of those in the interiors of neutron stars

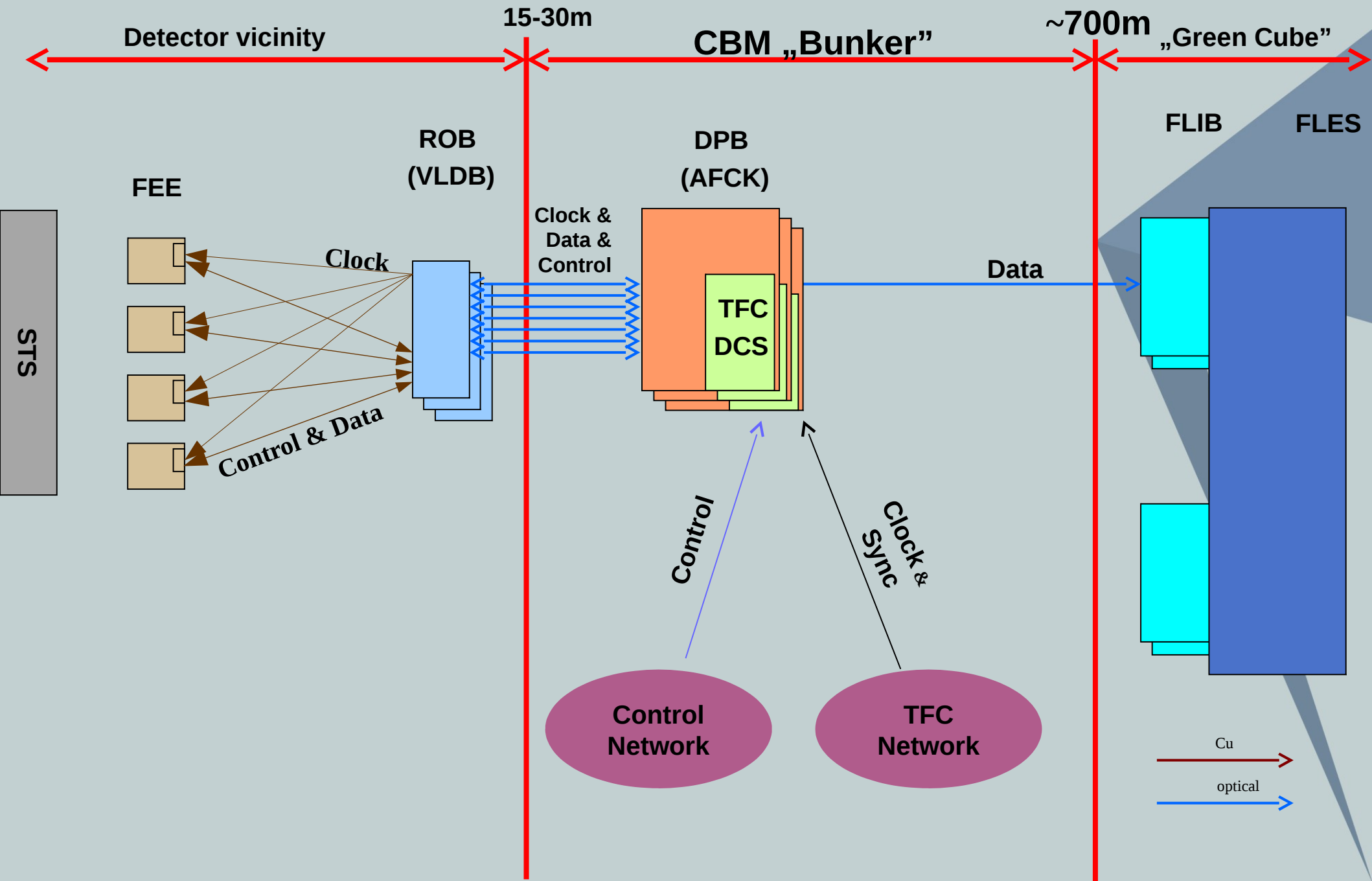


# CBM experiment

- Continuous work
- Multiple detectors
- Lack of external trigger
- Event identification based on aggregated data
- High event frequency (up to 100 MHz)



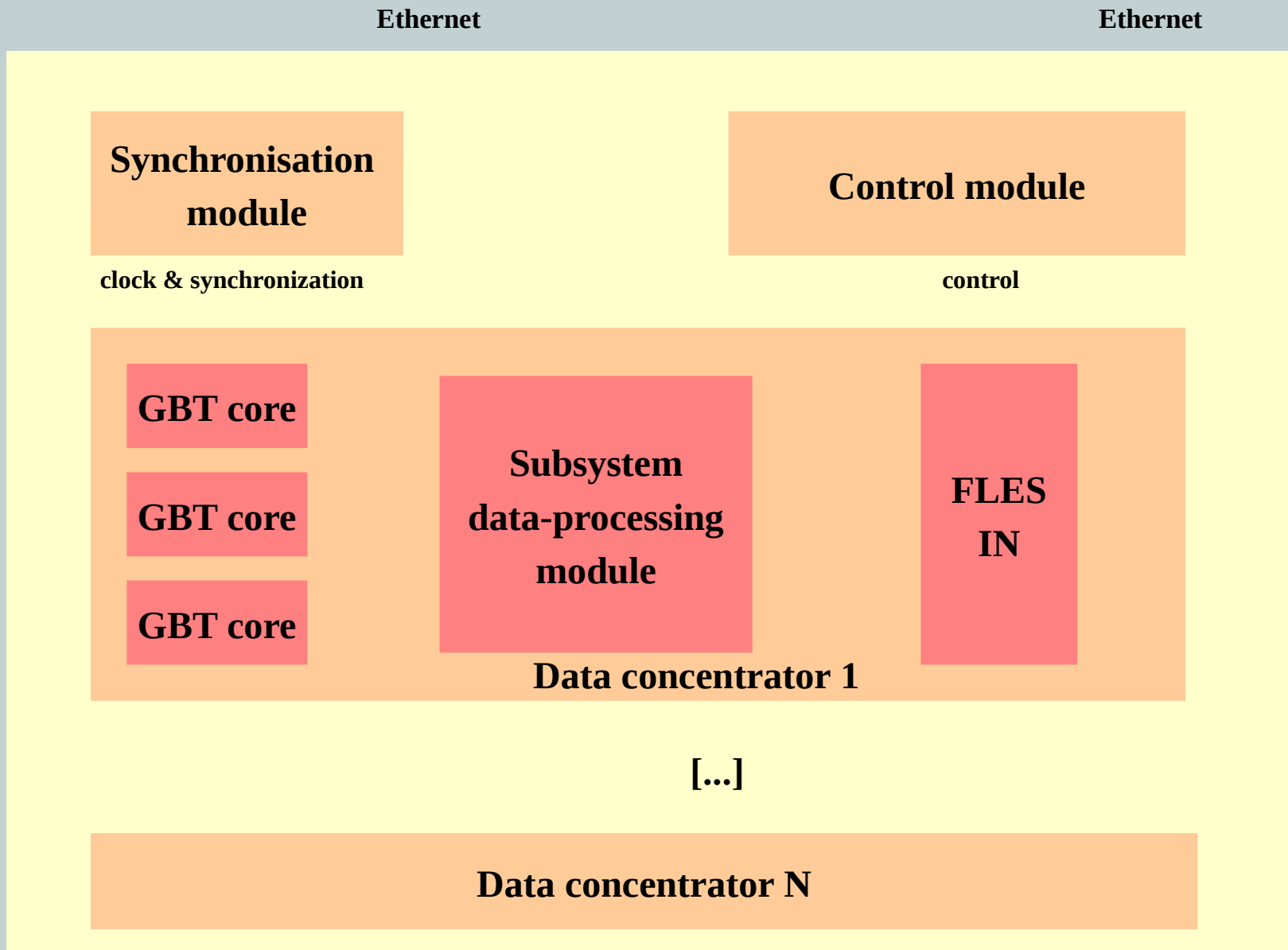
# Legacy data acquisition schematics



# Functions of DPB

- Collecting data from multiple low speed links from detection circuits
- Ordering and packaging data into "microcontainers" covering specified time intervals
- Sending packed data through high-speed links
- Distribution of synchronization signals
- Distribution of control commands (deterministic latency) and configuration to FEE modules

# Simplified block diagram of DPB firmware





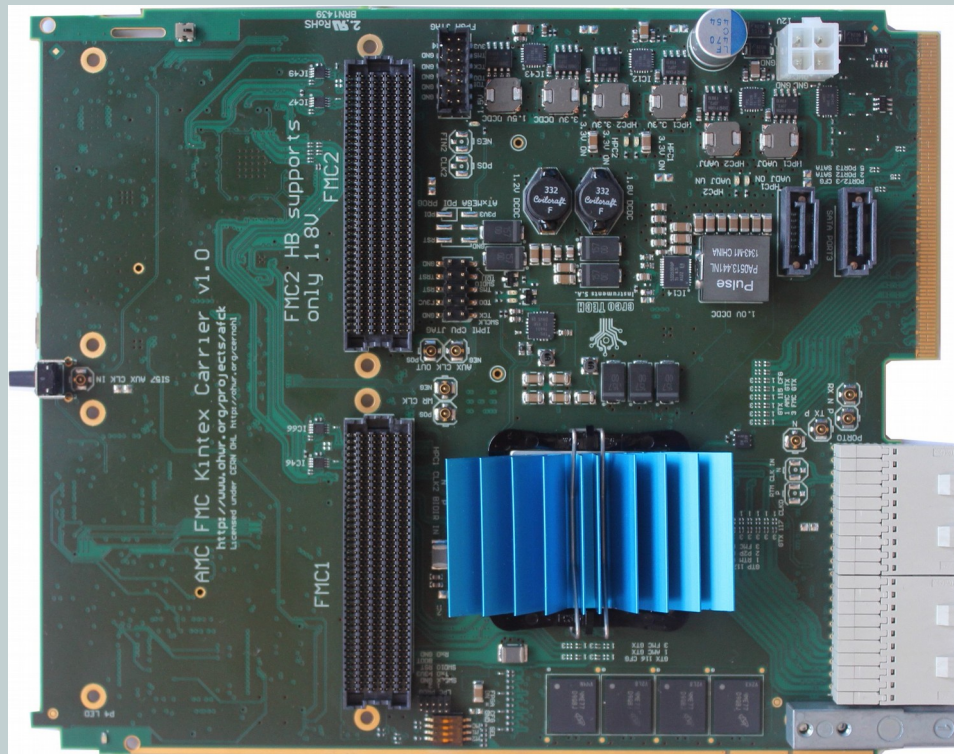
# Finished work

- Selection of hardware platform
- Selection the control protocol
- Protocol definition and verification with STS-XYTER devices



# Selection of hardware platform

- AMC FMC Carrier Kintex (AFCK) board
- Open hardware
- MTCA.4 ( $\mu$ TCA for Physics) architecture



# Selection of hardware platform

- Kintex-7 325T FFG900 FPGA
- 16 GTX (do 10 Gbps)
- 2xFMC HPC, AMC, RTM, 2xSata
- 2 GB DDR3 SDRAM
- Gigabit line configuration with replaceable capacitors
- Clock configuration with high performance crossbar

# Experiment controls

- Enabling operations on registers of all devices used in experiment
- Facilitation of development
- Backup (test) readout method

# Experiment controls

- Ethernet:
  - Cons:
    - Lack of reliability
    - High latency
  - Pros:
    - High bandwidth
    - Cheap infrastructure
    - Ability to utilize existing network
    - Easily implementable in FPGA

# Experiment controls

- Considered protocols:
  - TCP
    - Difficulty of implementation, high FPGA usage, many redundant features under experimental conditions
  - Etherbone
    - Open, simple, small FPGA usage, no reliability
  - IPBus
    - Open, simple, small FPGA usage, acknowledged transmission, advanced Linux driver

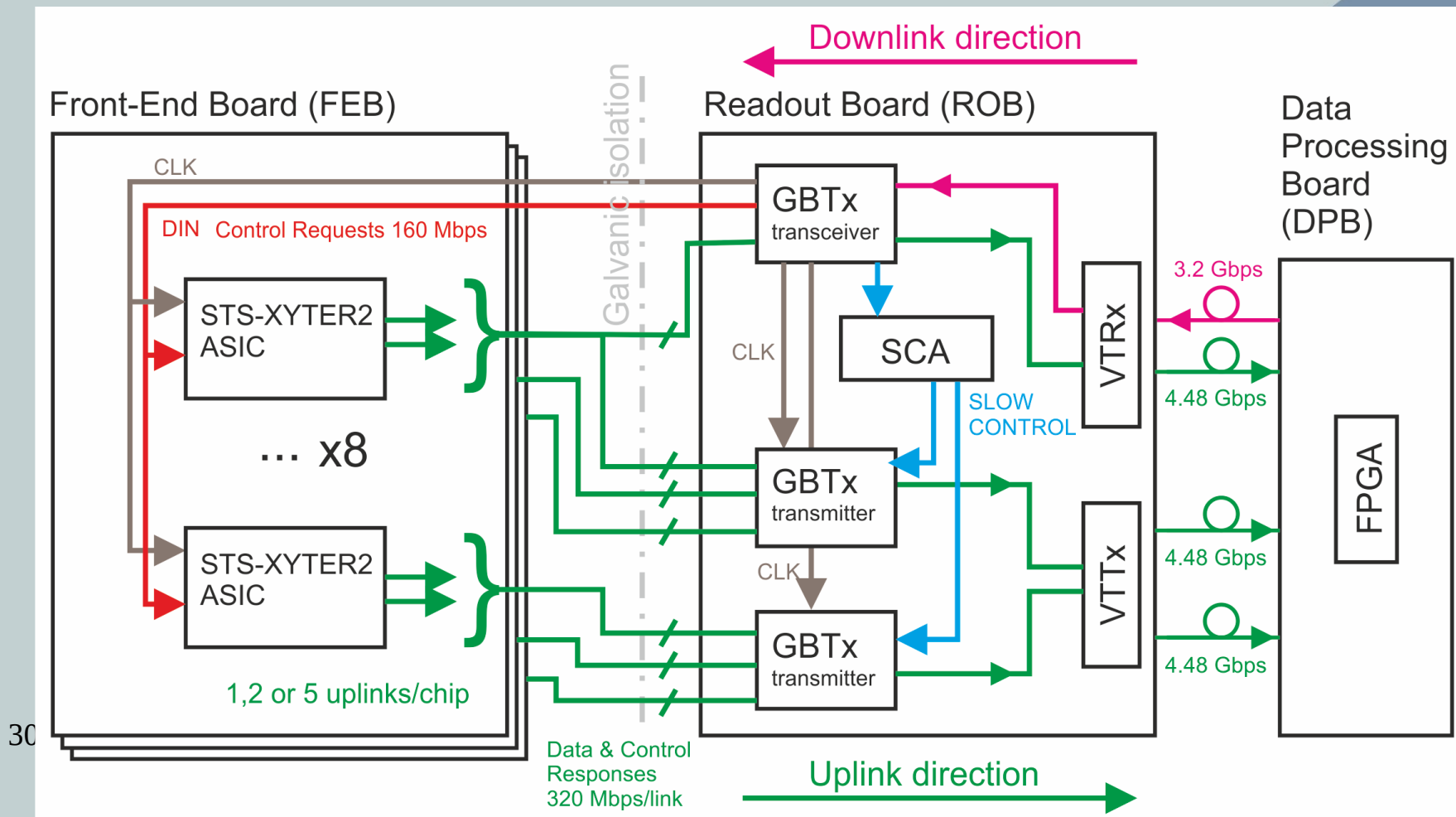
# Experiment controls

- Selection of IPbus
- IPbus core ported to Kintex 7
- Communication testing
- Automated register map generation for Linux IPbus driver



# FEE Readout

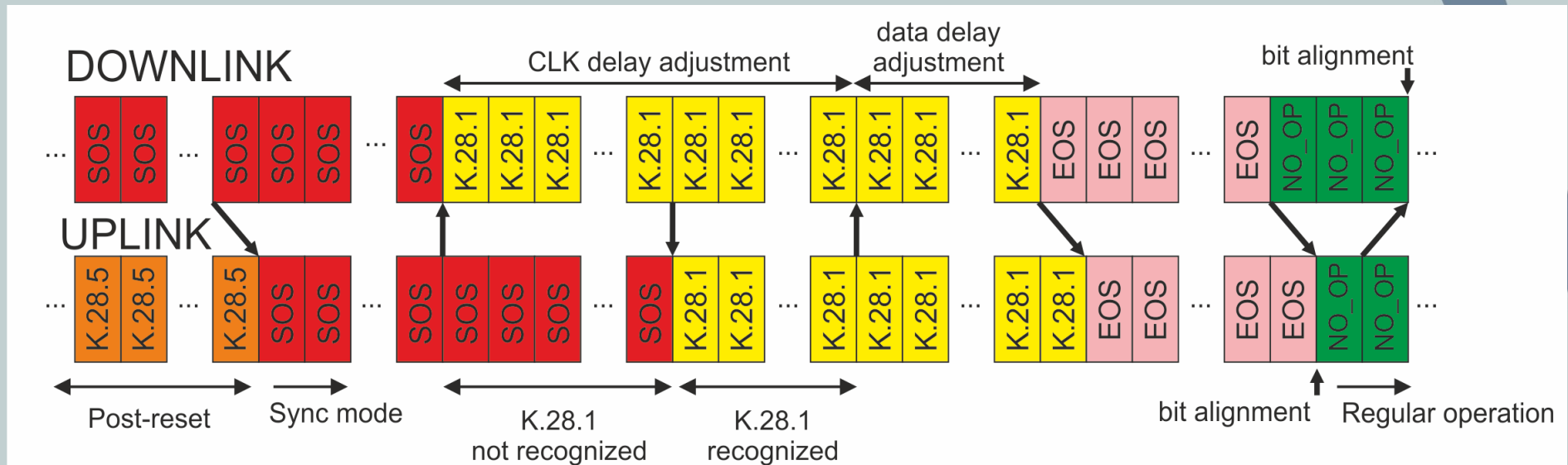
- Maximize the bandwidth of acquired data
- Providing deterministic delays in the transmission of control commands





# Communication protocol

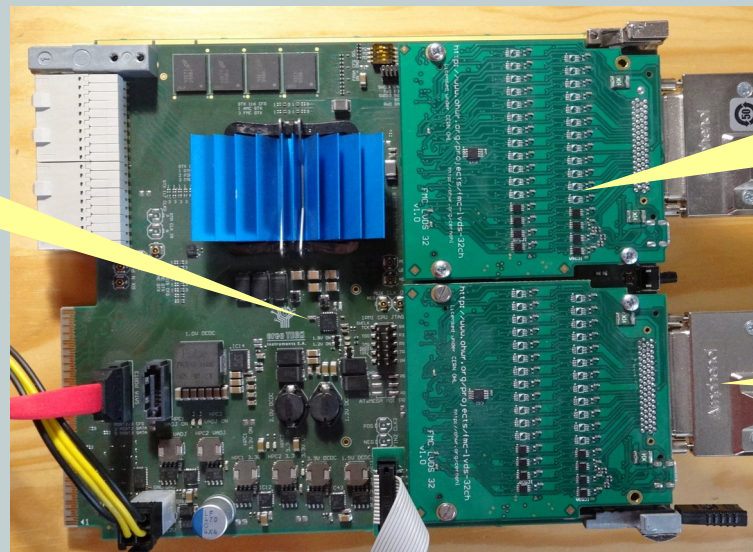
- E-link links provide constant, but unknown delay
- The protocol includes a link delay compensation procedure



# STS-XYTER protocol tester

- STS-XYTER emulation in FPGA
- Emulation of STS-XYTER interface module
- LVDC connection with AC coupling

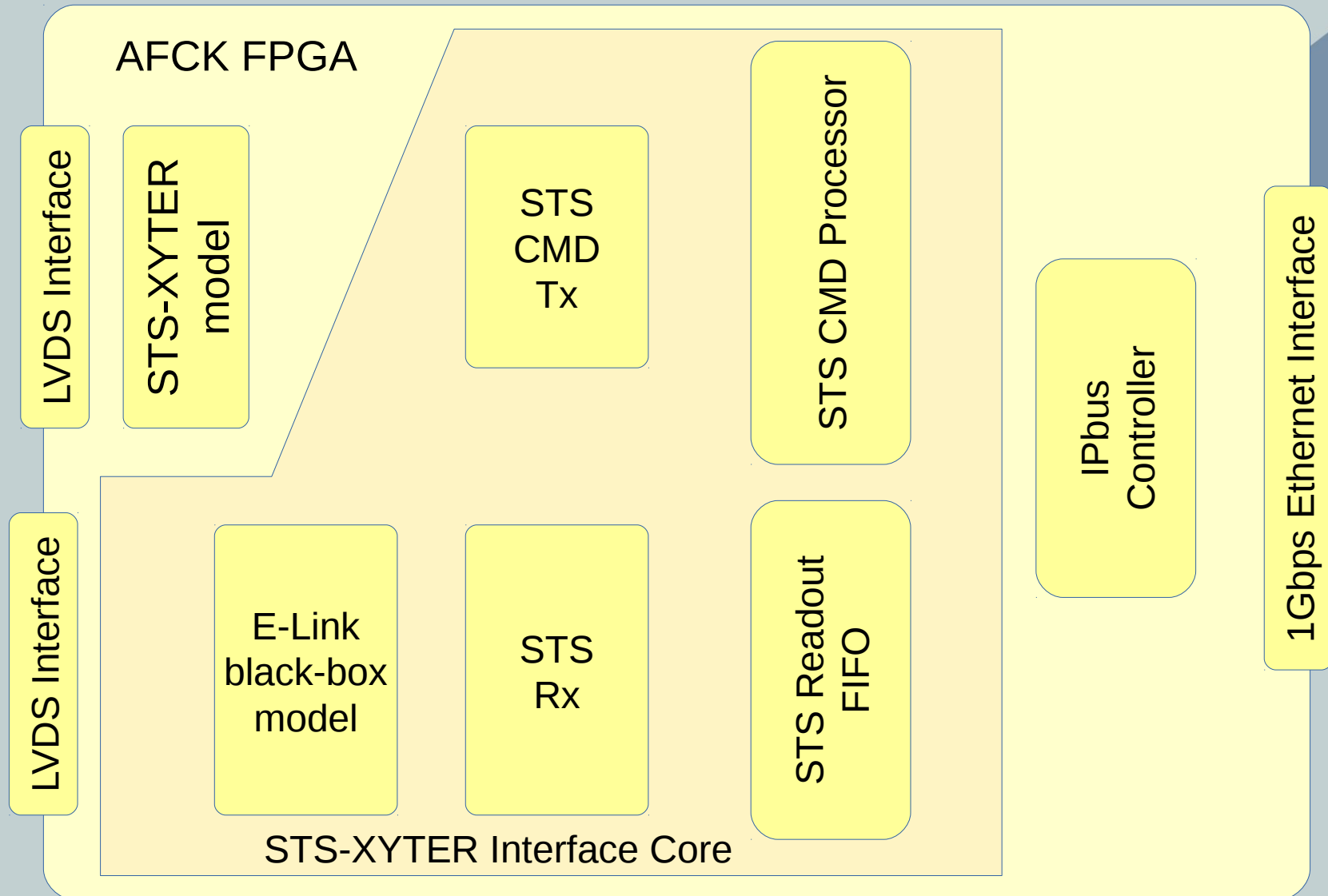
**The AFCK  
board**



**The FMC-VHDCI  
board**

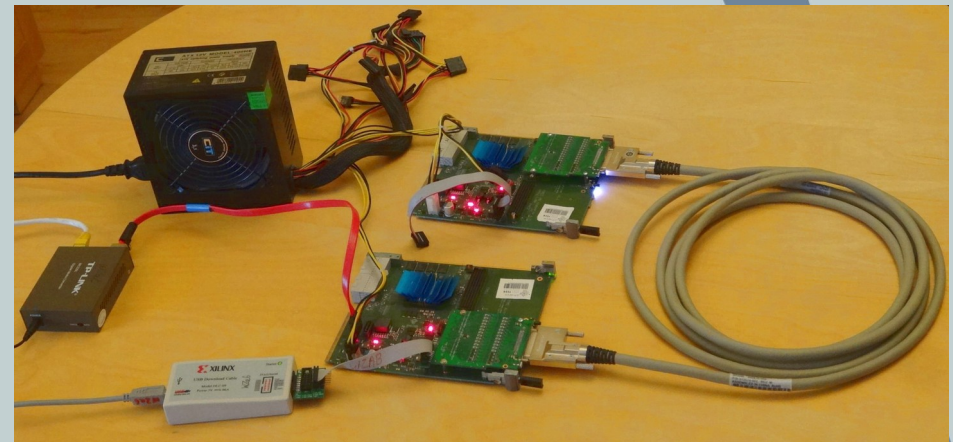
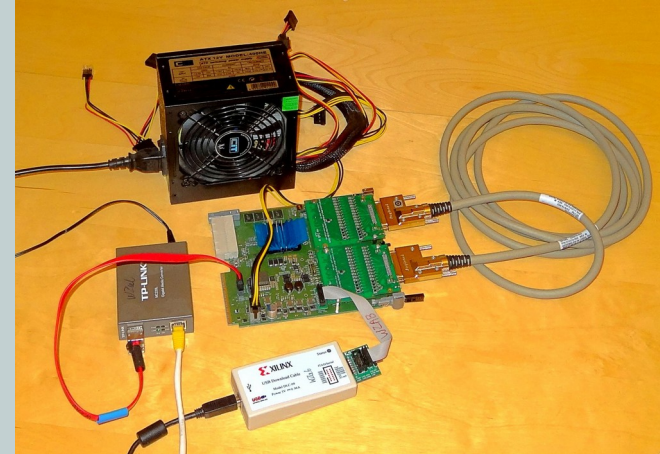
**VHDCI  
cable**

# STS-XYTER protocol tester



# STS-XYTER protocol tester

- Single board setup
  - STS-XYTER model and controller implemented in the same FPGA
- Two board setup
  - STS-XYTER model implemented on one board. Controller implemented on other board



# Synchronization

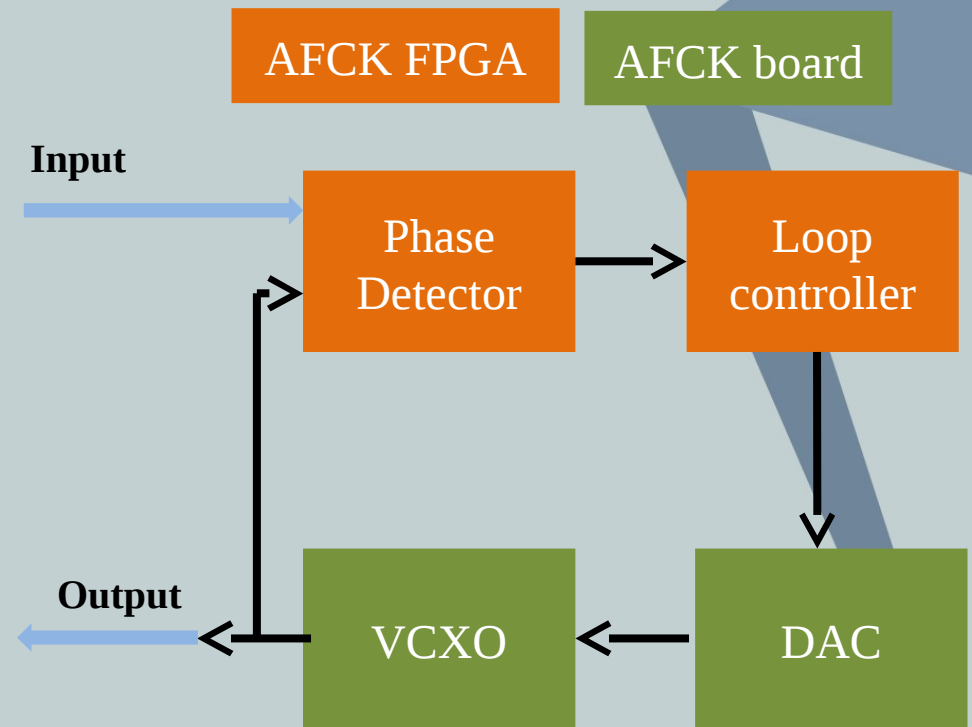
- FEE modules must work synchronously
- Clock frequency
- Time stamp
- GBTx recovers the clock from data transmitted from the DBP, with 3.2 Gbps link
- The recovered clock signal is transmitted to FEE
- GBTx provides deterministic command delays
- DPB communicates with GBTx via Ipcore GBT-FPGA
- The GBT-FPGA requires a high quality reference clock frequency of 40 MHz

# Synchronization

- Whiter Rabbit protocol considered as reference clock source for DPB
- Dedicated timing system is developed instead
- Acquired clock quality not yet defined, so jitter cleaning on DPB may be necessary

# Synchronization

- Example implementation of jitter cleaner
- Similar design implemented on timing system boards



# Ongoing and future

- Running STS tester via GBTx link (VLDB board)
- Development of beam tests firmware
- Preparations for new readout chain (CRI)





Thank you for attention!