The frontend electronics of the CBM Silicon Tracking System

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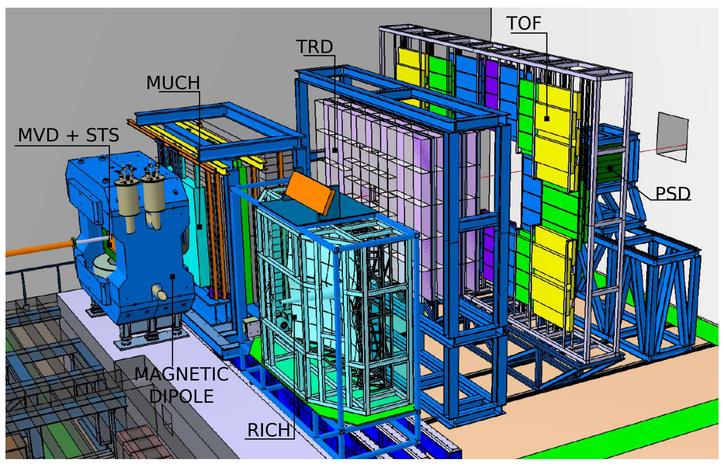
The Compressed Baryonic Matter (CBM) experiment and the Silicon Tracking System (STS)

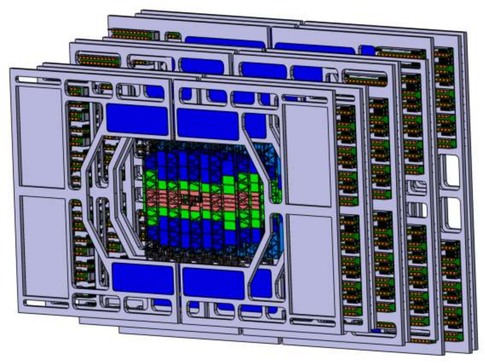
The CBM experiment:

- To explore the QCD phase-diagram at moderate temperature and high density.
- pA and AA collisions up to Au + Au @ 2-11 AGeV (SIS100) at 10^5-10^7 interactions/s.
- High speed data processing and acquisition system.
- 4D event reconstruction and fast selection algorithms.

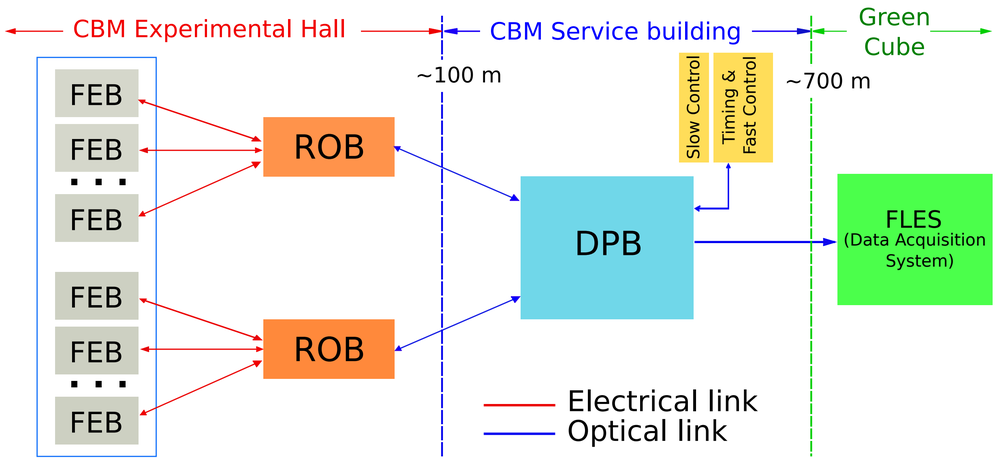


STS features:

- 8 tracking stations in 1 T field.
- Double-sided micro-strip Si sensors.
- 7.5° stereo-angle between front and back side strips.
- High efficiency.
- Tracking up to 1000 charged particles/collision.
- Radiation hardness: 10^{14} 1 MeV n_{eq}/cm^2.
- Low mass: material budget per station $\sim 1\%$ X_0.



The STS Readout chain



Block diagram of the STS Readout chain

Front End Boards (FEB)

Part of a functional module, where 2 FEB with detector specific ASIC are connected via microcables to a silicon sensor.

- Every FEB contains 8 STS-XYTER ASICs for reading out 1024 channels.
- Provides digitized hits.
- Located close to the silicon sensors.

Read out Boards (ROB)

- Data aggregation from several ASICs.
- Optical readout interface.
- Control and clock distribution.
- Based on CERN GBTx and Versatile Link components.
- Located inside STS box.
  → Limited space.
  → Radiation hardness.

Data Processing Board (DPB)

CBM DAQ layer with common hardware platform.

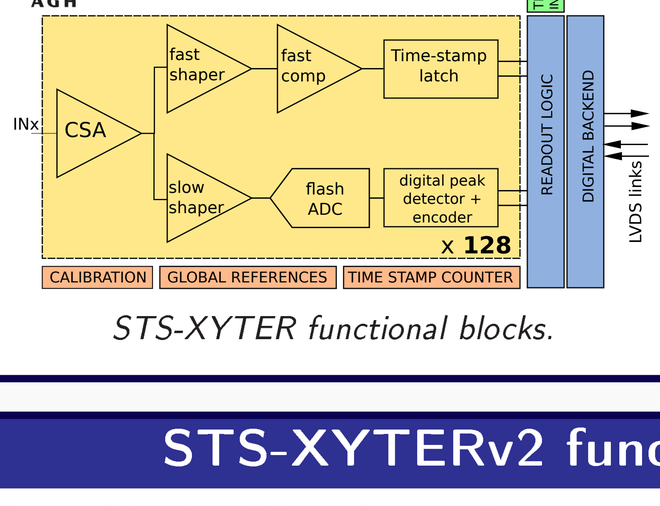
- FPGA based.
- Timing and control interfaces.
- Data preprocessing.

First Level Event Selection (FLES)

- Time slice building & full event reconstruction.
- Online event selection.

The STS-XYTERv2 ASIC

STS-XYTER → **S**TS + **X,Y** coordinates + **T**ime and **E**nergy **R**esolution
Low power, self-triggering ASIC dedicated for reading out the double-sided Si sensors. It provides time and energy information.



STS-XYTER functional blocks.

STS-XYTER features:

- 128 readout channels + 2 test channels.
- Time resolution: ~5 ns.
- 14 bit time stamp.
- 5 bit flash ADC.
- Linearity range up to 15 fC.
- Radiation hard layout.
- Digital backend compatible with the CERN GBTx data concentrator.

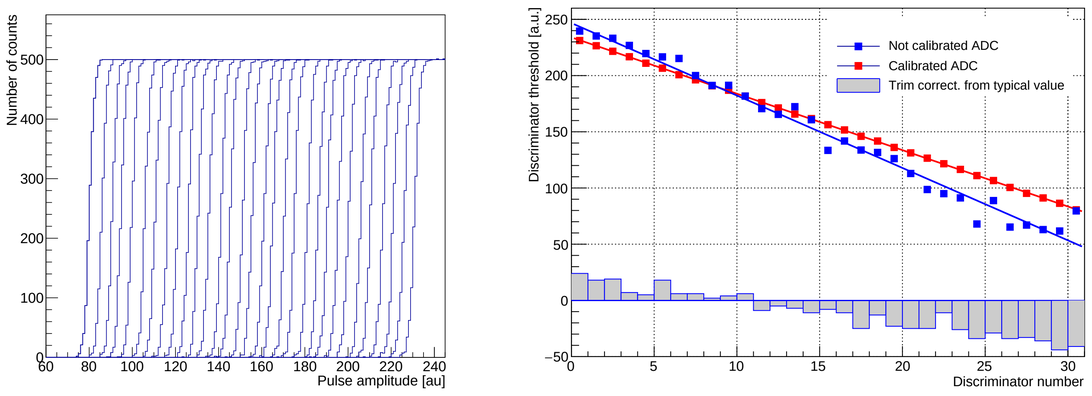
STS-XYTERv2 functionality tests

Test of backend interface and communication protocol

- Synchronization protocol (Sync., control, readout protocol).
- Link masking and ASIC addressing:
  → Chip bonded address.
  → Broadcast address.
- Register access (Write/Read).
- Generating and reading out test hits.

Analog frontend performance

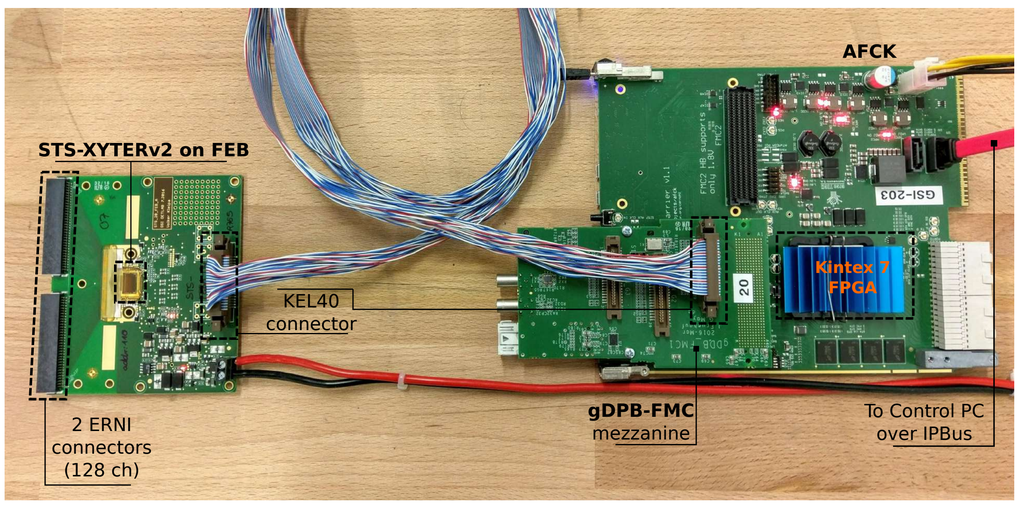
Development and test of ADC trim procedure to evaluate and calibrate in-channel ADC by using analog test pulses and acquiring S-curves with dedicated counters in the STS-XYTER.



S-curves from a selected channel in the STS-XYTER and ADC calibration

Test setup

Test of single STS-XYTER ASIC on FEB controlled via Protocol backend in AFCK FPGA. Flexible and modular platform for ASIC and sensor testing, software and firmware development.



- **STS-XYTER FEB:**
  Test board with 1 bonded ASIC and 128 channels connected.
  → Frontend side: Double ERNI connector for interfacing the silicon sensors.
  → Backend side: Kel40 connector as E-Link interface of a single STS-XYTERv2 (1 Clk, 1 Down-Link, 5 Up-Links)
- **gDPB-FMC:**
  Interface board Kel40 to FMC connector (only for prototyping).
- **AFCK:**
  AMC FMC Carrier Kintex (AFCK) as prototype DPB. FPGA based board implementing the STS-XYTER-DPB Protocol backend.
- **Control PC:**
  Readout with IPBus via SATA-to-SFP connection or optical fiber.

Summary and Outlook

- Frontend Board **(FEB)**, Readout Board **(ROB)** and Data Processing Board **(DPB)** are the major components of the CBM STS readout chain.
- **The STS frontend ASIC:**
  → The STS-XYTERv2 ASIC is available since fall 2016.
  → Several ASIC functionalities have been tested via protocol backend in AFCK.
  → Further studies such as channel performance, noise study and SEU tests are ongoing for optimizing and checking the STS-XYTER.