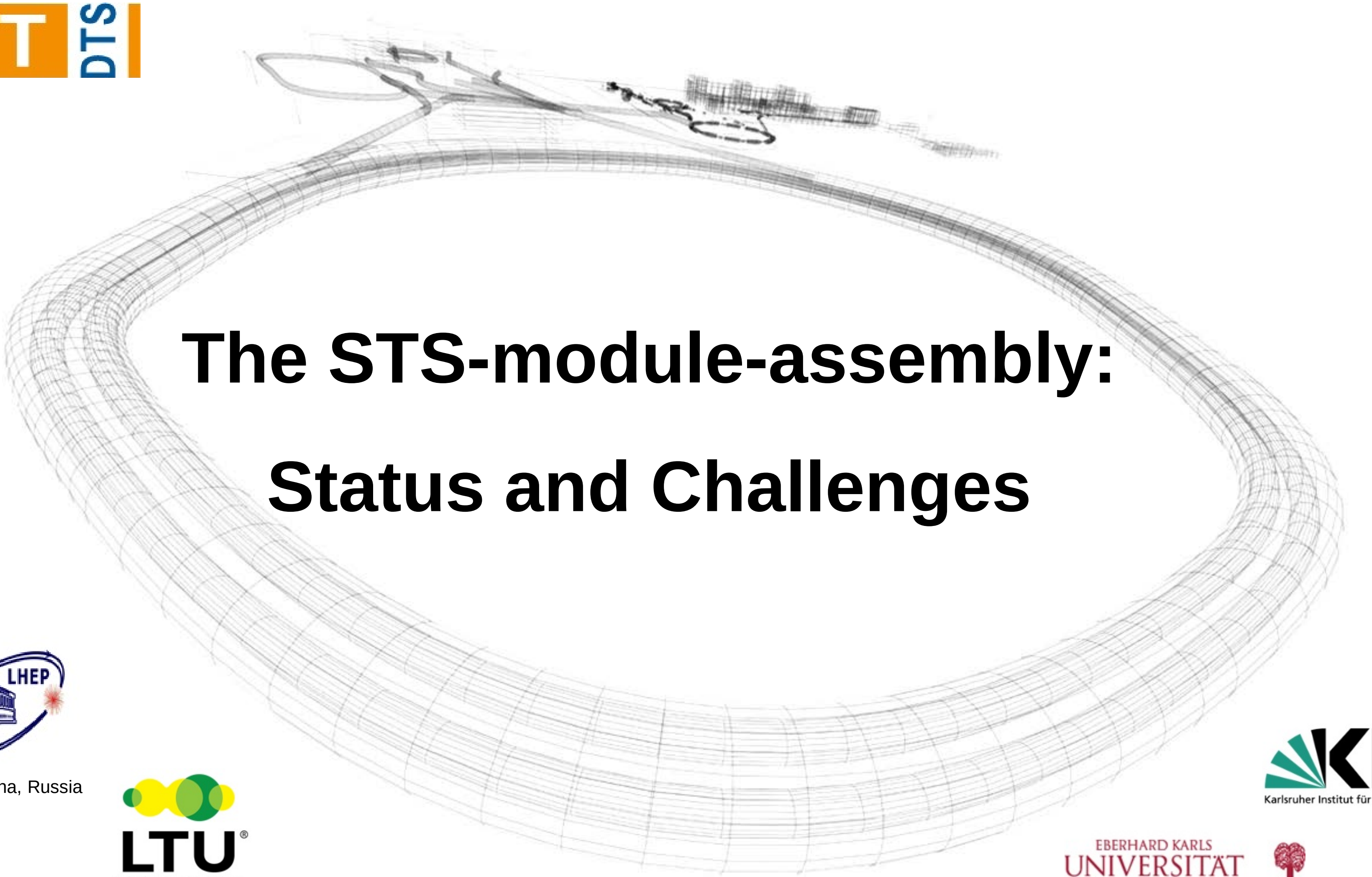
3. Annual MT Meeting

GSI Darmstadt, 31.1 – 2.2.17



The STS-module-assembly:

Status and Challenges

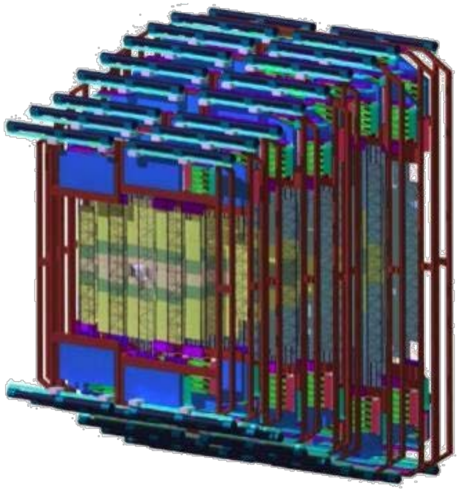
JINR/ Dubna, Russia

LTU Ltd/ Kharkov, Ukraine

contents

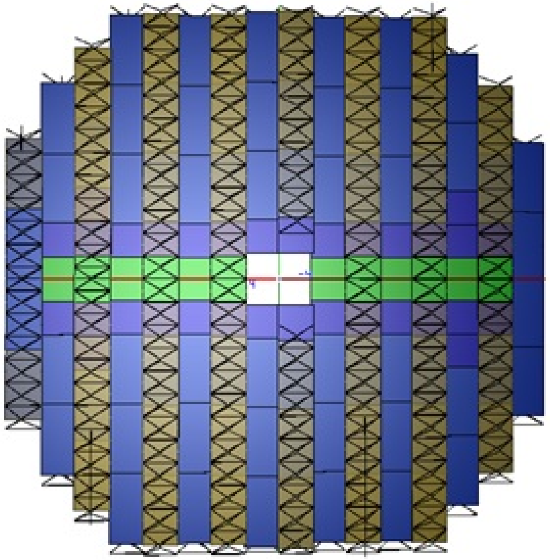
- the STS-module
- the module-components:
    - silicon sensors
    - signal transmission cables
    - ASIC´s and PCB´s
- the assembly-steps
- challenges:
    - yield of cables
    - QA-measurements
    - optimization of the alignment jigs
    - choice of glues

STS with 8 tracking stations

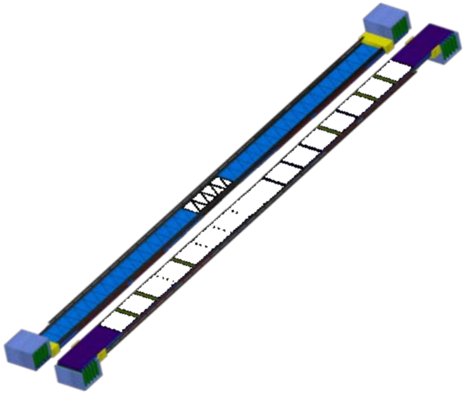


the CBM-
Silicon Tracking System

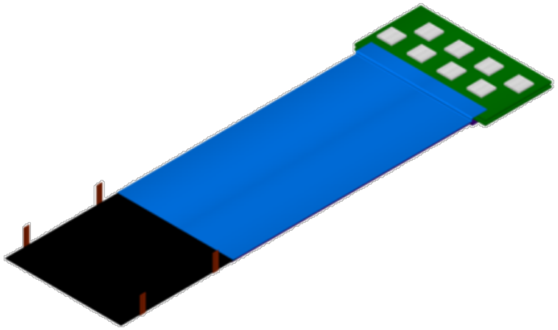
8 tracking stations



106 detector ladders

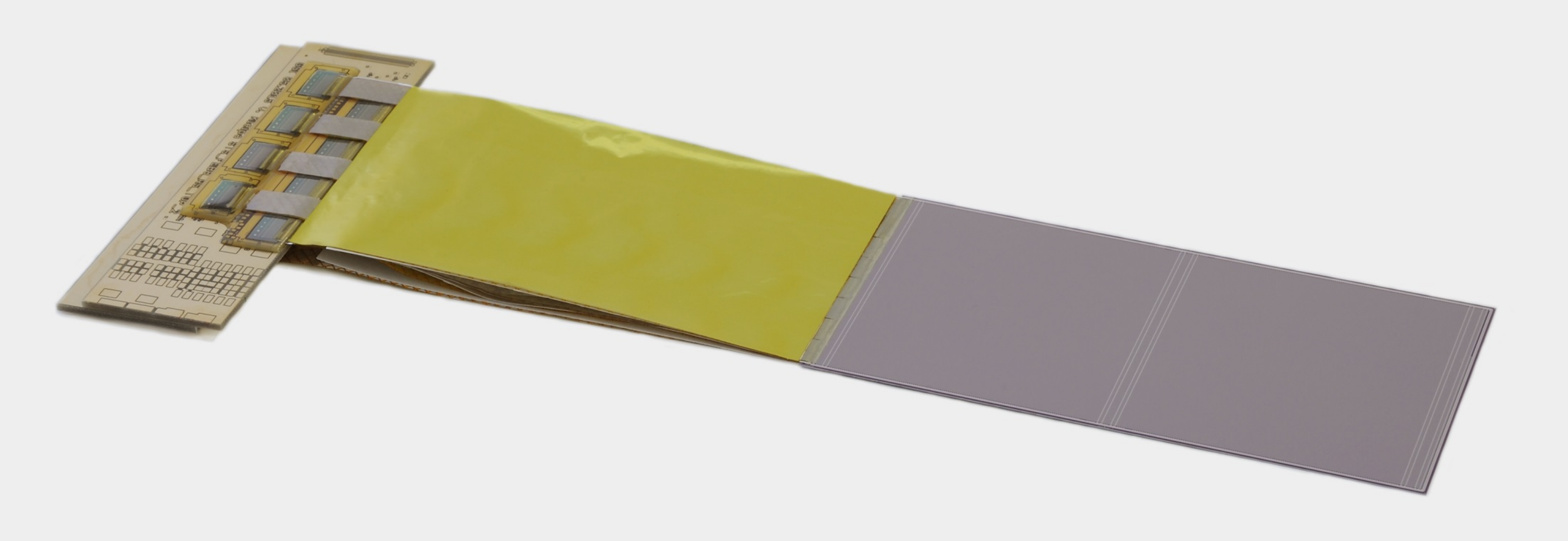


896 detector modules



The Silicon Tracking System (STS) is the core detector that provides track reconstruction and momentum determination of charged particles from beam-target interactions. It will consist of 8 tracking stations that are built from different types of basic functional modules which are mounted on carbon fiber ladders.

the Silicon-Sensor-Module



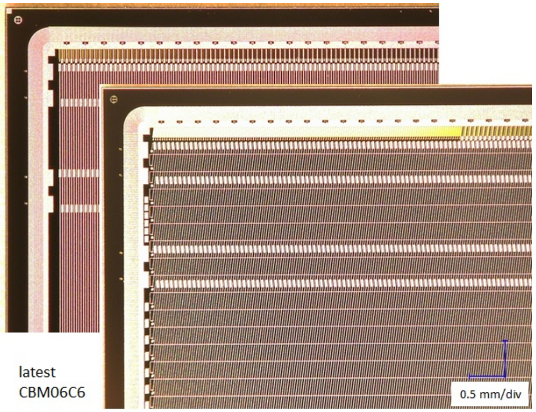
STS-module-components:

front-end-boards

signal transmission cable

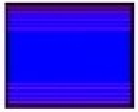
double-sided silicon microstrip sensor

the module-components: silicon-microstrip-sensors

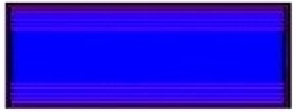


number of stripes: 1024
pitch of the stripes: 58 µm
pitch of the bond pads: 116 µm in two staggered rows

fill gaps at beam hole

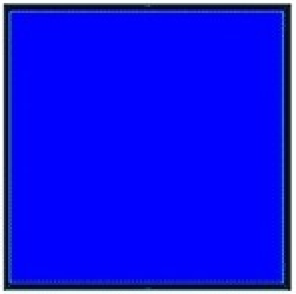


few sizes, small numbers

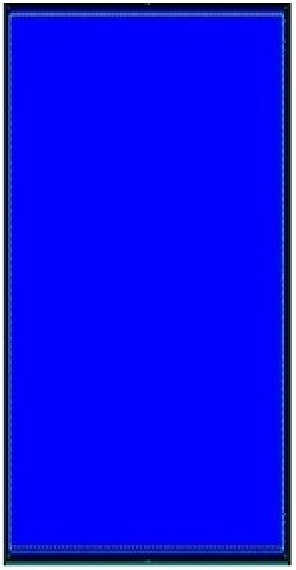


62 mm x 22 mm

62 mm x 42 mm



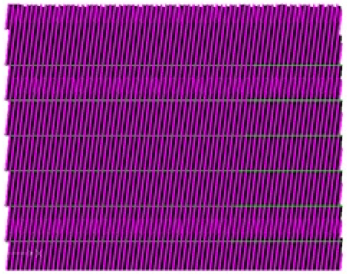
62 mm x 62 mm



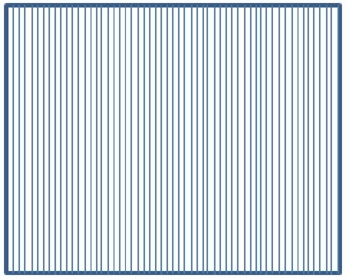
62 mm x 124 mm

strip orientation at 58 µm pitch

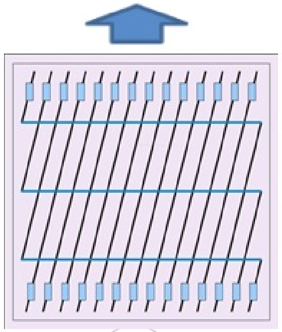
7.5 deg (front/p)



0 deg (back/n)



connectivity, r/o direction



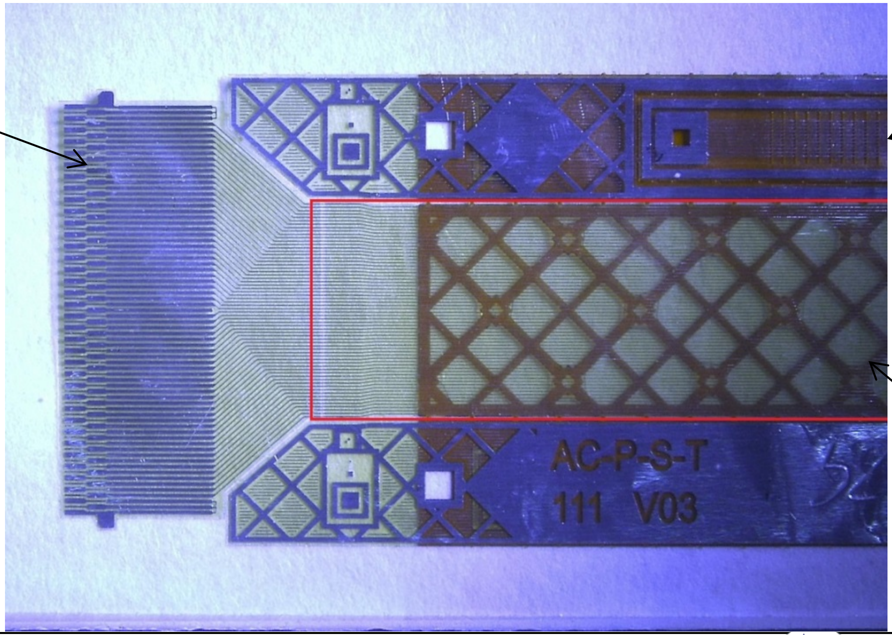
2nd metal interconnect required

the module-components:

signal transmission cable, version 1

version 1: Aluminum on Polyimide-cable from LTU/ Kharkiv, Ukraine

signal layer: 64 Al lines of 116 µm pitch, 14 µm thick on 10 µm Polyimide, lengths up to 500 mm



testfan

technological zone

red line: cutting line of the signal cable

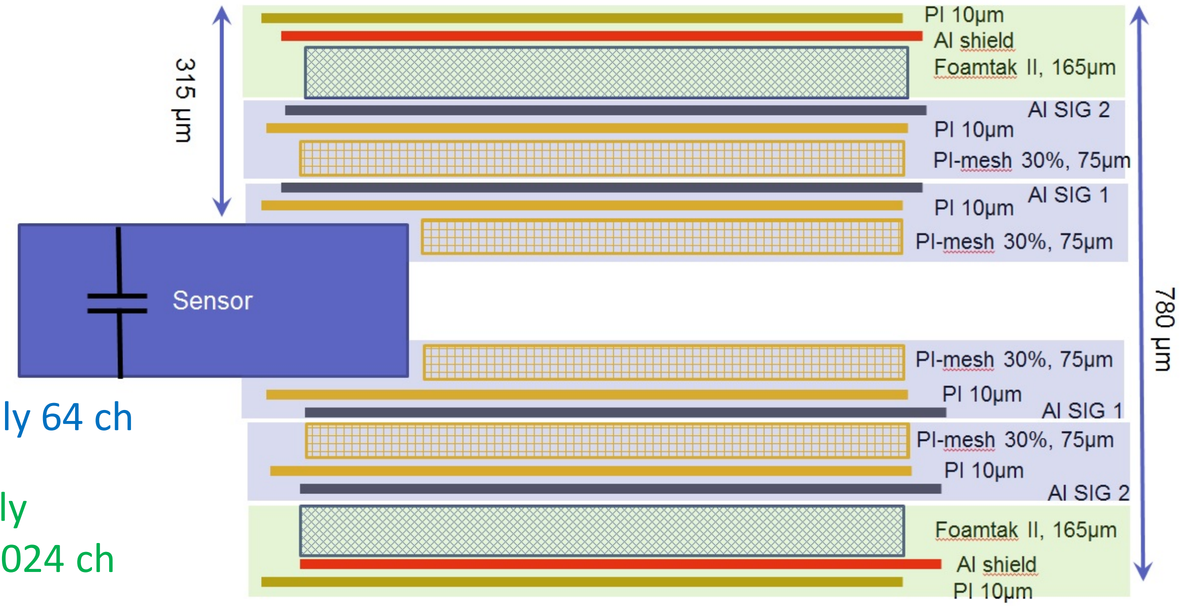
meshed spacer

A set of 32 microcables with different cable types is needed for one module!

the module-components:

signal transmission cable, version 1

microcable stack-up of version 1:



subassembly 64 ch

subassembly
full width 1024 ch

ε_r Foamtak II = 1,5

ε_r PI-meshed 30% = 1,75

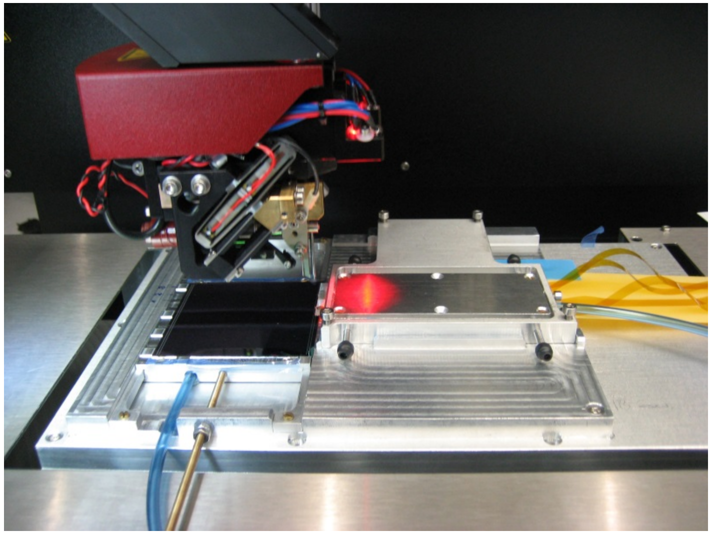
→ strip capacitance < 0,5 pF/cm

Additional spacers (PI-mesh) are placed between two signal layers to reduce the capacitance contributions from the adjacent connecting layers.
Shielding layers reduce the noise level and prevent shorting between the stacks of cables.

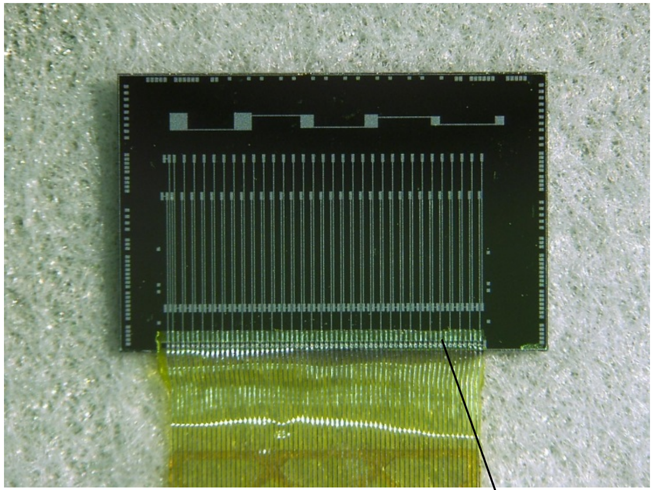
the module-components:

signal transmission cable, version 1

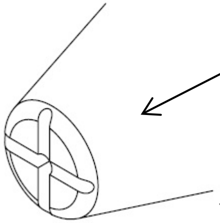
interconnection technology for version 1: TAB-bonding



TAB-bonding on the automatic bonder
F&K Delvotec G5

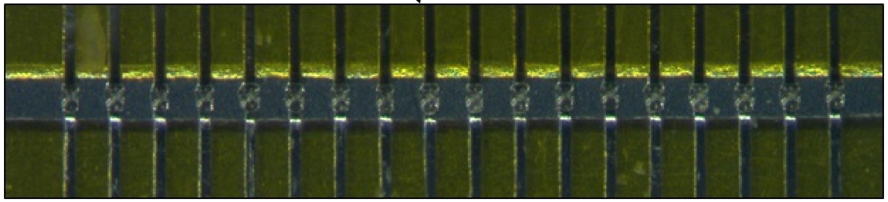


microcable TAB-bonded
to a dummy-ASIC



tip of the TAB-bondtool

Similar to a wirebonding-process TAB-bonding is a solid phase metal welding process using ultrasonic power and pressure to bond the Aluminum traces to the pads on the sensor or ASIC.



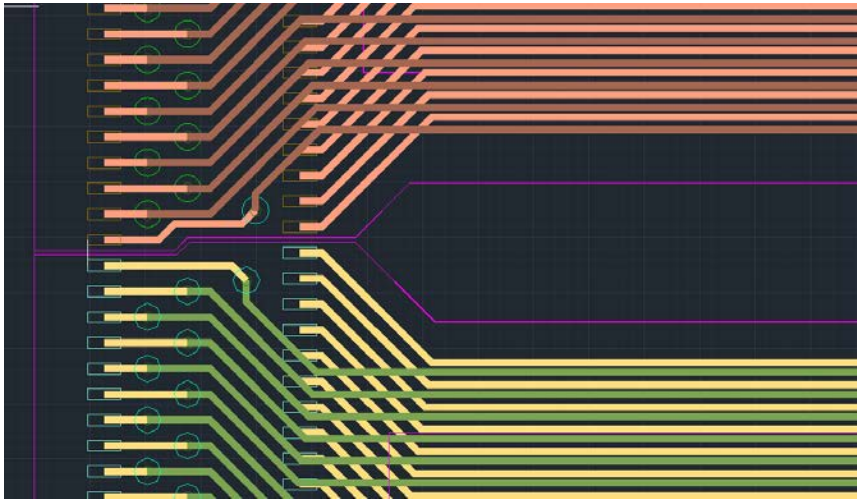
row of TAB-bonds

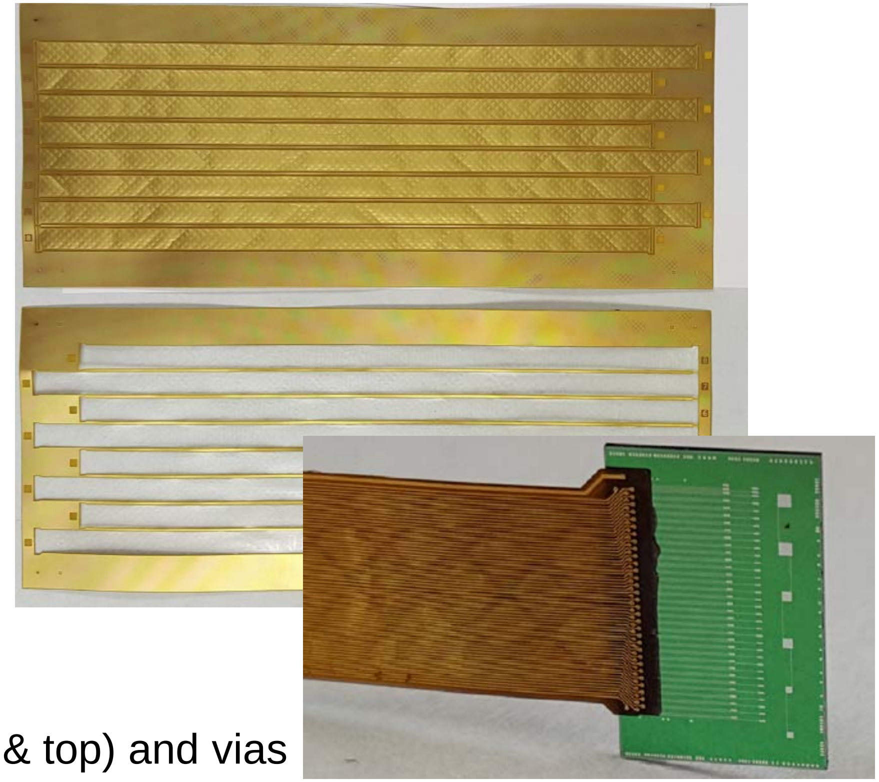
the module-components:

signal transmission cable, version 2

version 2: Copper-based microcables/
KIT-IPE (Dr. Thomas Blank & team)

As an alternative to the Aluminum-microcables a R&D-project has been started that investigates Copper-based cables.





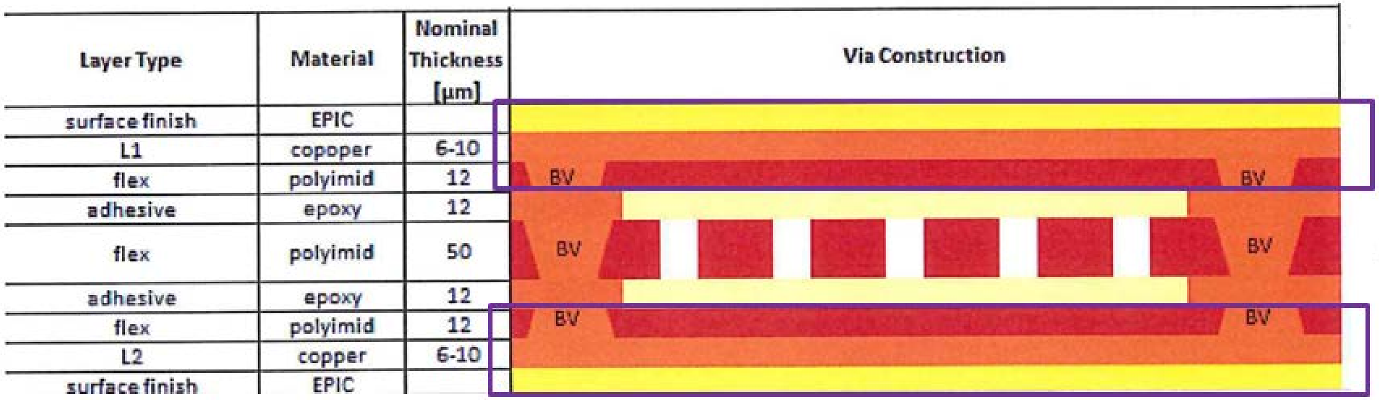
Benefits of Copper:

- well known in PCB-Flexboard technology
- offers interconnected multilayer solutions
  - ⟹ one cable with two layers (bottom & top) and vias instead of two single Al-cables

the module-components:

signal transmission cable, version 2

build-up of micro-copper-cable of version 2:



Layer Type	Material	Nominal Thickness [µm]	Via Construction
surface finish	EPIC		
L1	copopper	6-10	
flex	polyimid	12	
adhesive	epoxy	12	
flex	polyimid	50	
adhesive	epoxy	12	
flex	polyimid	12	
L2	copper	6-10	
surface finish	EPIC		

Layer 1

Spacer

Layer 2

→ two copper layers L1/L2 with spacer (30% filling), laminated to one cable, electrically interconnected

surface finish: EPIG (Electroless Palladium, Immersion Gold**),**
thin (300 nm) noble surface for soldering and bonding in contrast to standard ENIG (5..7µm) (-> Pitch), Palladium serves as a highly efficient diffusion barrier

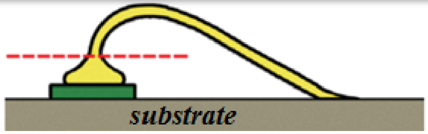
→ strip capacitance < 0,8 pF/cm

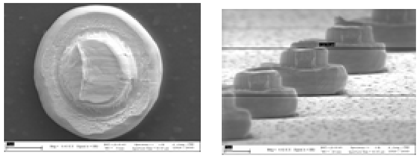
the module-components:

signal transmission cable, version 2

interconnection technology for version 2: Au-stud bumps + flip-chip

Ball - wedge gold wire bonding

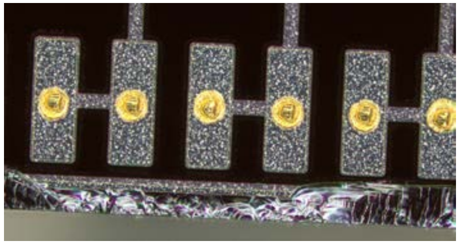




Gold-Stud bumps

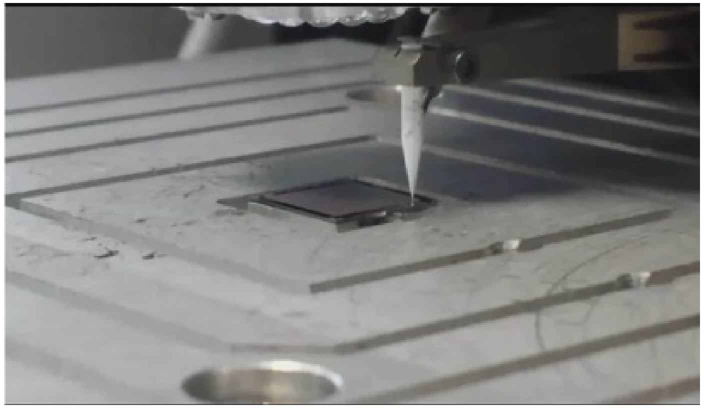
Source: J. Jordan – Gold-Stud bumps in flip-chip applications

→

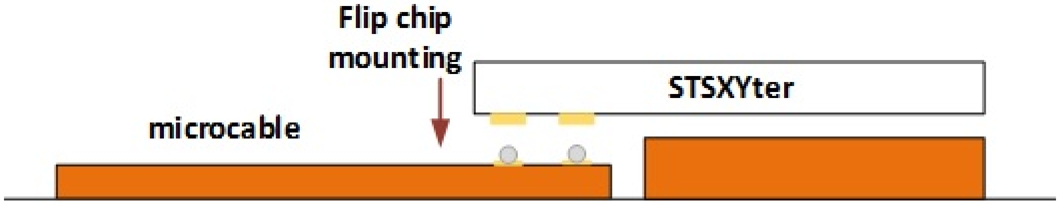


Au-Stud bumps on STSXter-Testchip

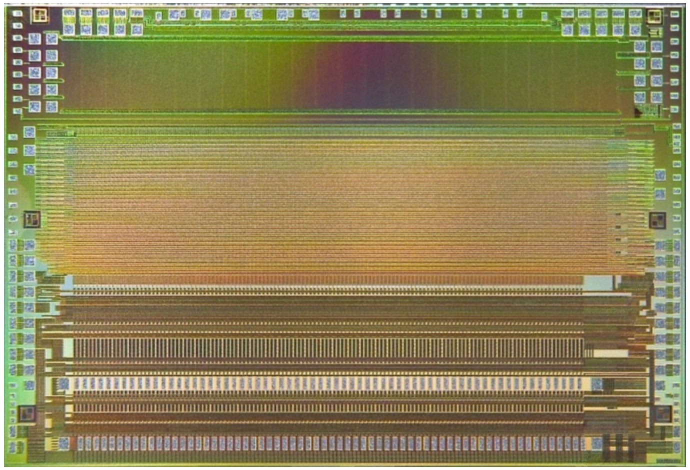
- *reliable and fast process*



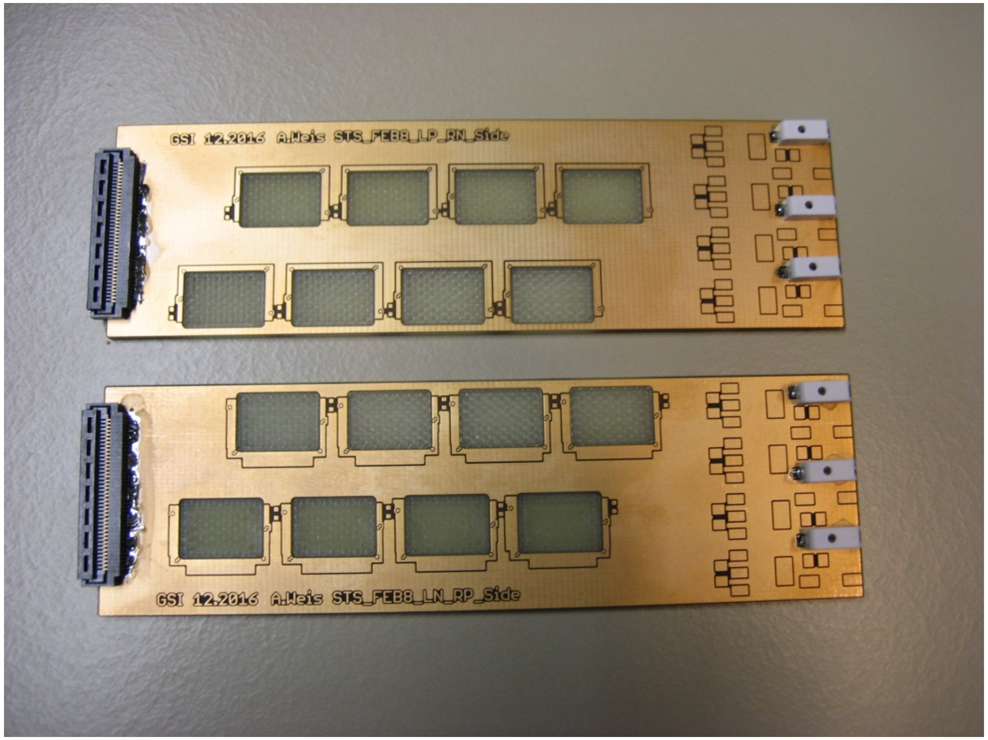
Ball-Wedge-Bonder



the module-components: front-end-boards



STS-XYTER-ASIC
with 128 channels and pitch of 116 µm
(same as the sensor bond pad pitch),
16 pcs. are necessary for one module



8-STS-XYTER-board
(dummy-PCB with power and signal connectors),
2 different pcs. are necessary

workflow for the module-assembly for the microcables/ version 1 from LTU

The workflow for the module-assembly consists of four main steps:

TAB-bonding of the microcables to the STS-XYTER-ASIC´s

⇩

TAB-bonding of the microcables to the silicon sensor

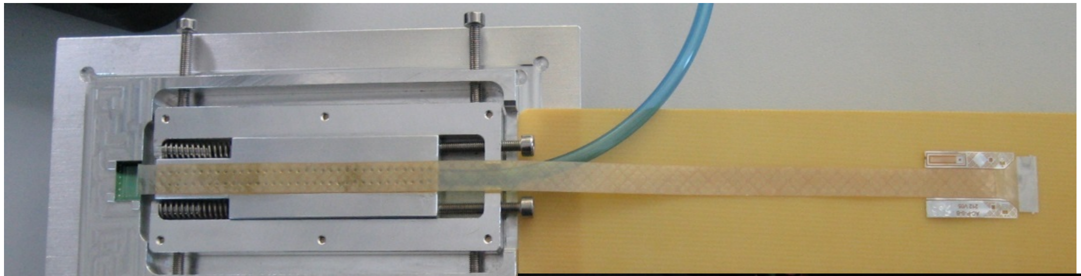
⇩

die- and wirebonding of the STS-XYTER-ASIC´s to the PCB-rows

⇩

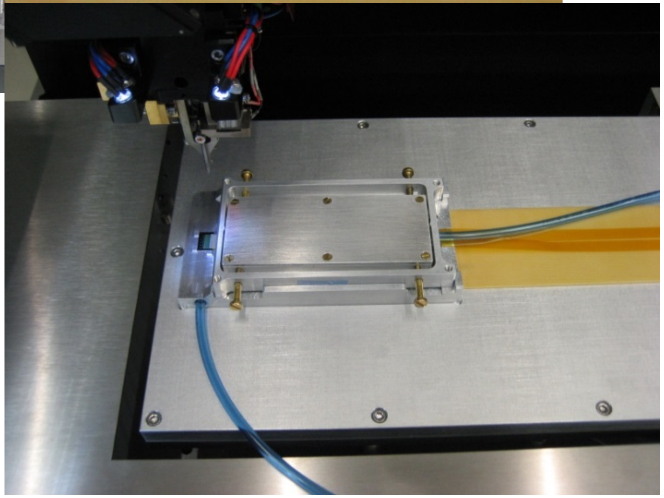
glueing of shielding- layers and spacers

assembly-step 1: TAB-bonding of the microcables to the STS-XYTER-ASIC´s

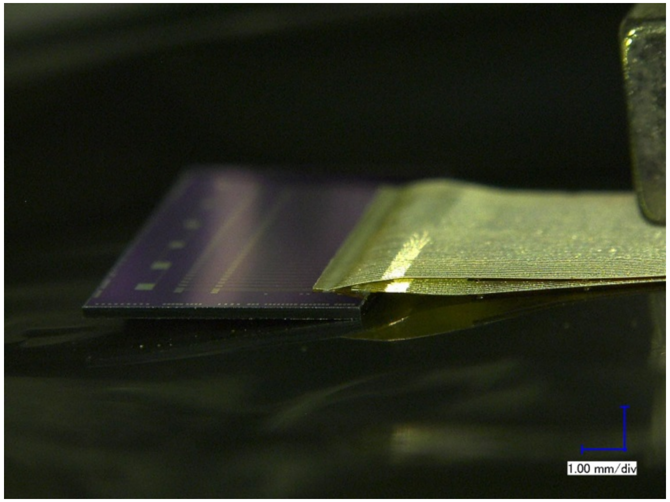


↑ fixing of the microcable with vacuum and alignment

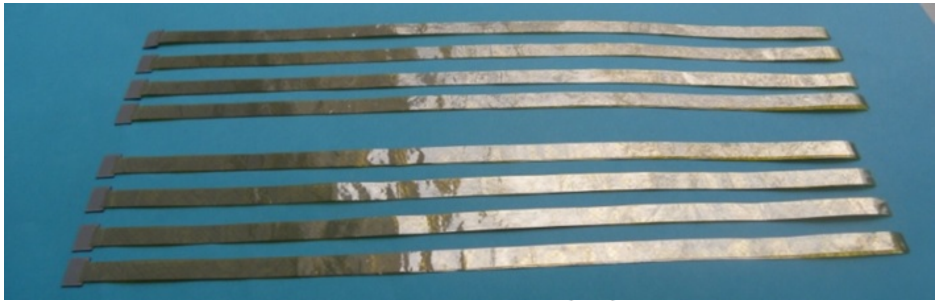
TAB-bonding →



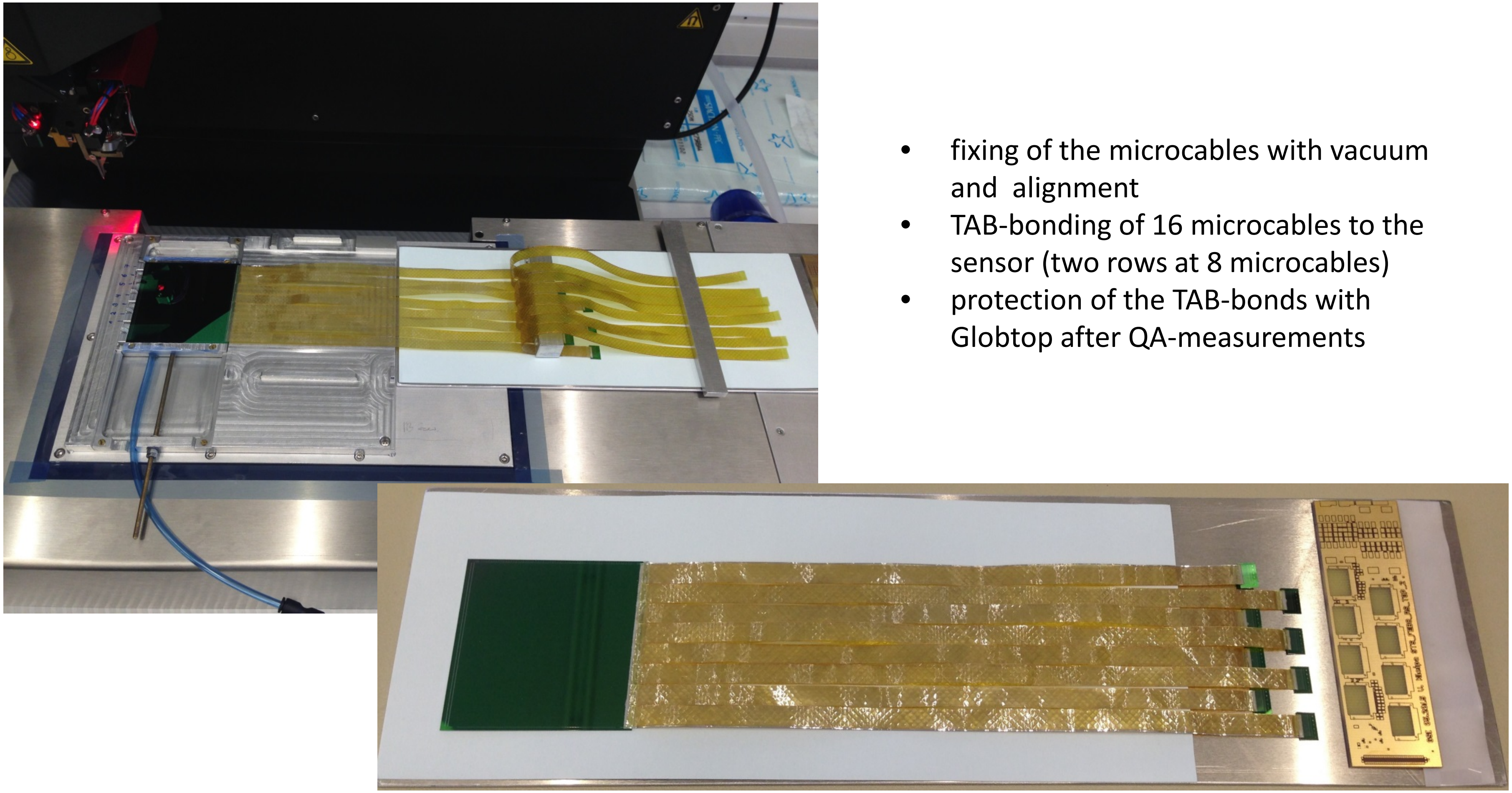
two layers of microcables, TAB-bonded to a dummy-ASIC and protected with Globtop after QA-measurements ↓



bottom and top layer of the microcables,
TAB-bonded to the 8 STS-ASICs for one sensor side →



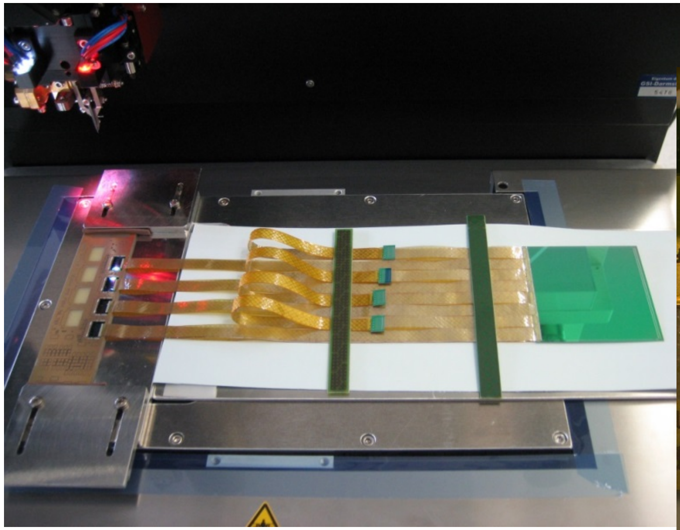
assembly-step 2: TAB-bonding of the microcables to the silicon sensor



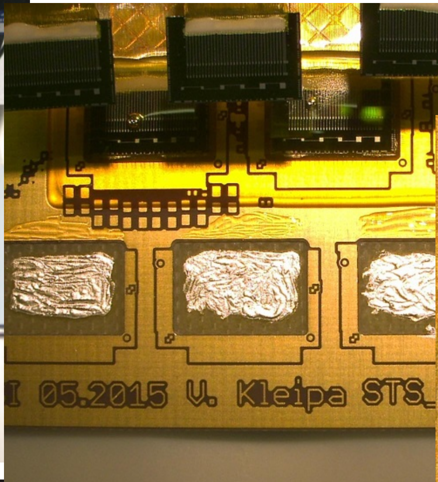
- fixing of the microcables with vacuum and alignment
- TAB-bonding of 16 microcables to the sensor (two rows at 8 microcables)
- protection of the TAB-bonds with Globtop after QA-measurements

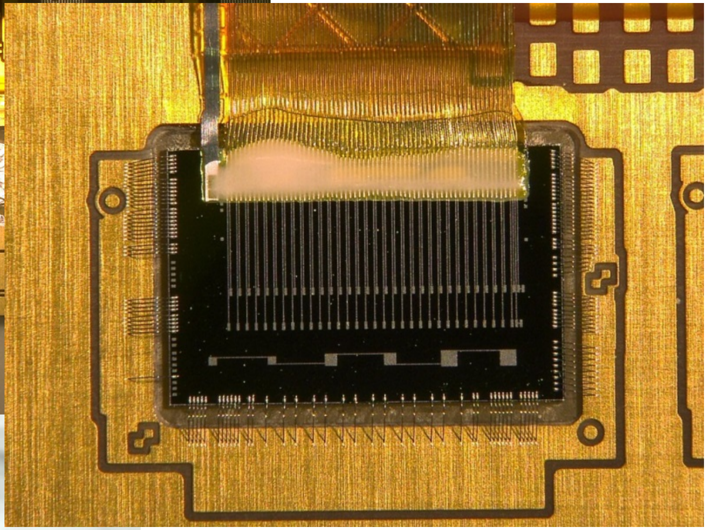
<u>assembly-step 3:</u> die- and wirebonding of the STS-XYTER-ASIC´s to the PCB-rows

wire-bonding of the STS-YTER-ASIC´s ↓



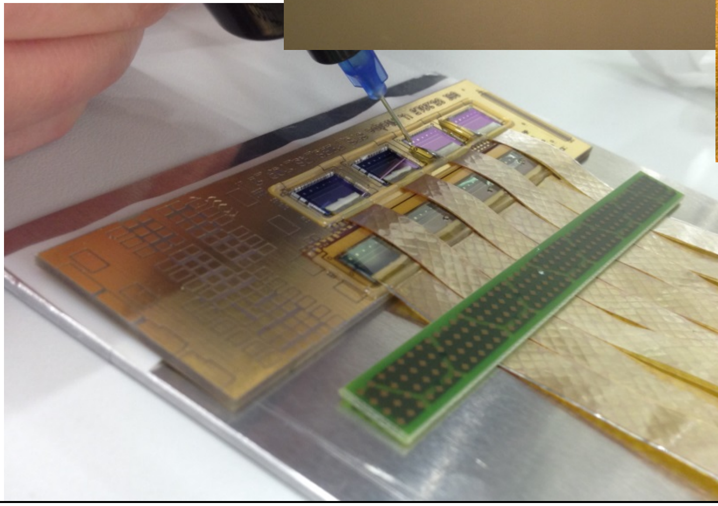
die-bonding of four ASIC´s for the 2nd row ↓



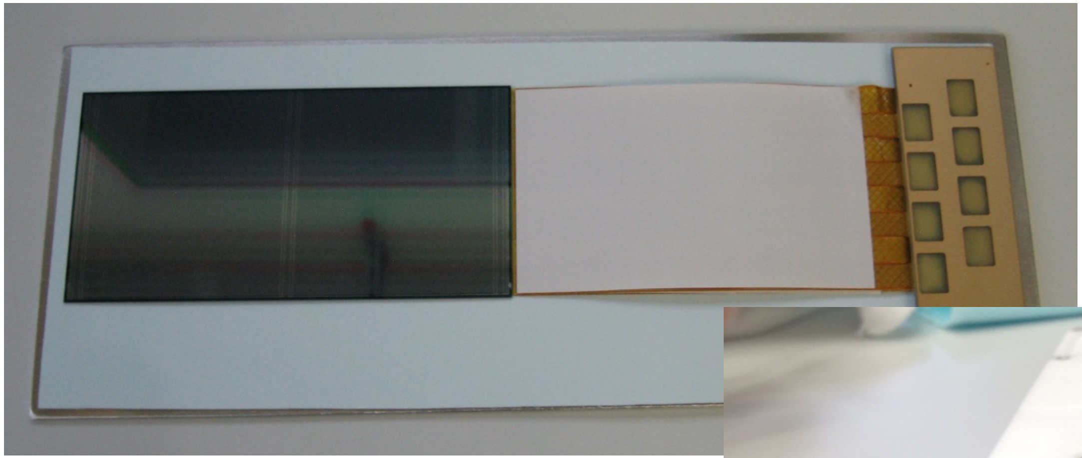


↑ wire-bonded STS-XYTER-ASIC

application of Globtop after QA-measurements



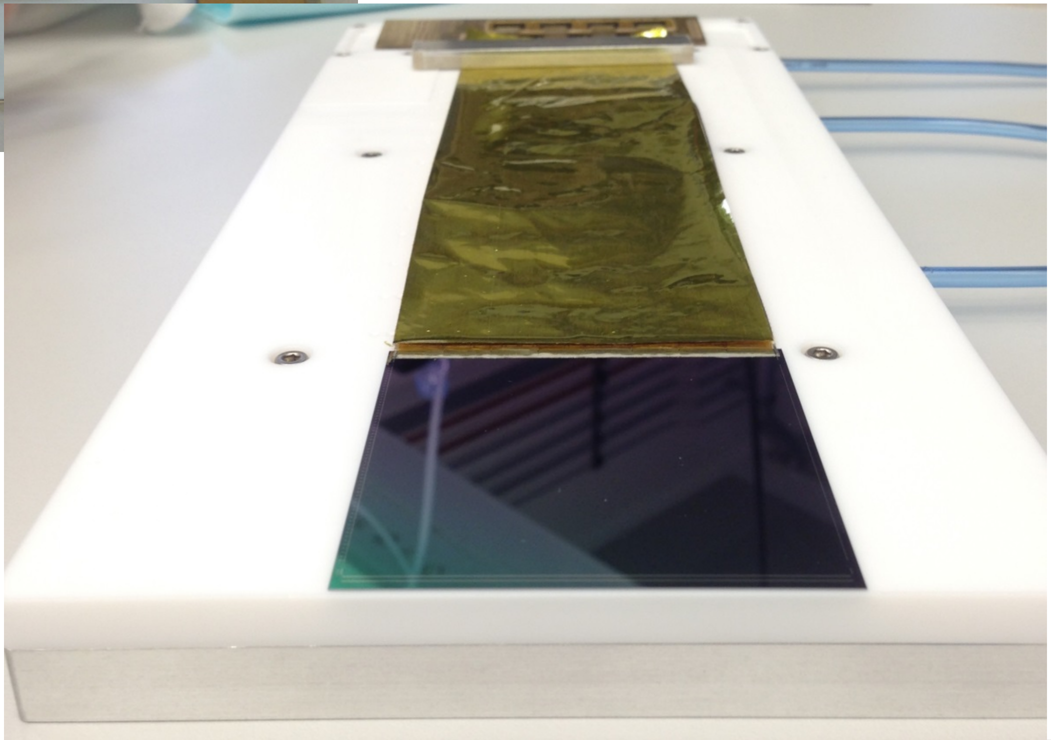
assembly-step 4: glueing of shielding-layers and spacers



← glueing of foamtak-spacer

glueing of shielding

↓



This semi-module then has to be turned to the n-side of the sensor and the steps have to be repeated!

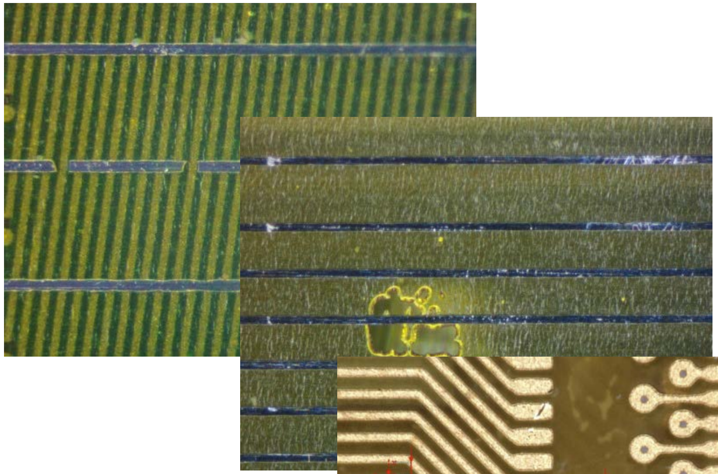
challenges:

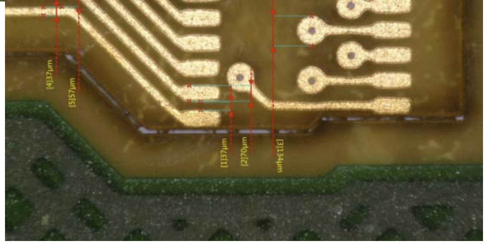
yield of cables

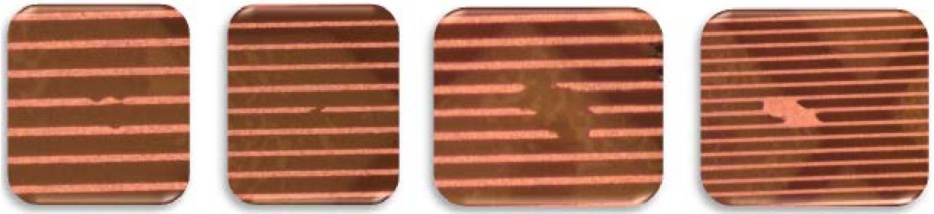
Since the microcables are very delicate objects with fine structures, the manufacturing processes are complex and can cause failures.

For the Aluminum microcables the yield decreases with the cable length. Yield improvements can be achieved by:

- using photomasks with higher resolution
- using better equipment
- using advanced raw material
- improvement of photolithography process
- improvement of etching parameters



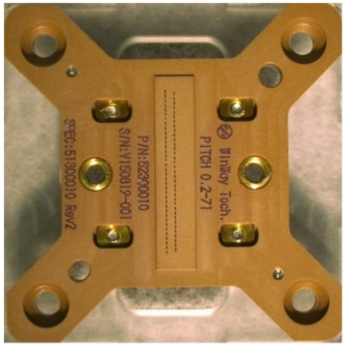


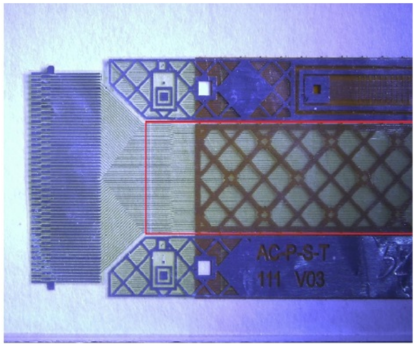


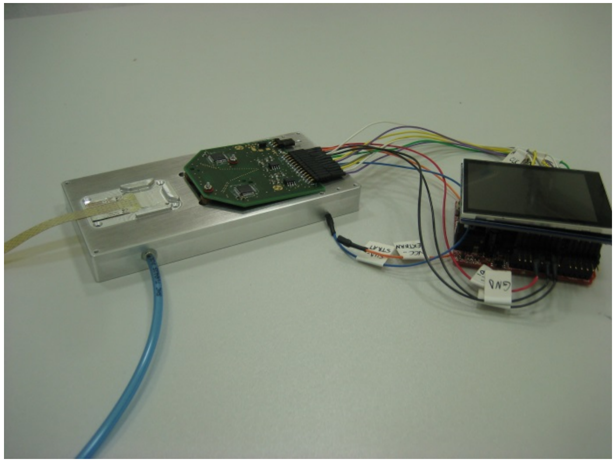
challenges:

QA-measurements

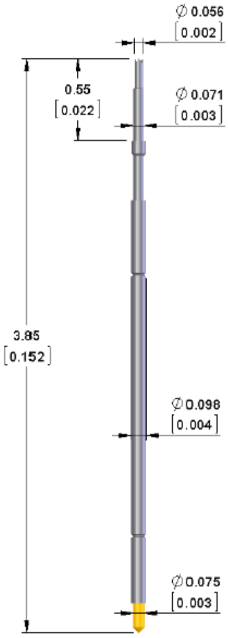
testsocket for the ASIC-TAB-bonds



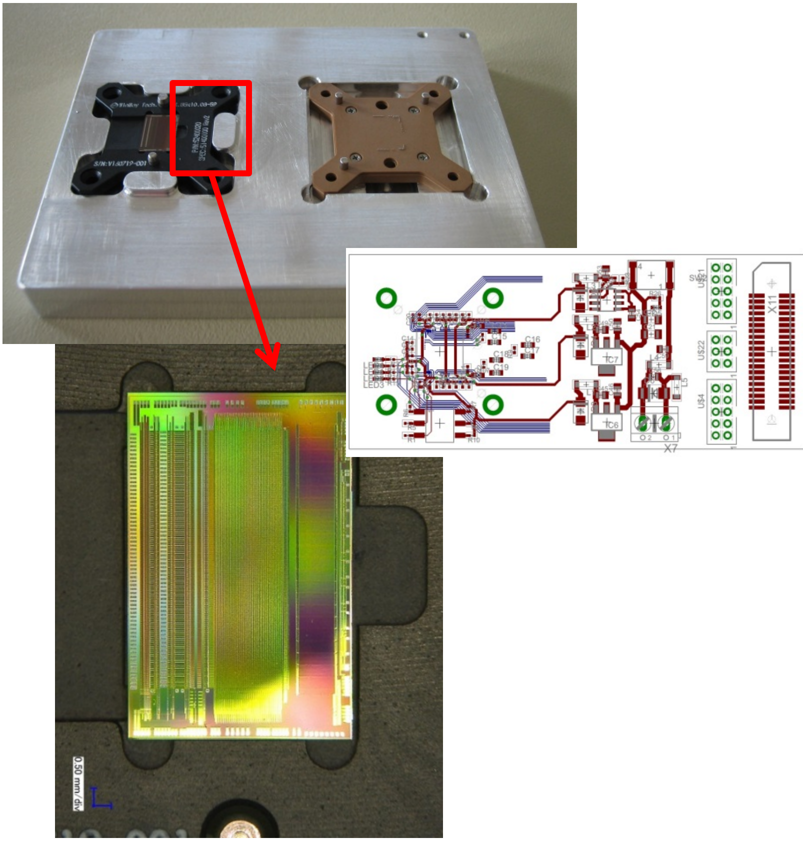




testsocket for the sensor-TAB-bonds



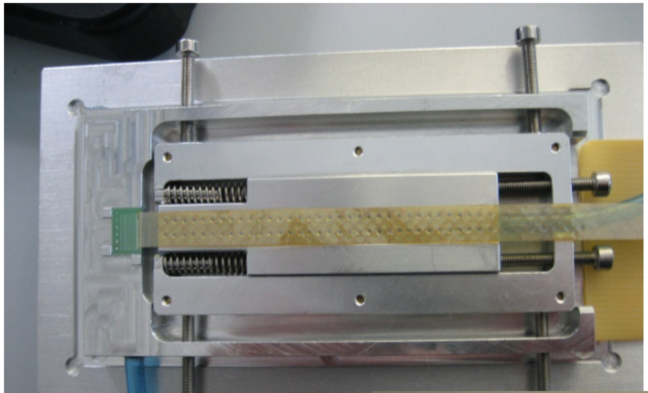
Pogo-pin



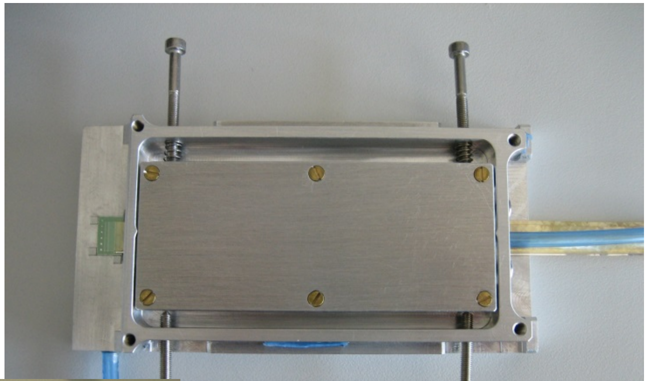
PCB´s, software and test procedures are still under development

challenges:

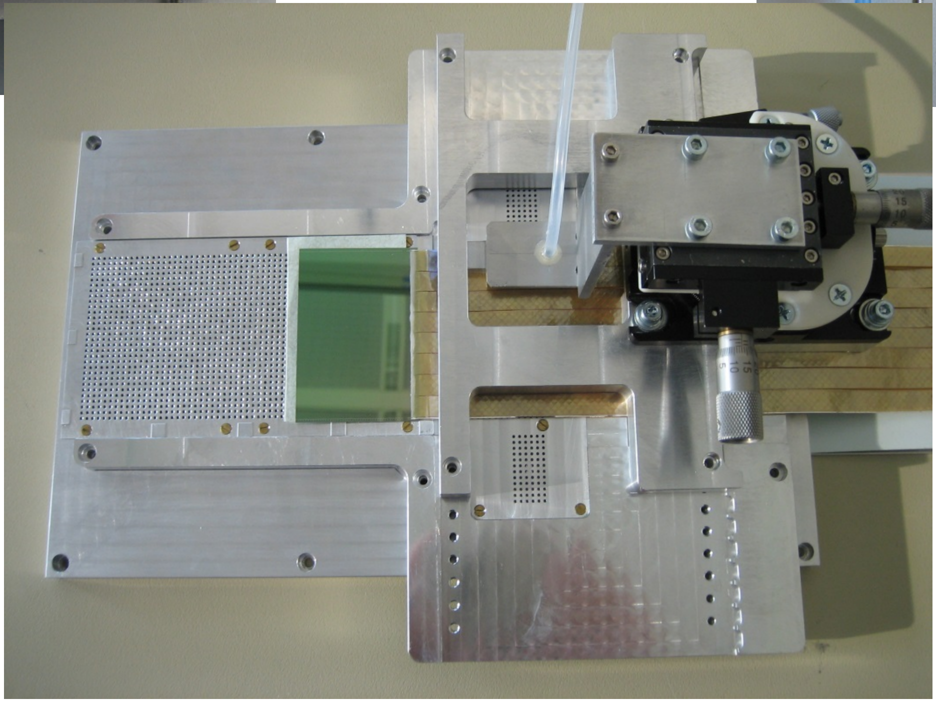
optimization of the alignment jigs



jig for bonding the 1st microcable layer on the ASIC



jig for bonding the 2nd microcable layer on the ASIC



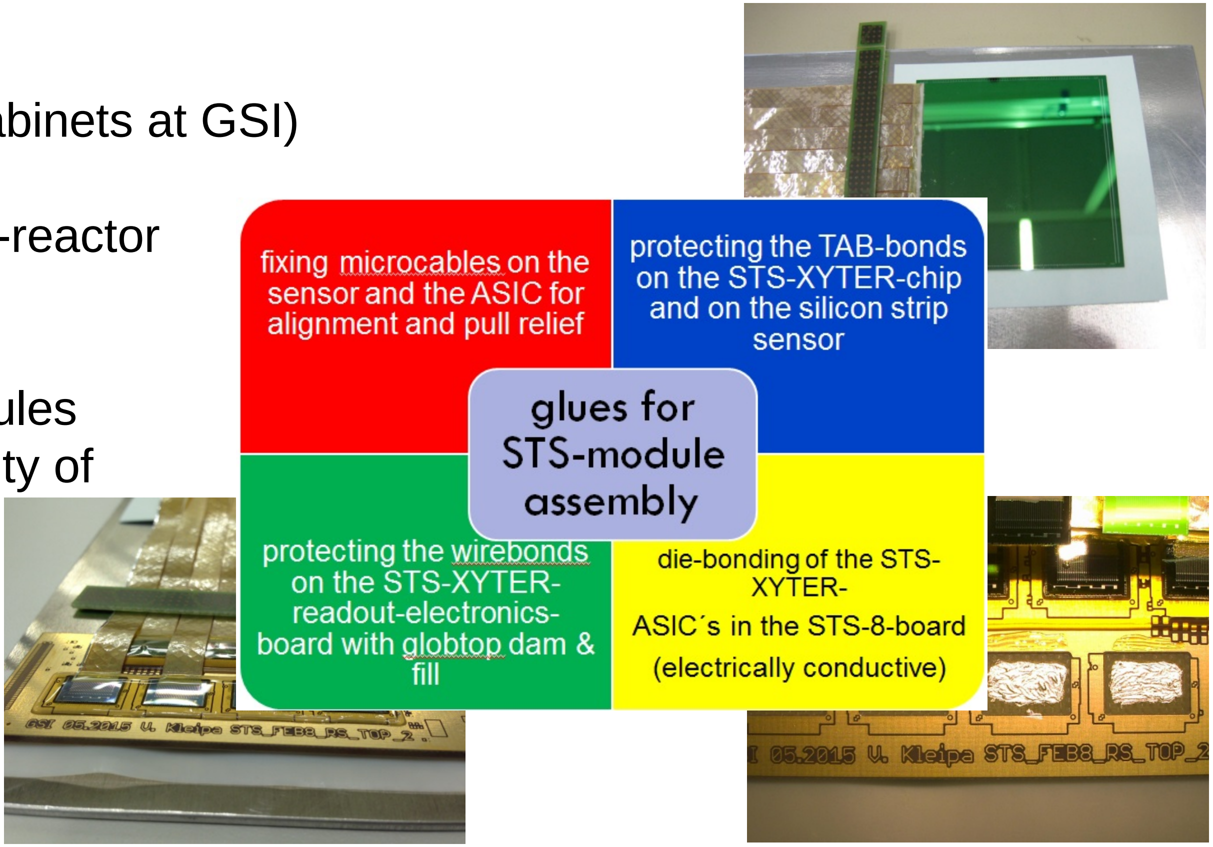
jig for bonding the microcables on the sensors

challenges:

choice of glues

To investigate the suitability of all the used glues for the STS-module-assembly several tests are necessary with regard to aging and radiation hardness:

- thermal cycles (in climate cabinets at GSI)
- irradiation tests (in the Triga-reactor at Mainz University)
- electrical tests with testmodules to assure that the functionality of the modules isn´t affected by the glue



glues for STS-module assembly

fixing microcables on the sensor and the ASIC for alignment and pull relief

protecting the TAB-bonds on the STS-XYTER-chip and on the silicon strip sensor

protecting the wirebonds on the STS-XYTER-readout-electronics-board with globtop dam & fill

die-bonding of the STS-XYTER-ASIC´s in the STS-8-board (electrically conductive)

Thank you for your attention!