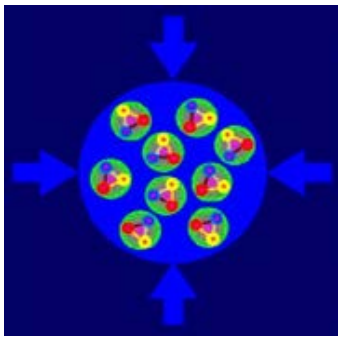
The CBM Silicon Tracking Station and CBM-related ASIC developments

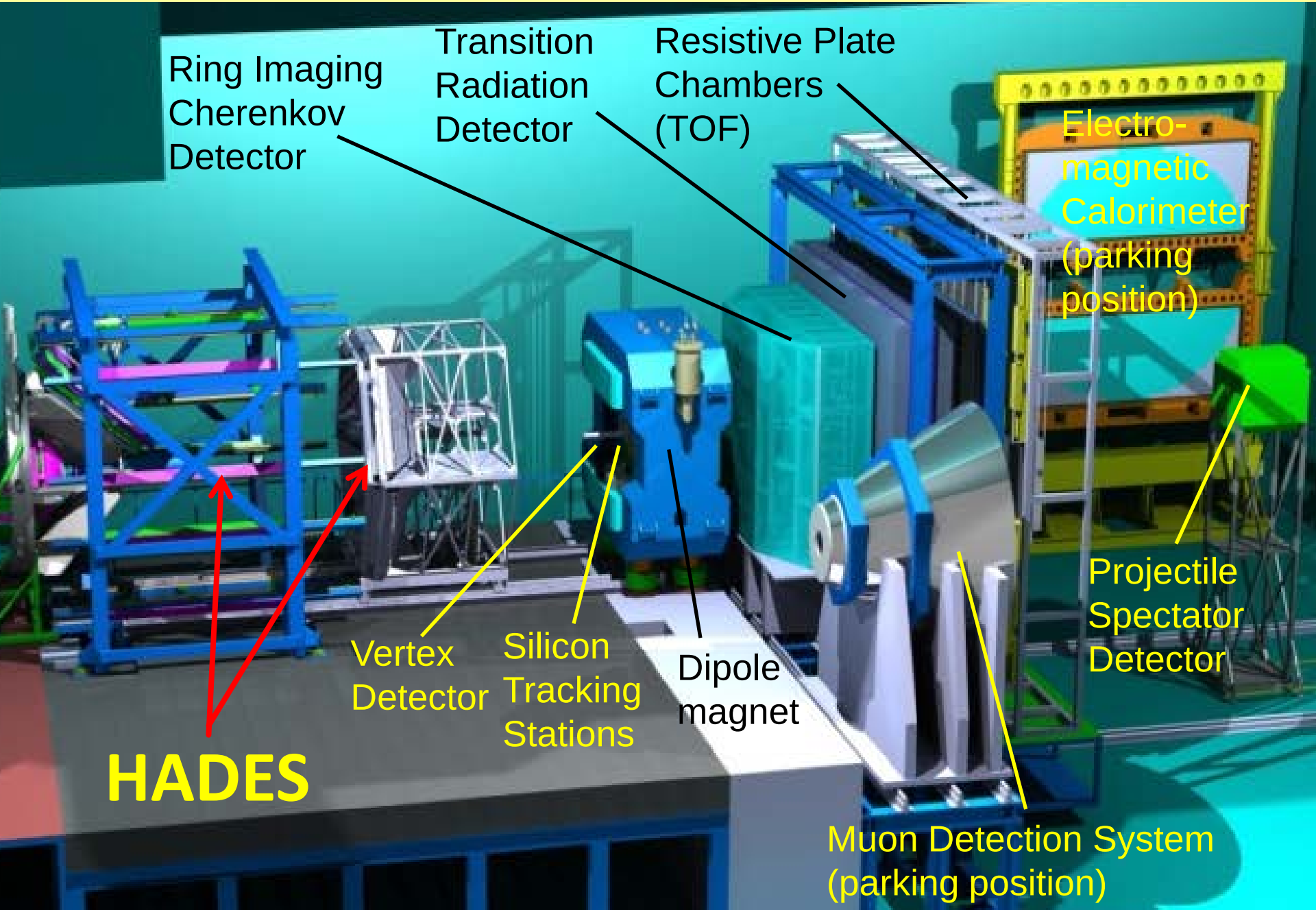
Christian J. Schmidt

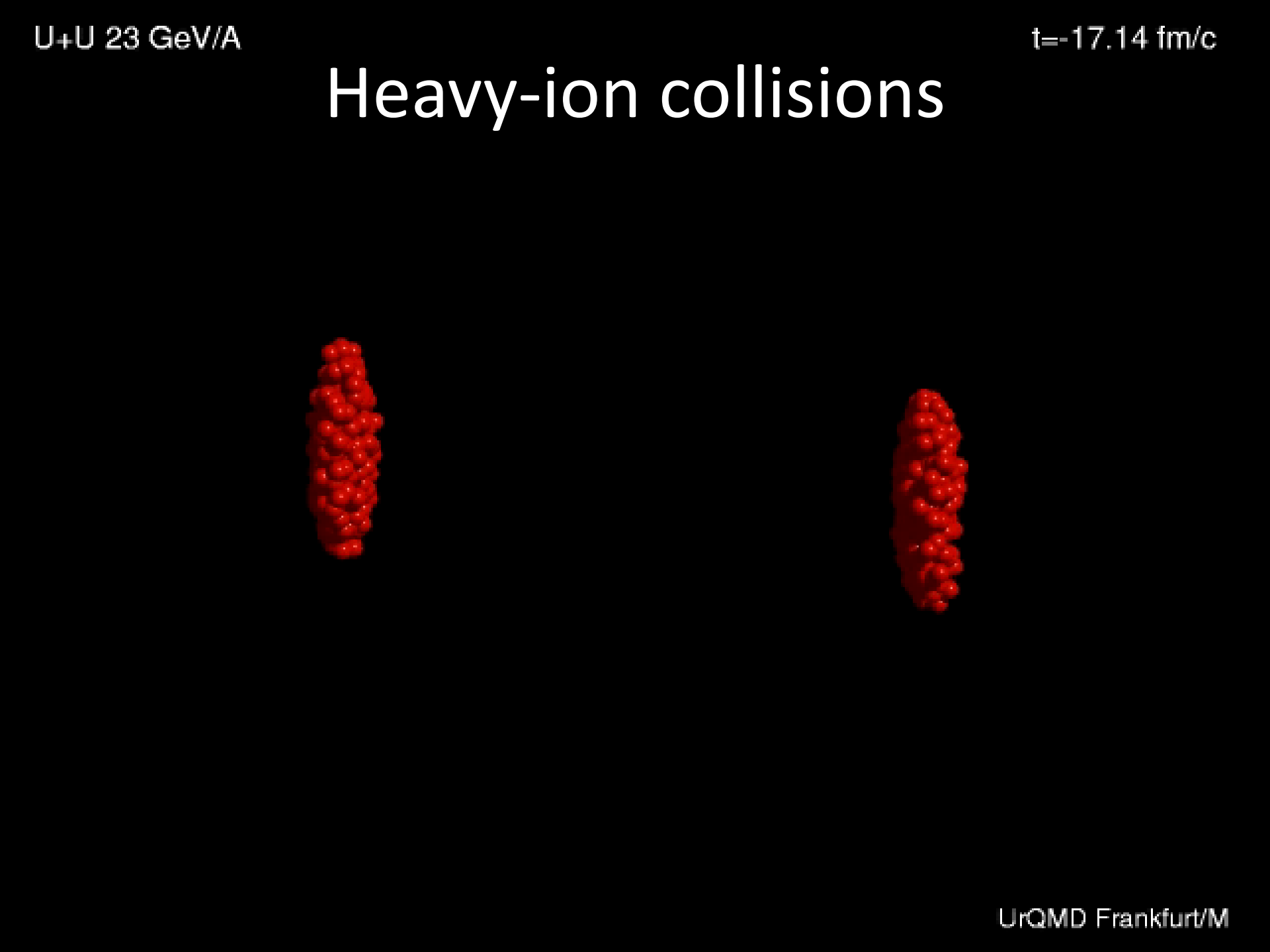
3rd Annual MT Meeting

Jan. 31st to Feb. 2nd, 2017, GSI, Darmstadt, Germany

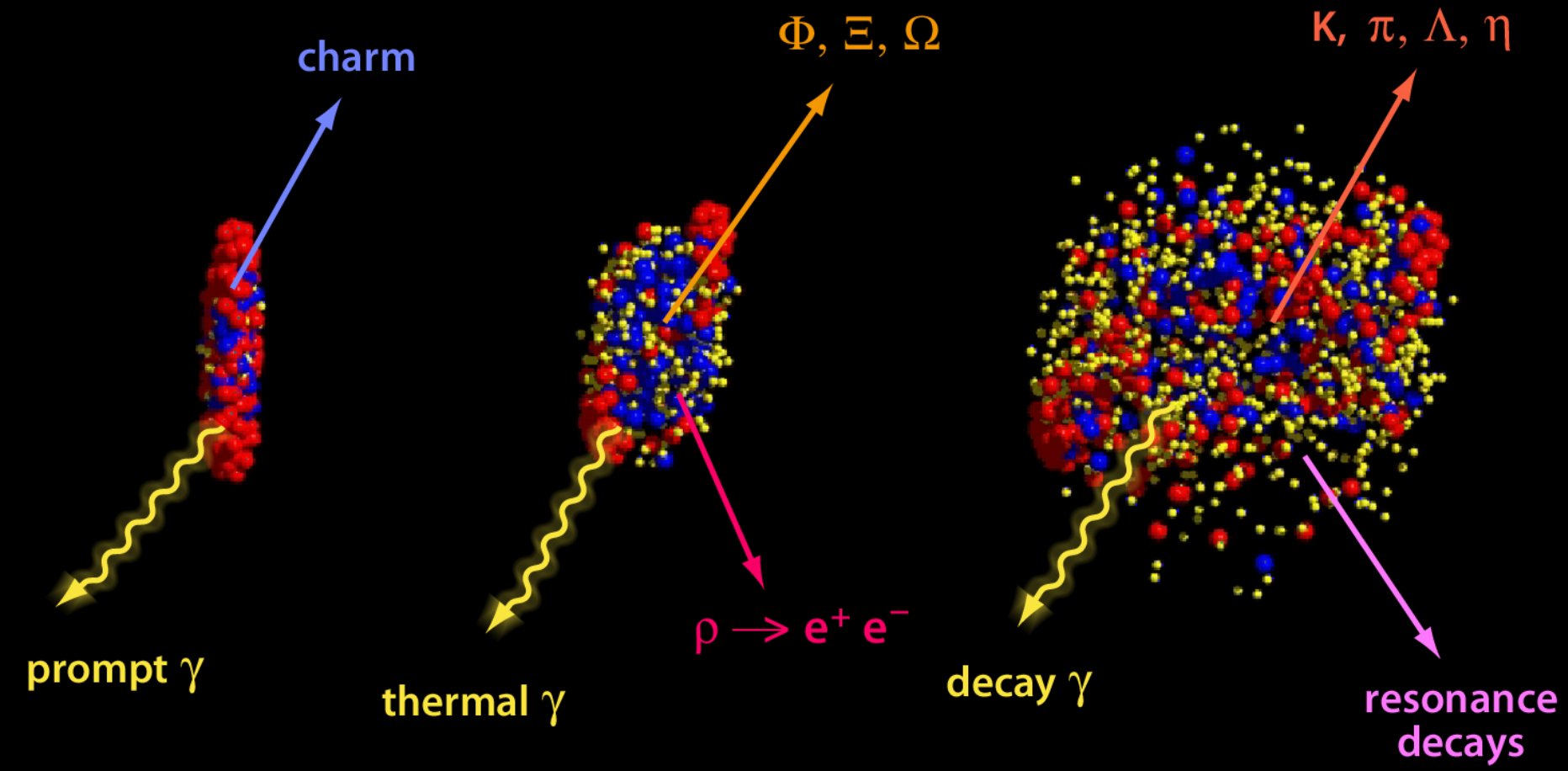


The Compressed Baryonic Matter Experiment

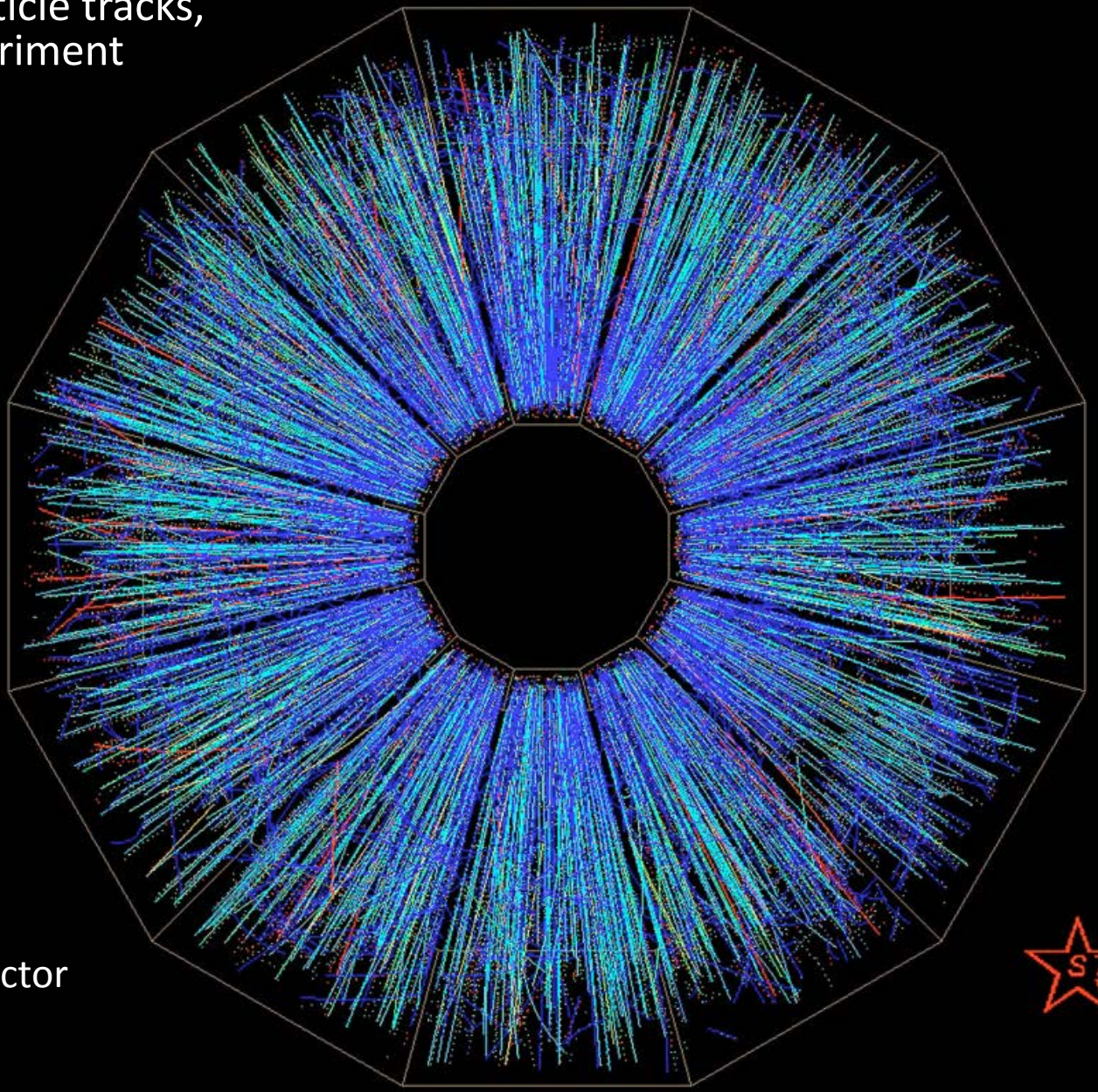



U+U 23 GeV/A
t=-17.14 fm/c
Heavy-ion collisions
UrQMD Frankfurt/M

Diagnostic probes



Charged-particle tracks, collider experiment



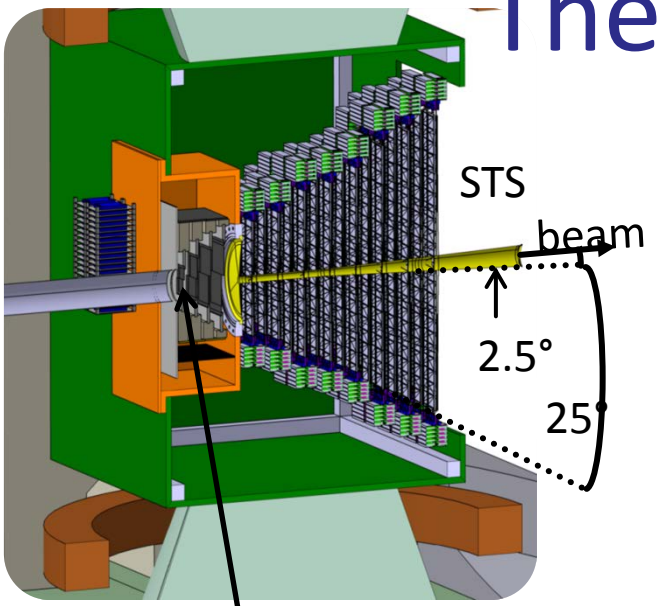
TPC detector

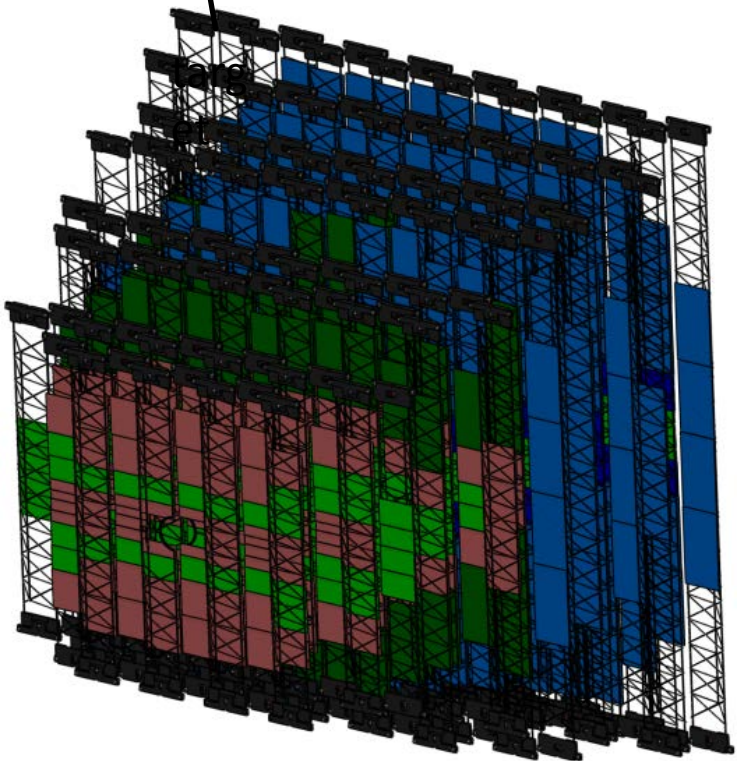
CBM technological challenges

fixed target configuration makes 10MHz Au+Au interaction rate feasible at FAIR

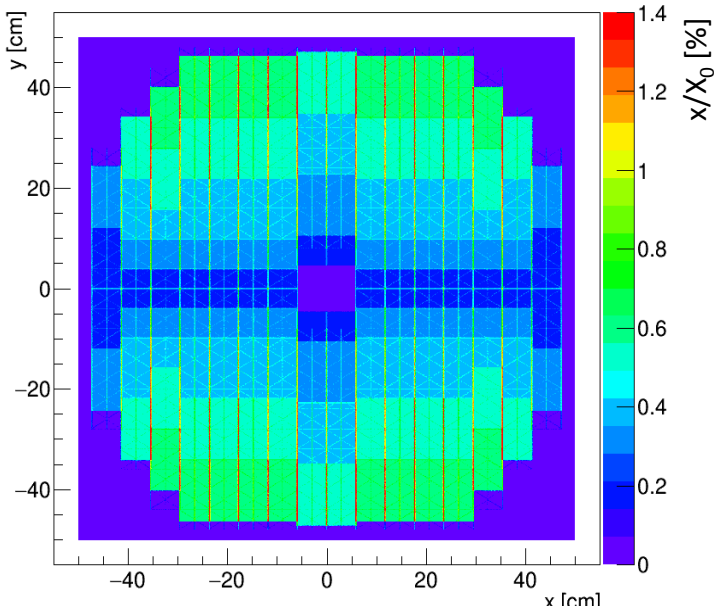
- determination of (displaced) vertices ($\sigma \approx 50\ \mu m$)
- identification of leptons and hadrons
- fast and radiation hard detectors
- free-streaming readout electronics
- high speed data acquisition and high performance computer farm for online event selection
- 4-D event reconstruction

The Silicon-Tracking-System





- Low-mass micro cables from sensor to FEE
- selftriggering ASIC readout
- 1.8 Mio channels, cooling power ~ 40 kW

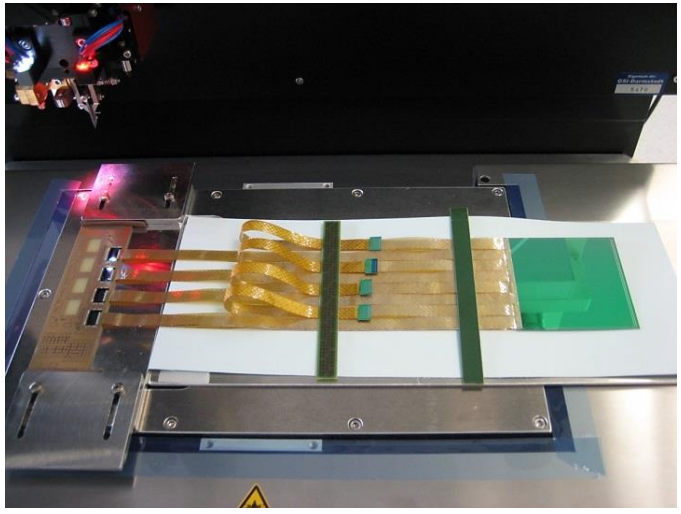


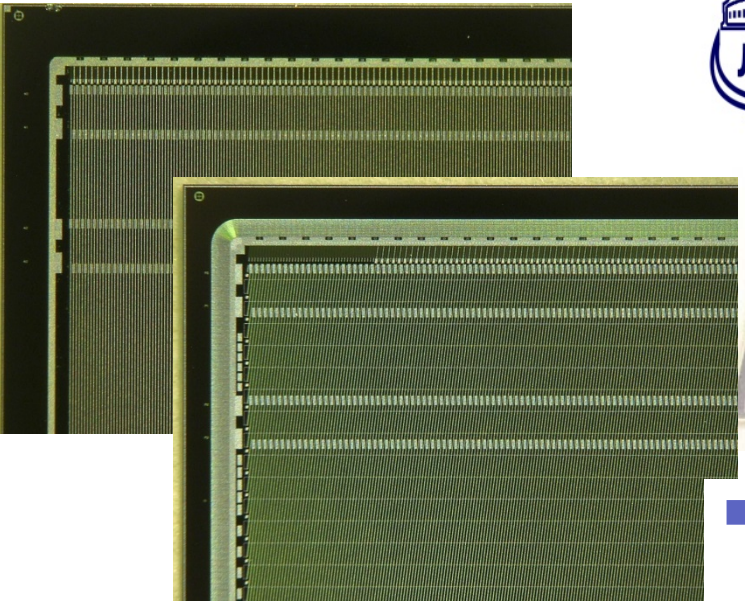
material budget per station

- ~ 3 sqm active sensor area
- double sided strips 7.5°, 58µm pitch
- 8 Stations,
- 106 ultra-light carbon ladders
- 896 Sensor modules

Assembly of double sided strip detector modules, a collaborative effort → talk by Carmen Simons

- prototyping ongoing





- Topical workshop on radiation induced surface effects in silicon detectors, Oct. 2016 at KIT

CBM-related Chip Developments and Options

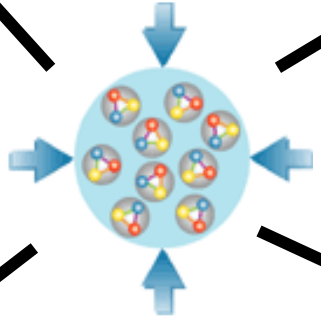
PADI for Diamond
M. Ciobanu, ISS

PADI for TOF
M. Ciobanu, ISS Bucharest

GET-4 TDC (TOF)
H. Flemming, H. Deppe, GSI

CBM MuCH XYTER
E. Atkin et al, MEPhI

CBM STS-XYTER/MuCH-XYTER
AGH Krakow, R. Szczygiel et al



CBM-GBTx
Chipset ordered from CERN

GBTx
FPGA emulation for VECC and JINR

SPADIC for TRD
ZiTi Heidelberg, P. Fischer et al

SPADIC 2.0 with e-link interface

Rad tolerant LDOs
SCL Chandigarh, India

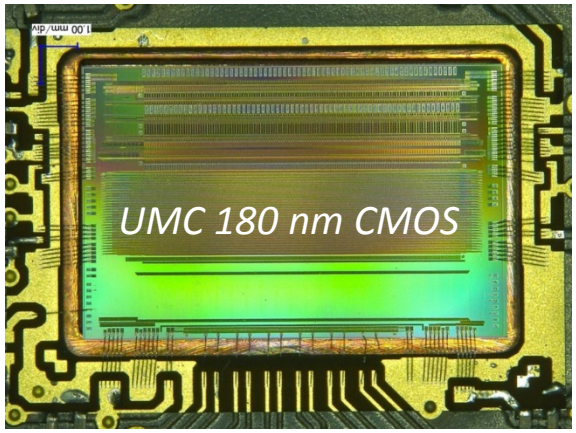
Fully digital Read-out ASIC “STS-XYTER”

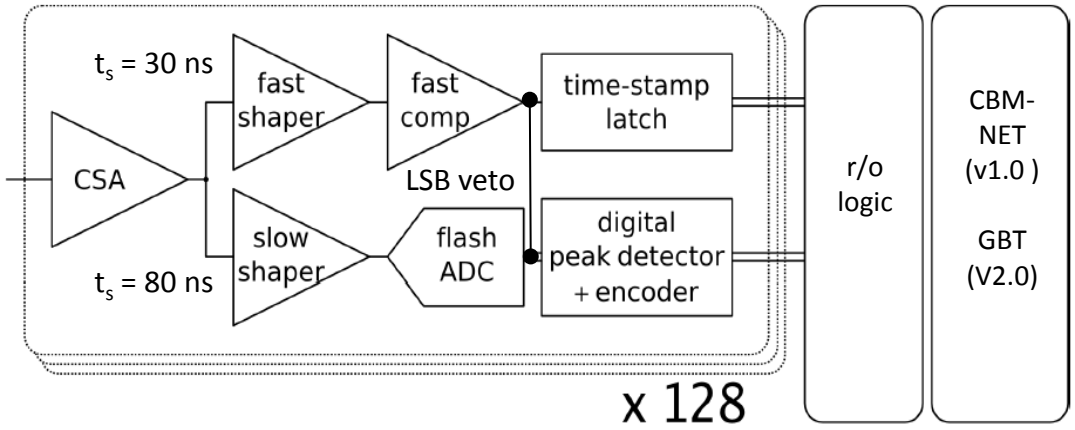
- *purely data driven read-out*
- *time-stamped data elements*
- *250kHz per channel*

for every channel:

- fast branch: time-stamp
- slow branch: signal height digitization (energy)

STS-XYTER ASIC





channels	128, polarity +/-
noise	< 1000 e^- under load
ADC range	16 fC, 5 bit
clock	160 MHz
power	< 10 mW/channel
timestamp	< 5 ns resolution
out interface	5 × 320 Mbit/s LVDS

noise minimization in self-triggering system:

effective two-level discrimination

- trigger to the timestamp latch vetoed if ADC-LSB generated no signal

Design Team:
R. Szczygiel et al. at AGH Krakow/Poland

AGH

STS-XYTER

R. Szczygiel et al. AGH Krakow

STS-XYTER turns into MuCH-XYTER via Gain Switch (x 0,2)

- Submission Review in Feb. 2015: Noise is an issue →

  system issue, optimization with complete system perspective,

  extensive architectural studies → goal < 1000 ENC

- Submission Review in Oct. 2015 → full go for submission

- STS-XYTER 2.0: adaptation to GBTx-eLink-readout, STS-r/o protocol

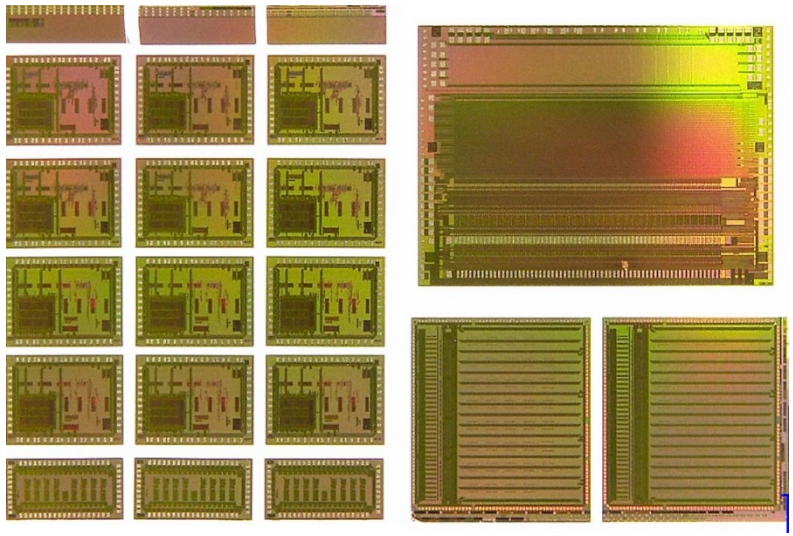
→ intensive collaboration AGH-WUT (W. Zabolotny (DPB)) on design and verification

  - STS-XYTER defines critical path for STS!
  - → This submission has all architectural elements included!

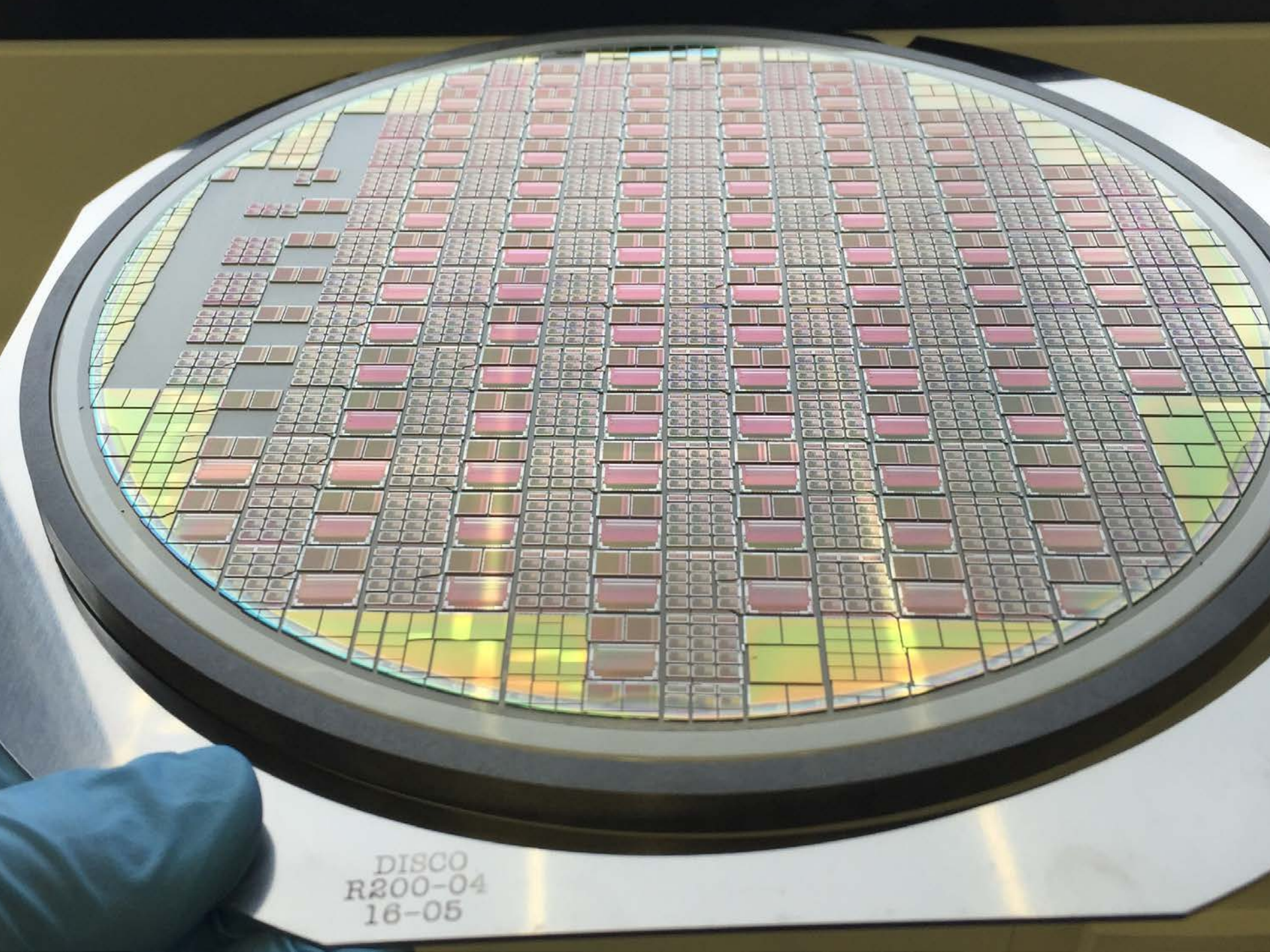
Long awaited STS-XYTER 2.0 Submission Mai 2016

...evolved to a grand CBM-Joined 6-Chip Submission

- STS-XYTER 2.0 → yield 930 chips for STS- and MUCH-prototyping
- TOF readout ASICs, Volume production for operation at STAR
  - Get4-TDC in two versions:
    - Bug-fix version
    - Version for robust operation at 40MHz
  - PADI – fast 8-channel TOF pre-amp



- SPADIC V2 → prototype run with CBM compatible e-link interface


DISCO
R200-04
16-05

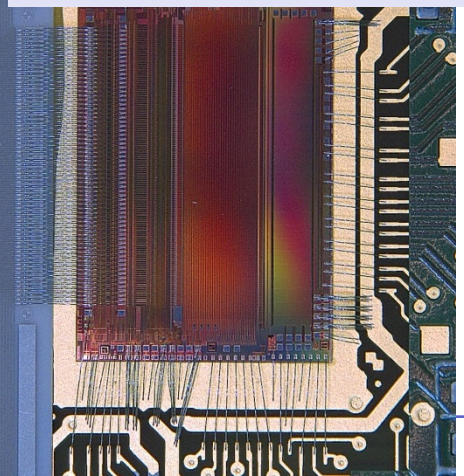
The Readout-ASIC STS-XYTER

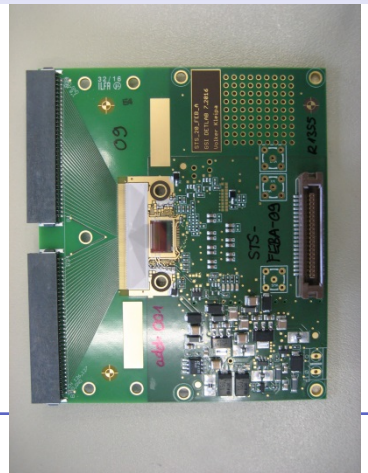
- The moment of truth:

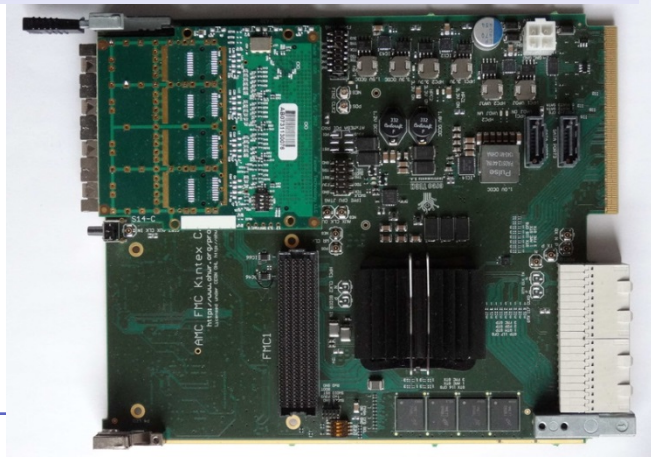
  Testing is a joined AGH, WUT, VECC and GSI effort

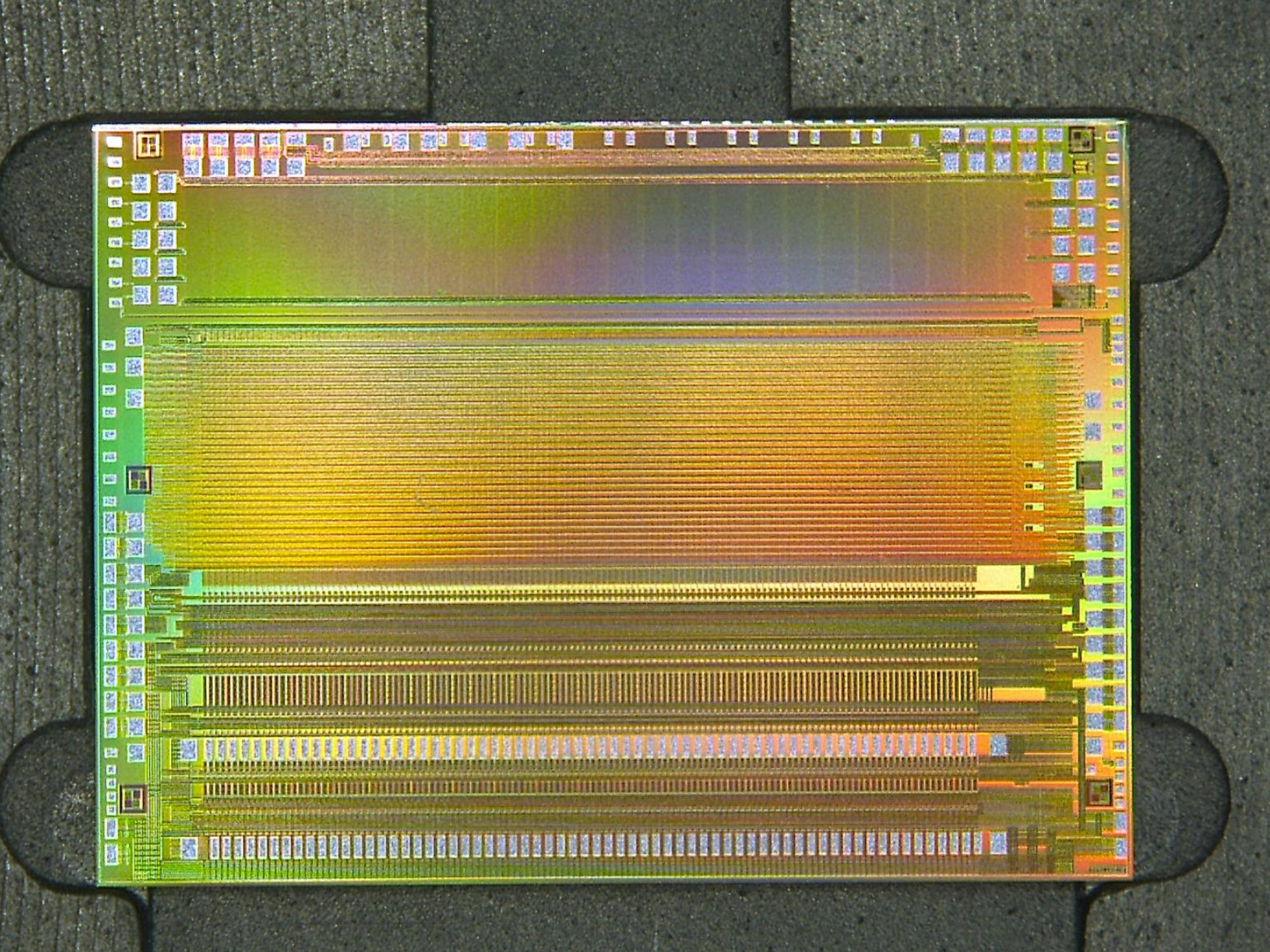
  → workshop on STS-XYTER testing Feb. 2017 in India

- Beam-time Feb. 2017 at Helmholtz FZ-J COSY: Rad. tests

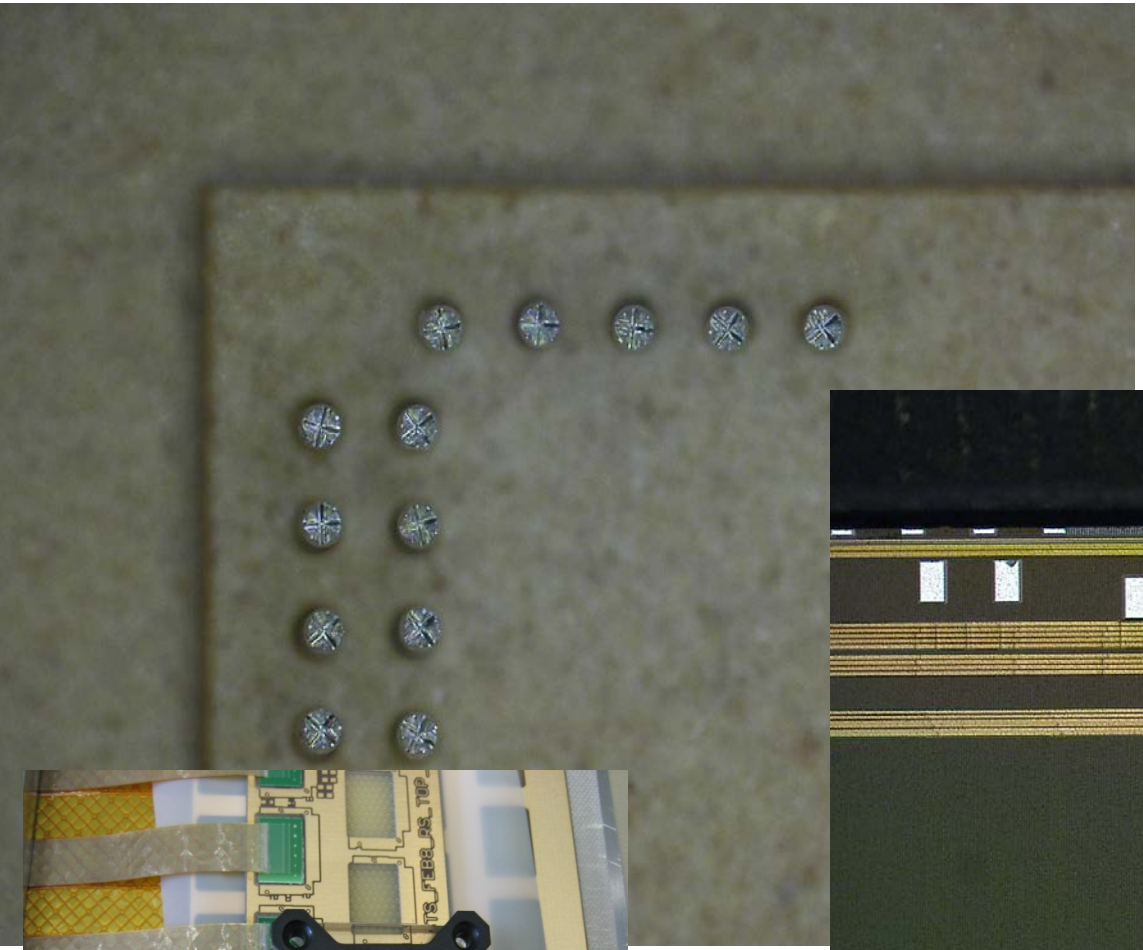


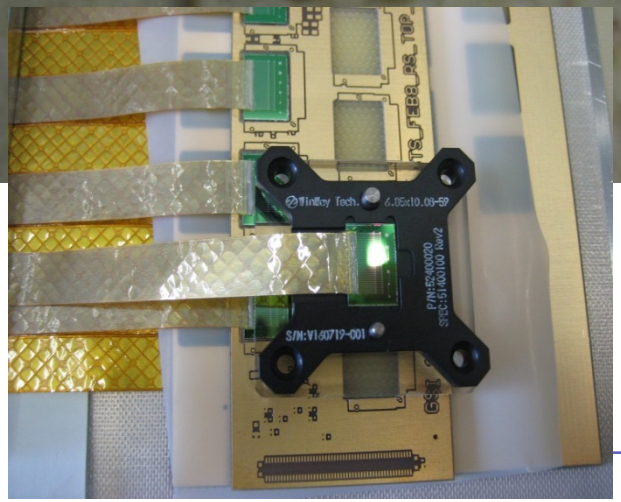


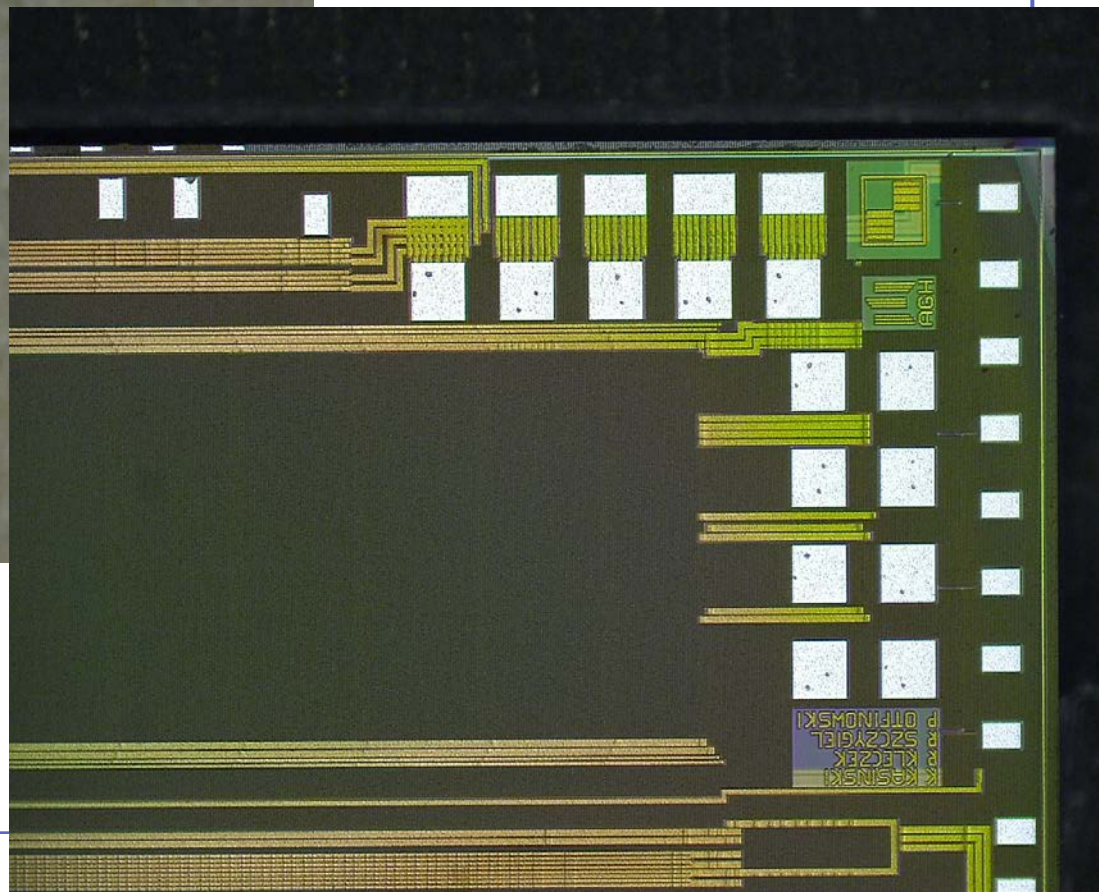


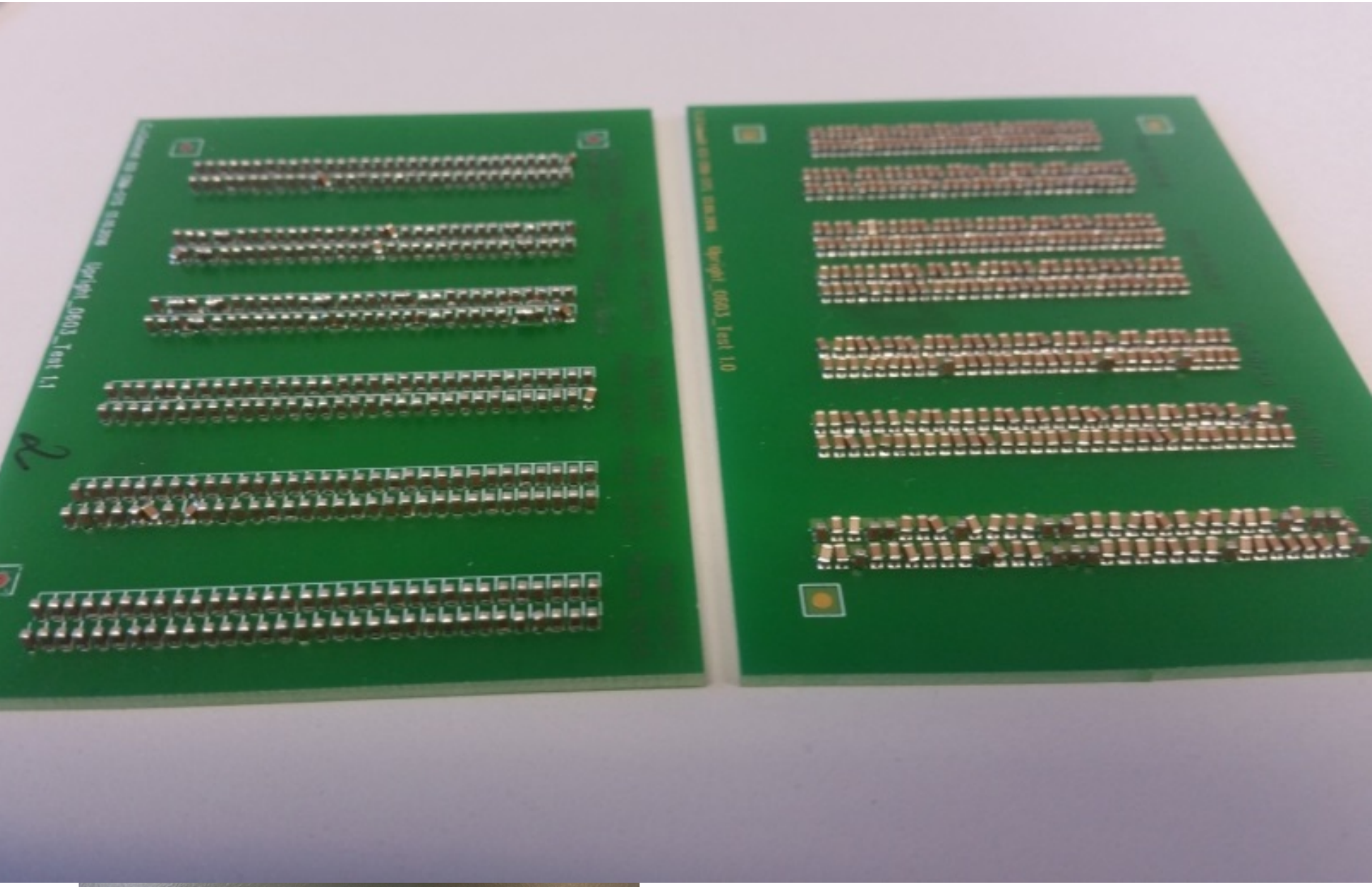


Dicing precision successful: 100µm Pogo-Pins match!



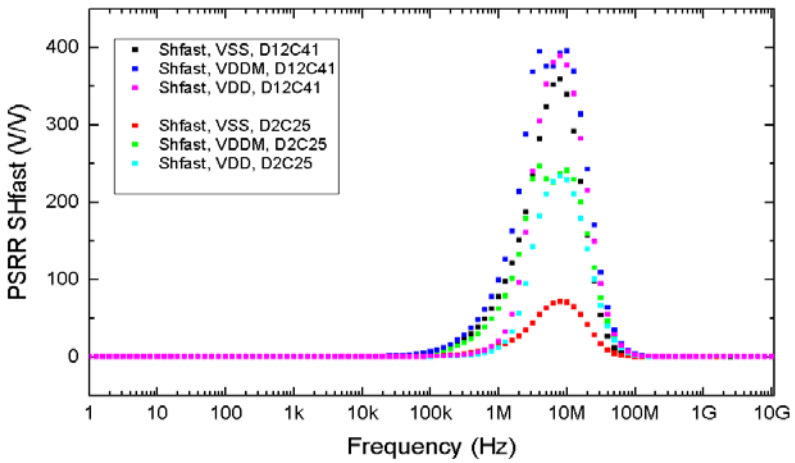




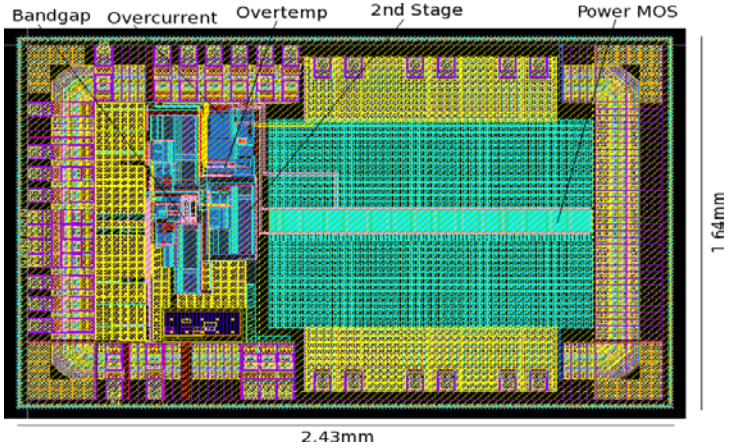


SCL realizes radiation tolerant LDOs for CBM

- Linear regulators for skimming at point of load
- Sensitivity to Total Ionizing Dose evaluated by VECC Kolkata → OK for CBM
- Sensitivity to Single Event Upset evaluated by GSI at COSY, FZJ → OK for CBM



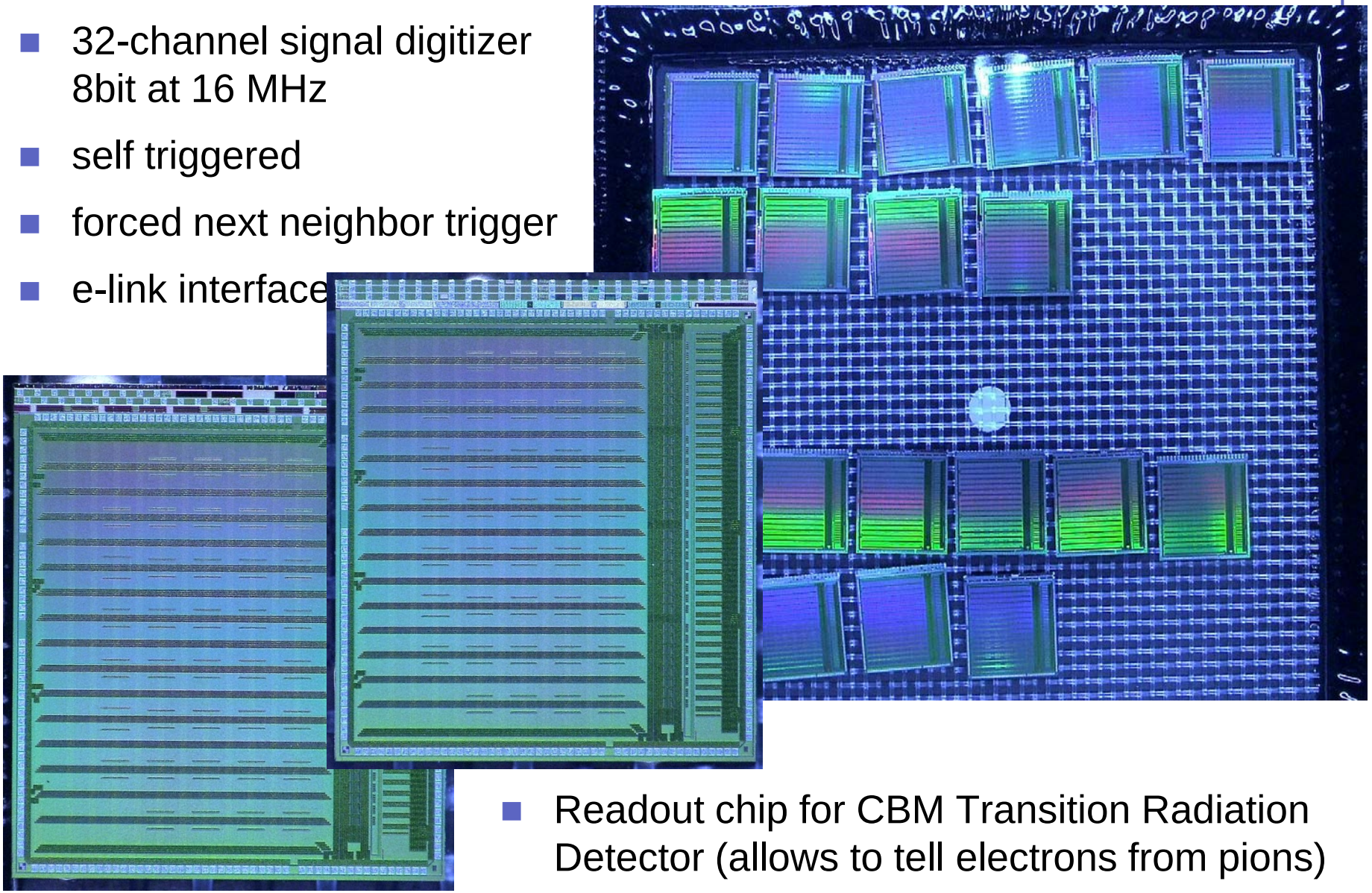
STS-XYTER single ended cascode very sensitive to supply noise



180nm Tower Jazz Process

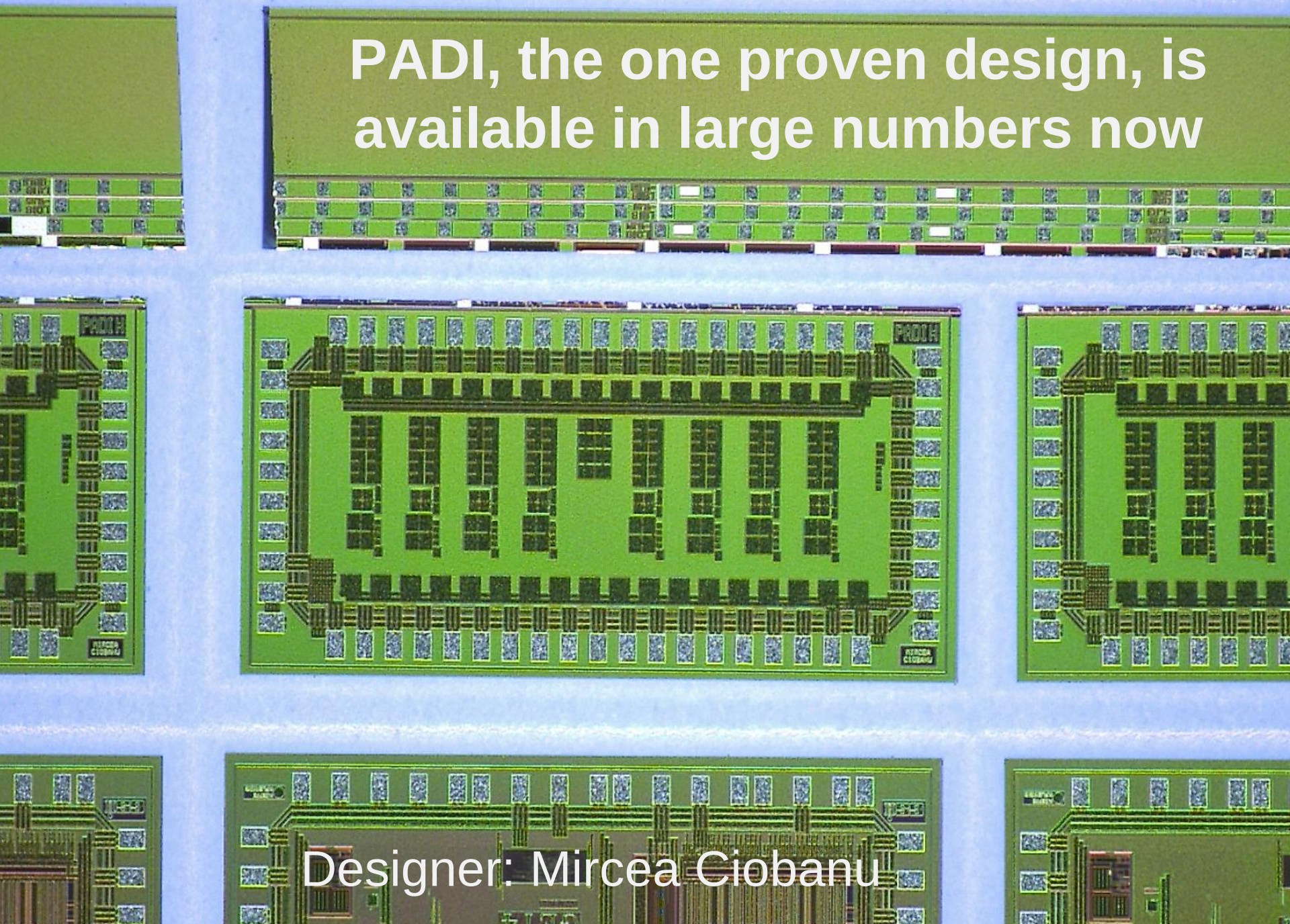
CBM-TRD: Spadic 2.0 in two versions being tested

- 32-channel signal digitizer
  8bit at 16 MHz
- self triggered
- forced next neighbor trigger
- e-link interface

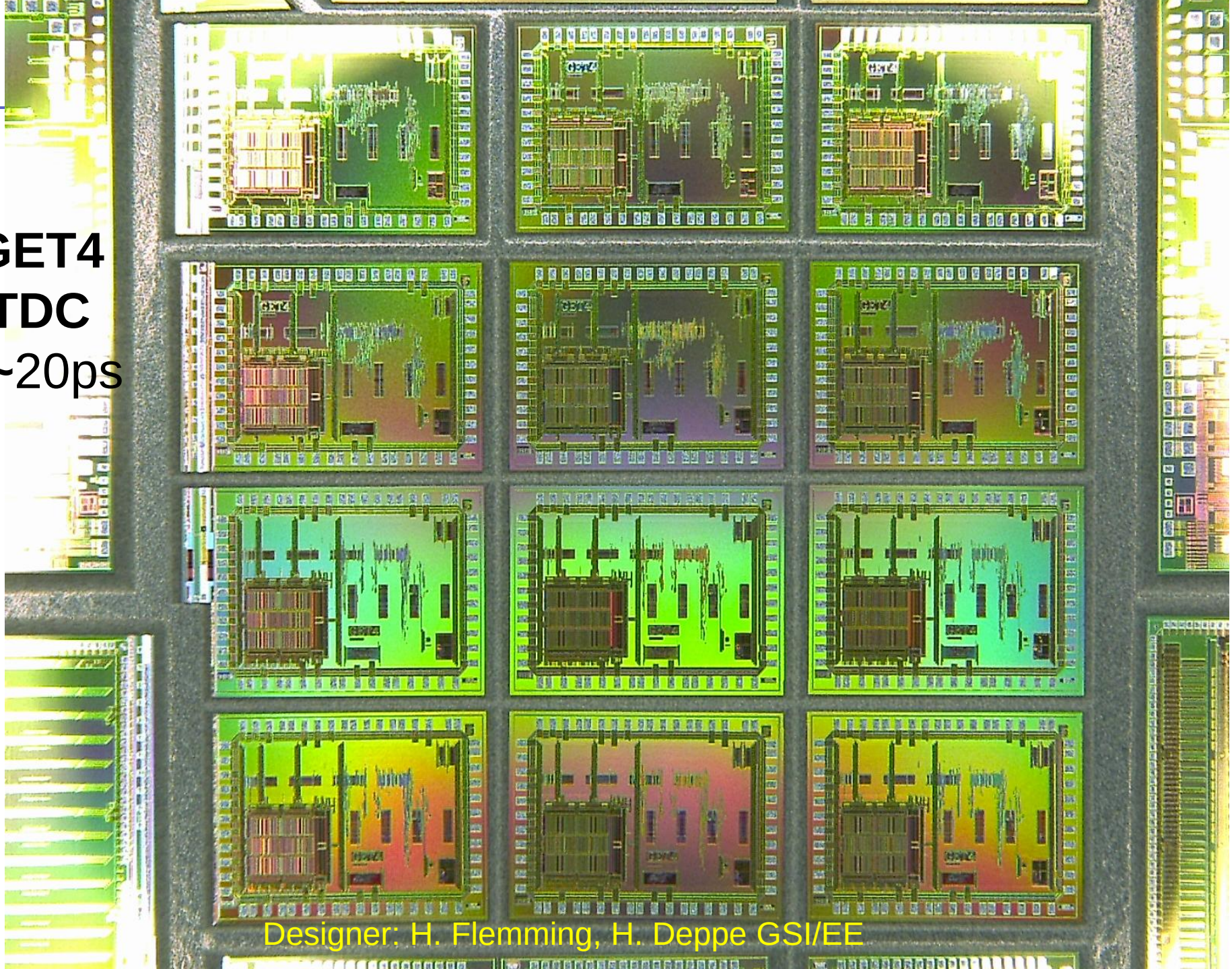


- Readout chip for CBM Transition Radiation Detector (allows to tell electrons from pions)

PADI, the one proven design, is available in large numbers now



Designer: Mircea Ciobanu


GET4
TDC
σ~20ps
Designer: H. Flemming, H. Deppe GSI/EE