XXXVIII-th IEEE-SPIE Joint Symposium Wilga 2016

Tests for the Readout Chain components of the CBM STS

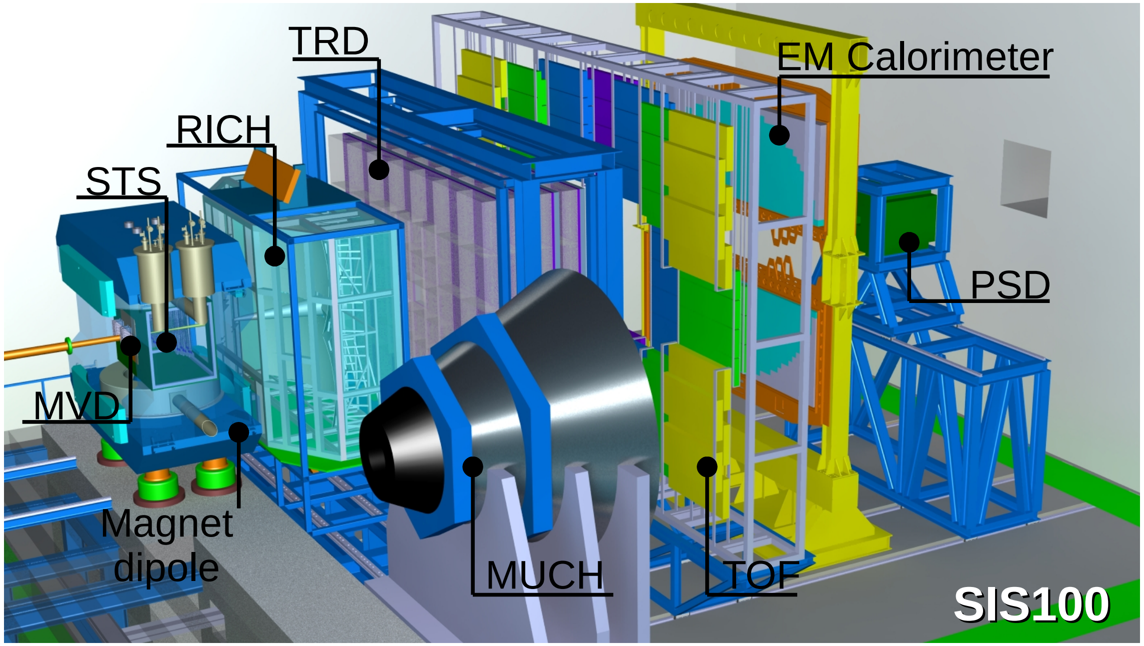
Adrian R. Rodriguez

for the CBM Collaboration

June-1st-2016

Introduction

The **C**ompressed **B**aryonic **M**atter (CBM) experiment at FAIR



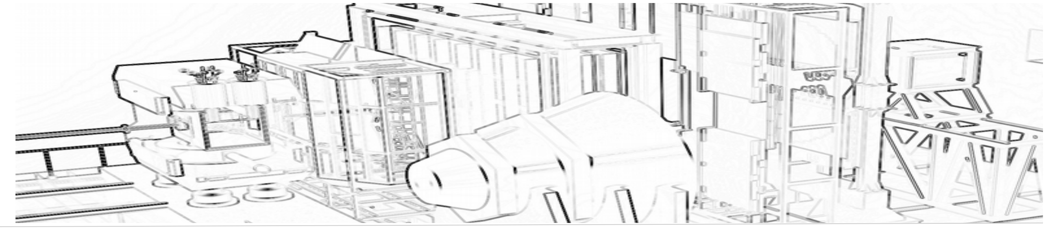
Goals:

- To explore the QCD phase diagram in the region of very high baryon densities.
- Search for the phase transition between hadronic and quark-gluon matter, the QCD critical endpoint.
- High precision measurement of rare probes.

Challenges:

- Very high collision rate (up to 10 MHz).
- Self-triggered read-out electronics.
- High-speed data processing and acquisition system.
- 4D event reconstruction and fast selection algorithms.
- High granularity and radiation tolerant detectors & frontend electronics.

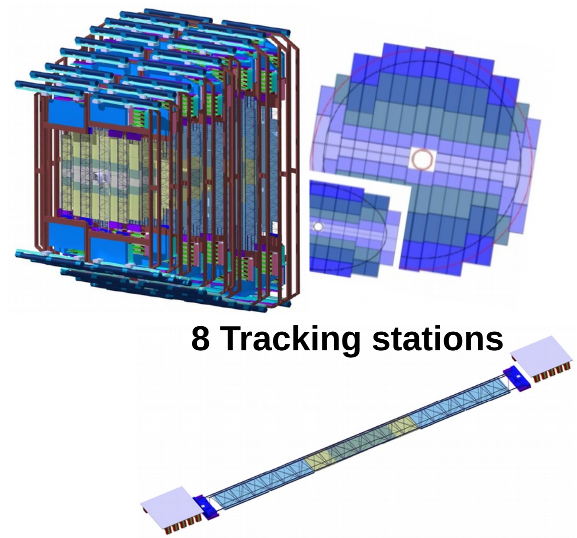
Introduction

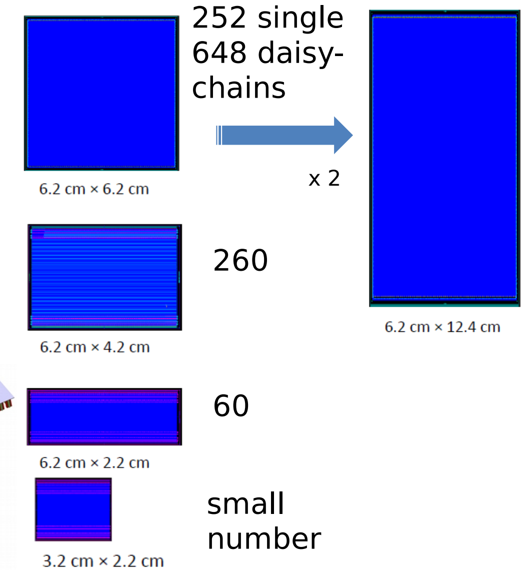


The Silicon Tracking System in numbers...

Essential component for tracking up to 1000 tracks/event at event rates up to 10 MHz in A+A collisions.

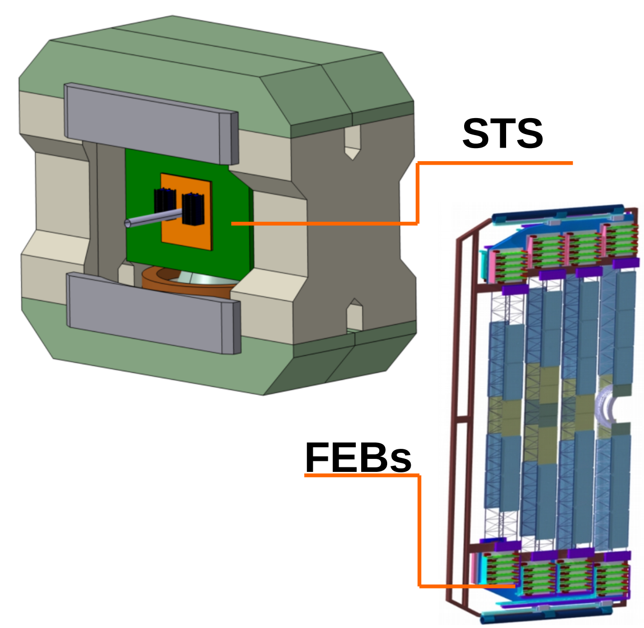
- ~1300 double sided Si strip sensors (2 x 1024 strips).
- δp / p ≈ 1%.
- 25 µm single hit spatial resolution.
- Material budget 1% X_o per station.
- 8 tracking stations.
- 1.8 million channels.





Challenges:

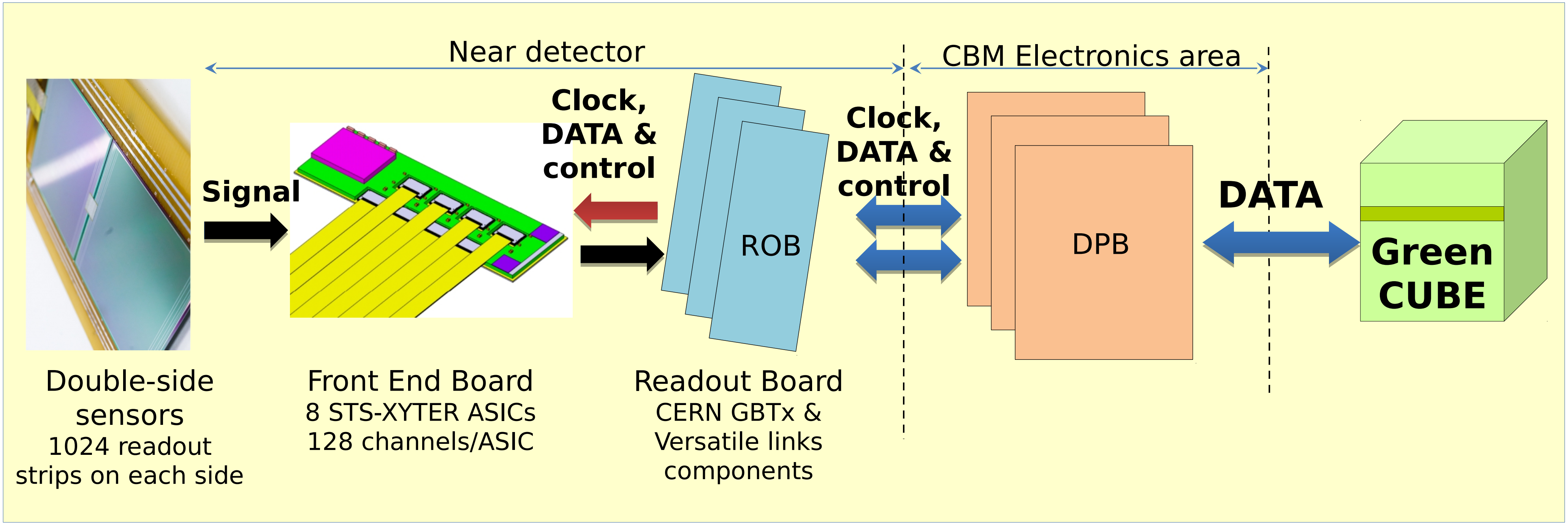
- STS is contained in a volume of approximately 1.4x2.3x1.3 m^3 inside the superconducting CBM magnetic dipole (B=1 T).
- Readout electronics mounted on top and bottom of the individual detectors ladders.
- Radiation flux at the electronics place up to 200 krad/yr.
- Signal rate (typical value 150 kHz/channel) will produce 200-300 GB/s.
- Cooling and heat dissipation (approximately 40 kW).



Outline

- The STS readout chain
- Test setup for the STS-XYTER v1 at GSI
- Noise measurements
- The C-ROB concept and brief description
- The Versatile Link Demonstrator Board (VLDB)
- Towards VLDB tests
- Status and Outlook

The STS readout chain



1. Frontend board (FEB)

8 ASICs (STS-XYTER).

Mounted close to the detector.

2. Readout board (ROB)

Data aggregation from several FEBs, clock distribution and synchronization.

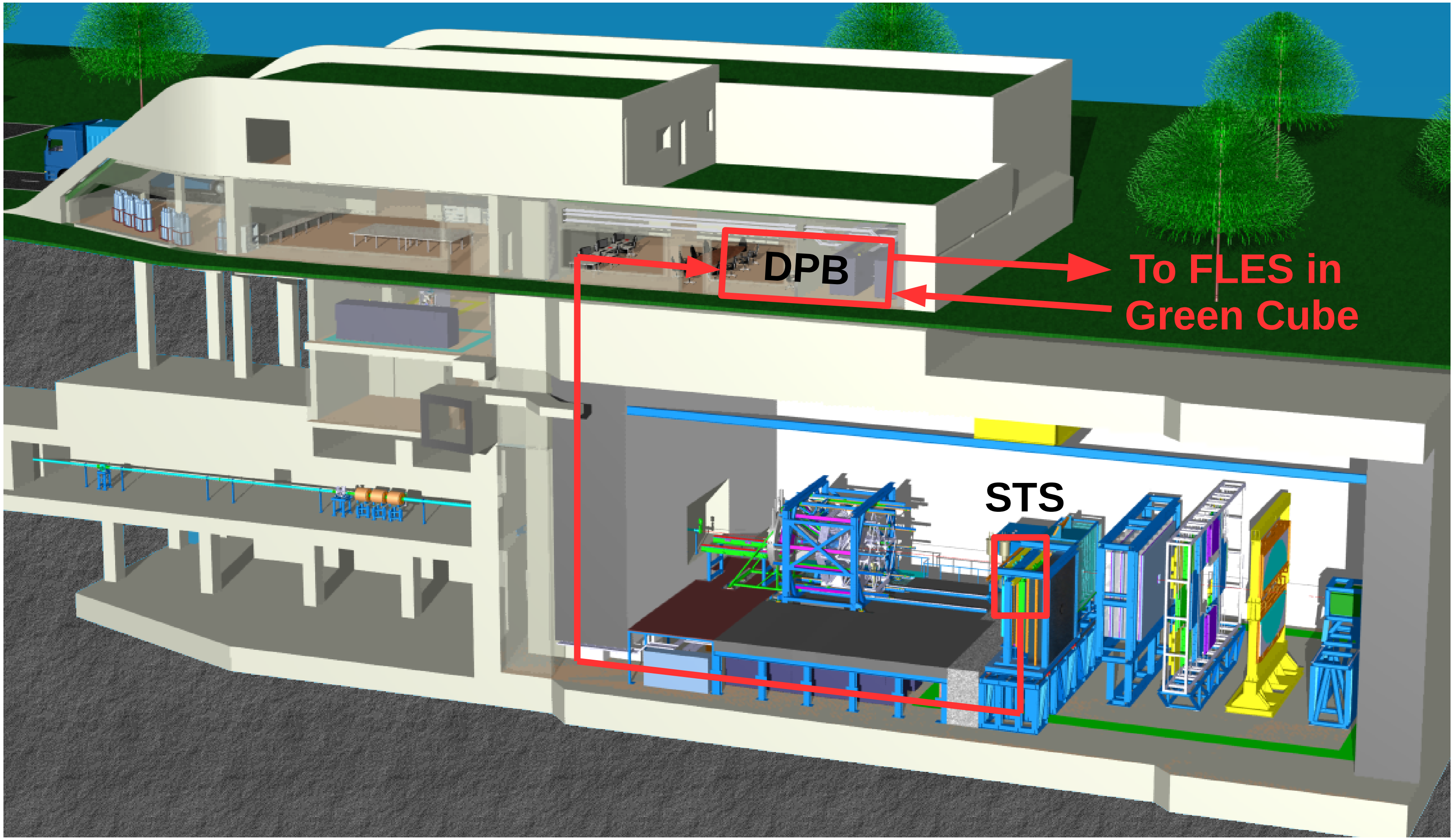
3. Data processing board (DPB)

Data preprocessing, interface to slow and fast control and timing distribution.

Limited space, Radiation Hardness

The STS readout chain

1752 FEBs 24000 electrical links ~30-80 cm	600 ROBs 2400 MM fibers ~50-80 m	78 DPBs up to 624 SM fibers several 100 m



Motivation

Motivation:

To establish a prototype readout chain and all the necessary components with sufficient performance (e.g. FE noise, readout bandwidth):

- Tests different sensors types with the STS-XYTER.
- To investigate sensor performance and FE noise.
- To compare realistic simulations with experimental measurements.
- To gain experience to establish a low-level noise setup at GSI lab.

To optimize the development of the C-ROB for every specific application:

- Board design.
- System integration and cooling.

The STS-XYTER

STS-XYTER ASIC v1

CRACOW
AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

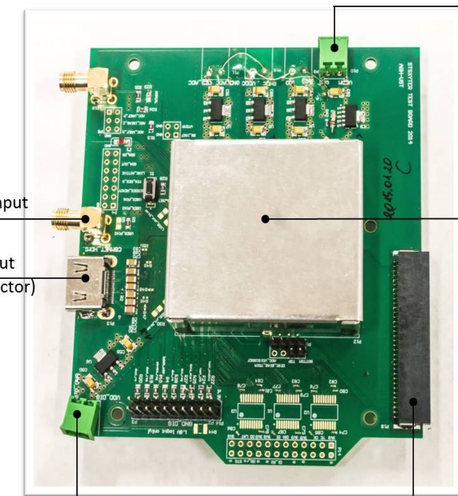
ASIC dedicated for signal detection from the double-sided Si sensors.

- Self-triggering chip with 128 channels.
- Provides digitized hits with:
  - 5 bit Energy Resolution.
  - 14 bit Time stamp.
- STS-XYTER v1 backend → CBMnet protocol

Main goal
Noise optimization!
<1000 e- rms in charge measurement in the final system

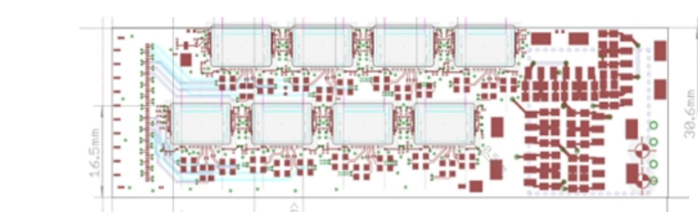
K. Kasiński, W. Zubrzycka.
Test systems of the STS/MUCH-XYTER2 ASIC - from wafer-level to in-system verification.
June 1st. 2016. Wednesday 09:00

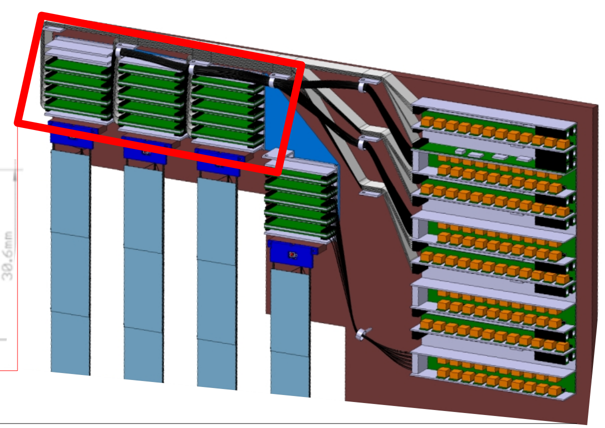
STS-XYTER v1 prototype board



FEB-8
- for reading 1 sensor side (1024 channels)
- Required for module assembly.
- highly integrated (space, cooling,...)

GSI



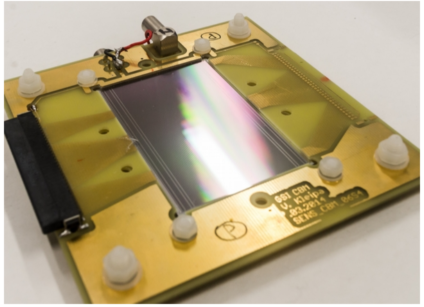


The STS-XYTER v1 test setup at GSI

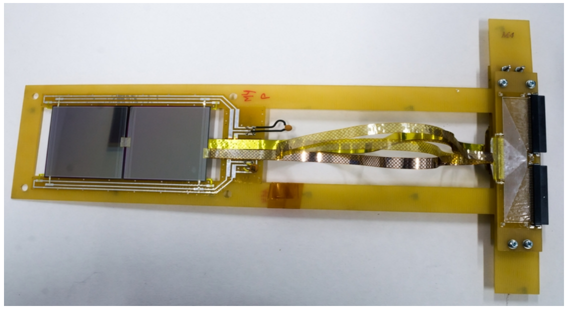
Features:

- 1 prototype FEB with 1 ASIC.
- Test pulses were generated by the internal pulser, triggered by an external pulse generator.
- 14 ASIC channels are bonded.

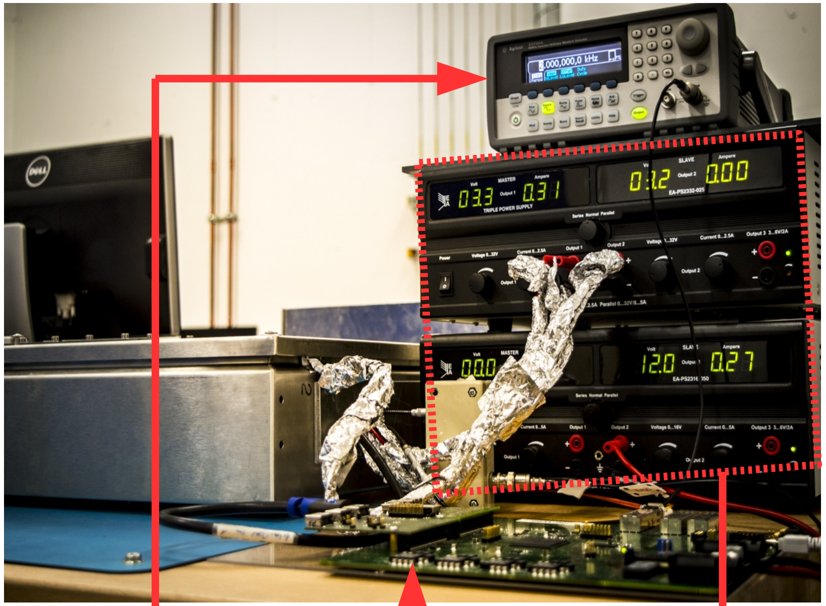
  … … … …
- 1 Syscore 3 ROC
- System configured with CBM-NET backend.



Medium size sensor (4.0 x 6.2 cm^2)



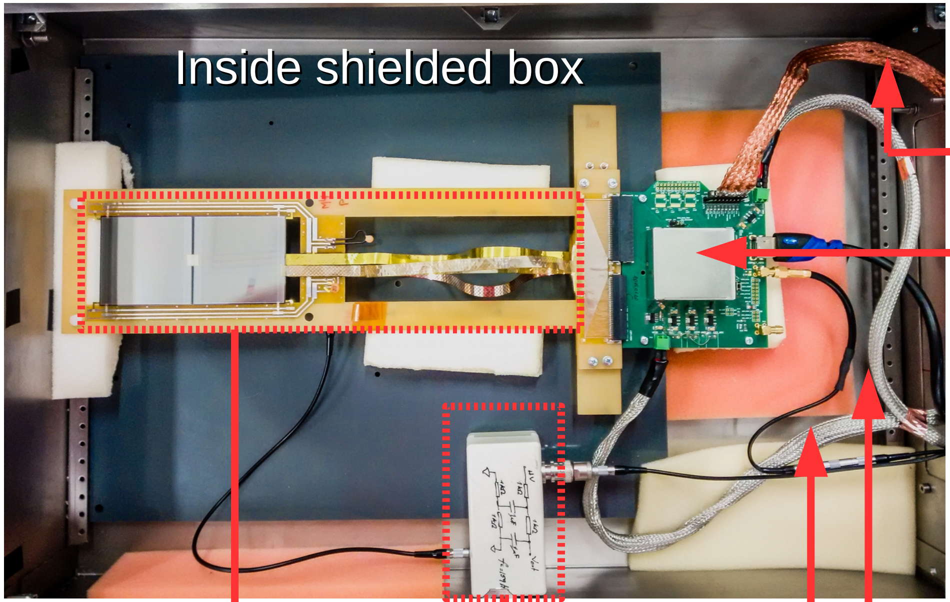
2 daisy chained sensors (6.2×6.2 cm^2) + 30 cm microcable readout



Pulse generator Agilent (40 MHz)

Syscore 3 ROC

LV Power Supplies



FEB grounded to shielded box

Prototype FEB

Shielded cables STSXYter LV

HV bias filter

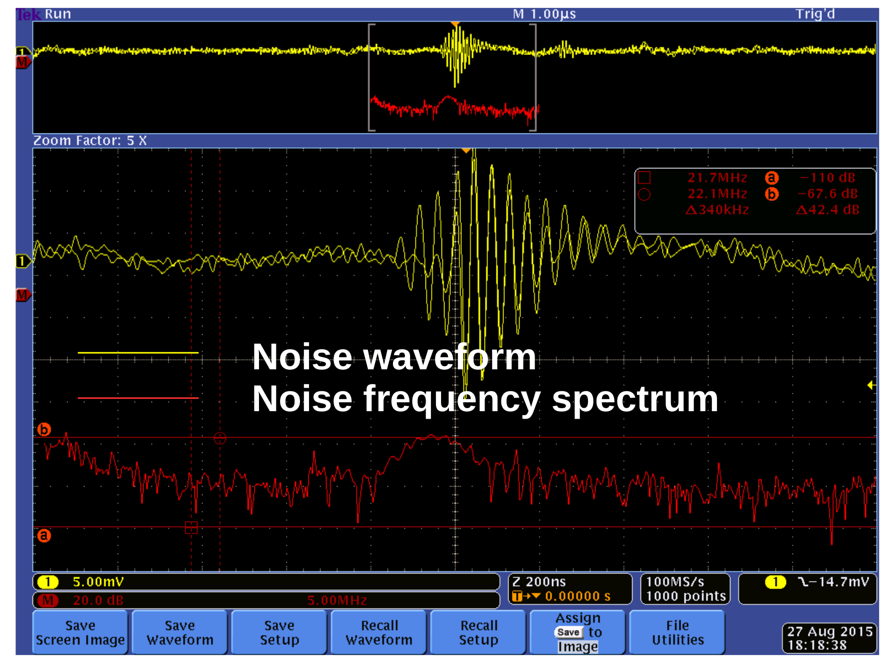
daisy-chained sensors & microcable

The STS-XYTER v1 noise level measurements

Evaluating noise levels

Main contribution to noise:

- Sensor bias.
- Sensor:
  - strip capacitance, inter-strip capacitance.
  - series resistance.
- Microcable.
- FEB low voltage cables.
- Common mode noise.



Keithley 2410 Power Supply connected to a Tektronik Oscilloscope via a 20 db attenuator.
Before filtering

Optimization:

- **Two stage RC and LC filters** with common mode noise suppression in the sensor bias.
- **LV cables shielding**.
- **Ground scheme** (FEB, shielding box, cables and LV supply connected to a common ground point).

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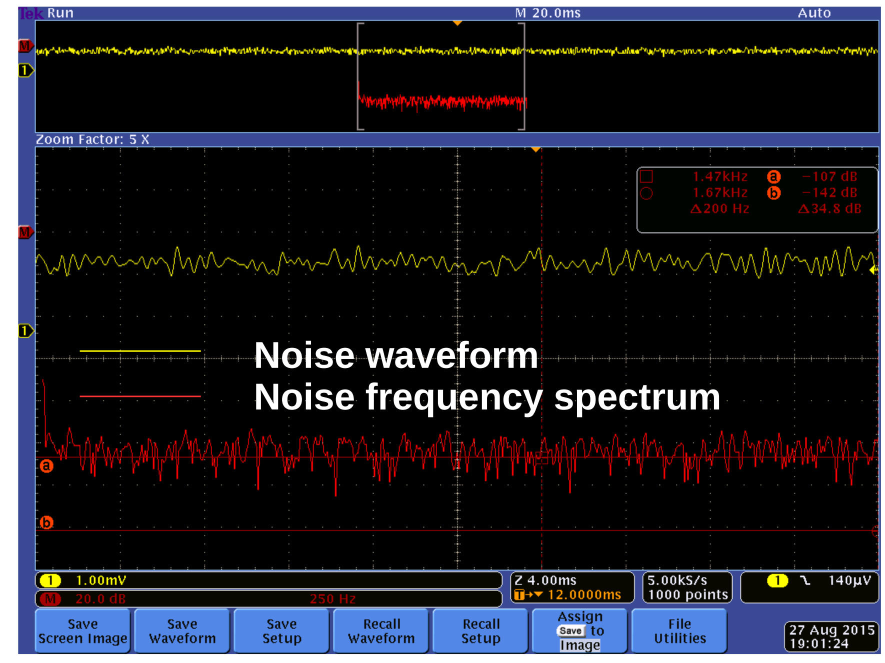

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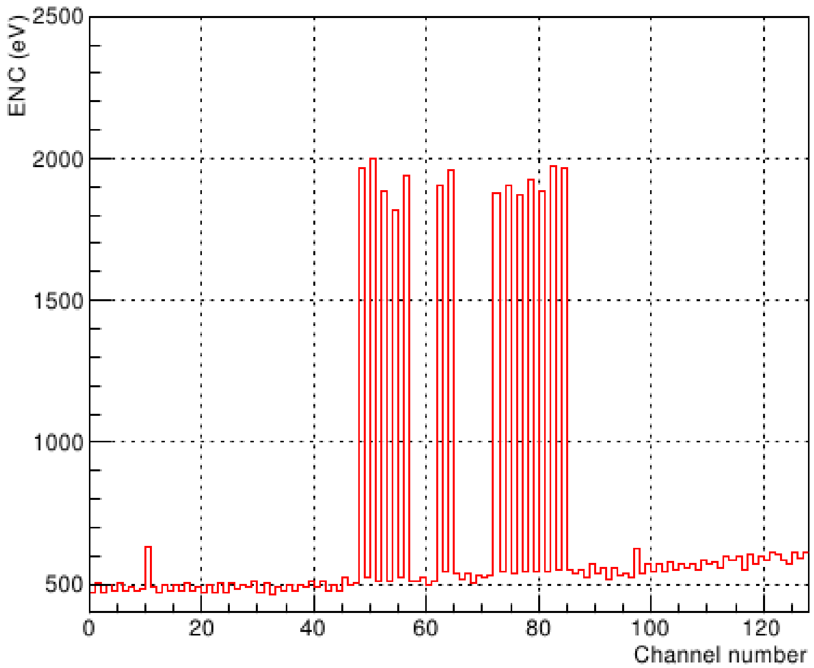
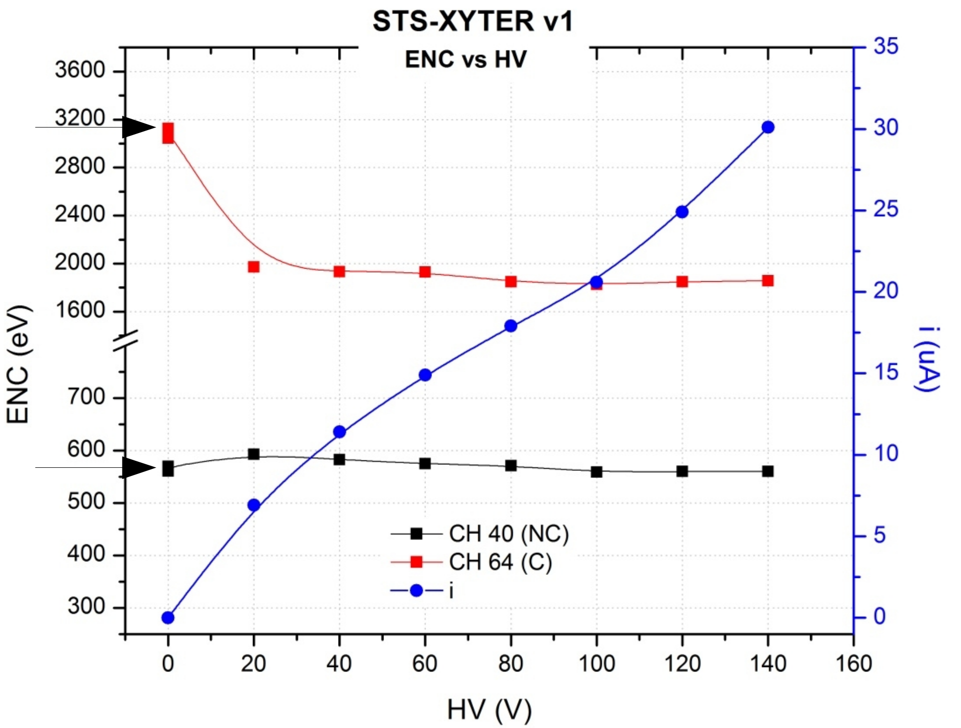


Equivalent noise charge in the 128 channels of the STS-XYTER v1. Average value over the 31 comparators.



Equivalent noise charge in connected and non-connected channels of the STS-XYTER v1 as a function of the sensor bias voltage. Lines are just to guide the eyes.

Realistic post-layout simulations estimated the noise level for connected channels around 1600 e-.
Measured average ENC values around 1900 e-.

The Readout Board (ROB)

from FEB

to FEB

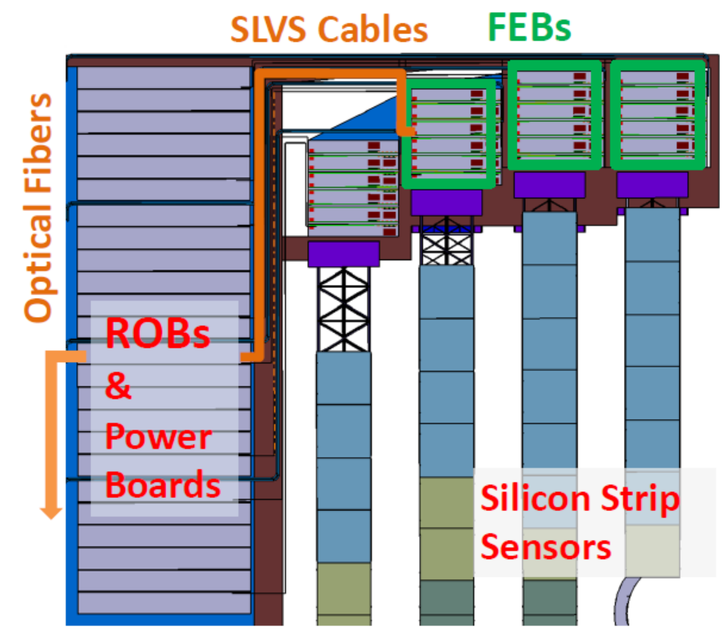
Intermediate functionality

- Data aggregation
  - ASICs (several thousands e- links)
- Data Readout
  - Optical transfer
- Data path
  - control, synchronization

Requiremments

- Located inside STS box.
  - Radiation hardness.
  - Limited space

CERN GBT based solution



¼ station (every 2nd ladder)

to DPB…

from DPB…

ROB concept:

- 3 GBTx with 40 SLVS frontend links.
- 1 VTRx and VTTx with 1 optical down and three uplink.
- 1 SCA for GBT control.
- Power dissipation ~7 W.
- Stacked mounted on cooling fins similar to FEBs.

The VLDB demonstrator

Versatile Link Demonstrator Board (VLDB)
CERN development:

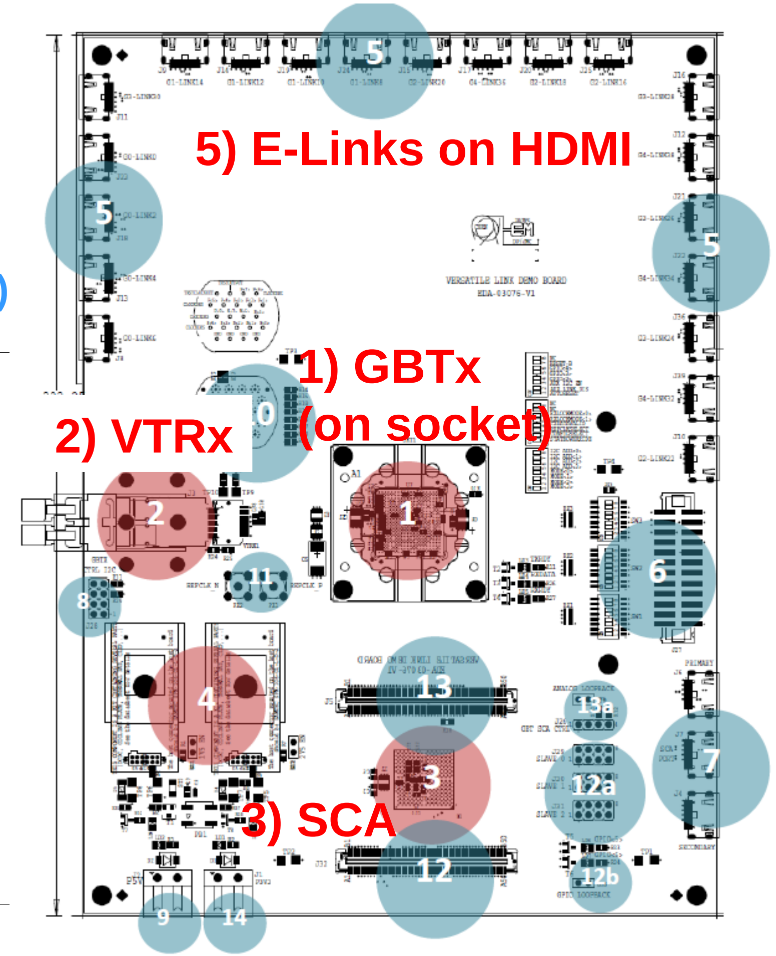
- 1 GBTx *data transceiver ASIC* **(1)**
- 1 VTRx *optical transceiver module* **(2)**
- 1 SCA *slow control ASIC* **(3)**
- FEASTMP *DC-DC converters* **(4)**
- FEE interfaces (20 E-Links) on HDMI connectors (160-320 Mbps) **(5)**

It will be possible:

- Test Readout chain and Front End systems connectivity to the GBTx using the e-links HDMI connectors:
  - DPB prototype (AFC-K)
  - Optical interface to VLDB/GBTx
  - Electrical interface (E-Links)
  - Frontend: "STS emulator" firmware (until STS-XYTER v2 available)
- Perform full system functional tests in radiation environment

First experiences with devices

- Device configuration and operation.
- Performance studies.
- Backend firmware and software development.



The Common CBM ROB prototype

for prototyping of all GBT based readout chains in CBM
Full GBTx, SCA and Versatile Link **functionality** required for readout and control.

STS: final ROB with different form factor, connectors, cooling features

From VLDB to C-ROB:

- **3 GBTx ASICs**

- connect up to 40 STS-XYTER devices at 320 Mbps.

- 1 Optical Transceiver (**VTRx**)
- 1 Twin Transmitter (**VTTx**)

- 3 optical uplinks : 13.44 Gbps total readout bandwidth
- 1 optical downlink at 3.2 Gbps for control

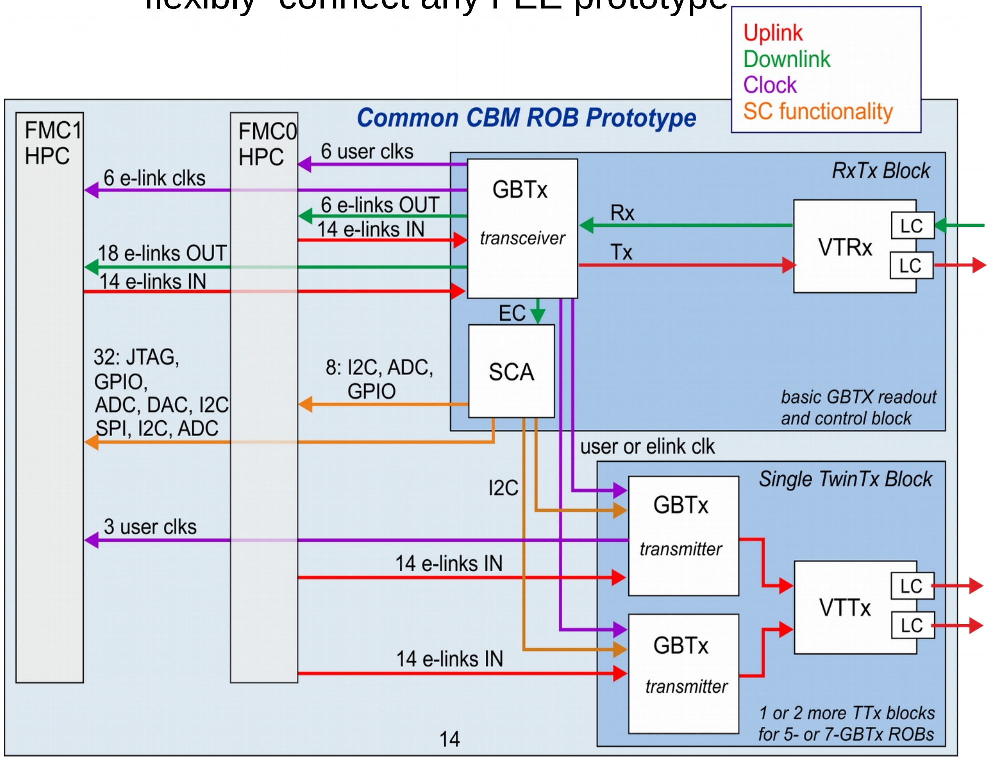
- **1 GBT SCA**

- I2C interface for control of slave GBTx
- additional multi purpose SCA functionality

C-ROB applications:
- STS
Connect up to 40 STS-XYTER (40 x 320 Mbps uplink)
- MUCH
connect up to 9 FEB (36 x 320 Mbps uplink).
- TOF
Connect to 24 GET4 (24 x 80 Mbps uplink)
(It will use only the Master GBTx)

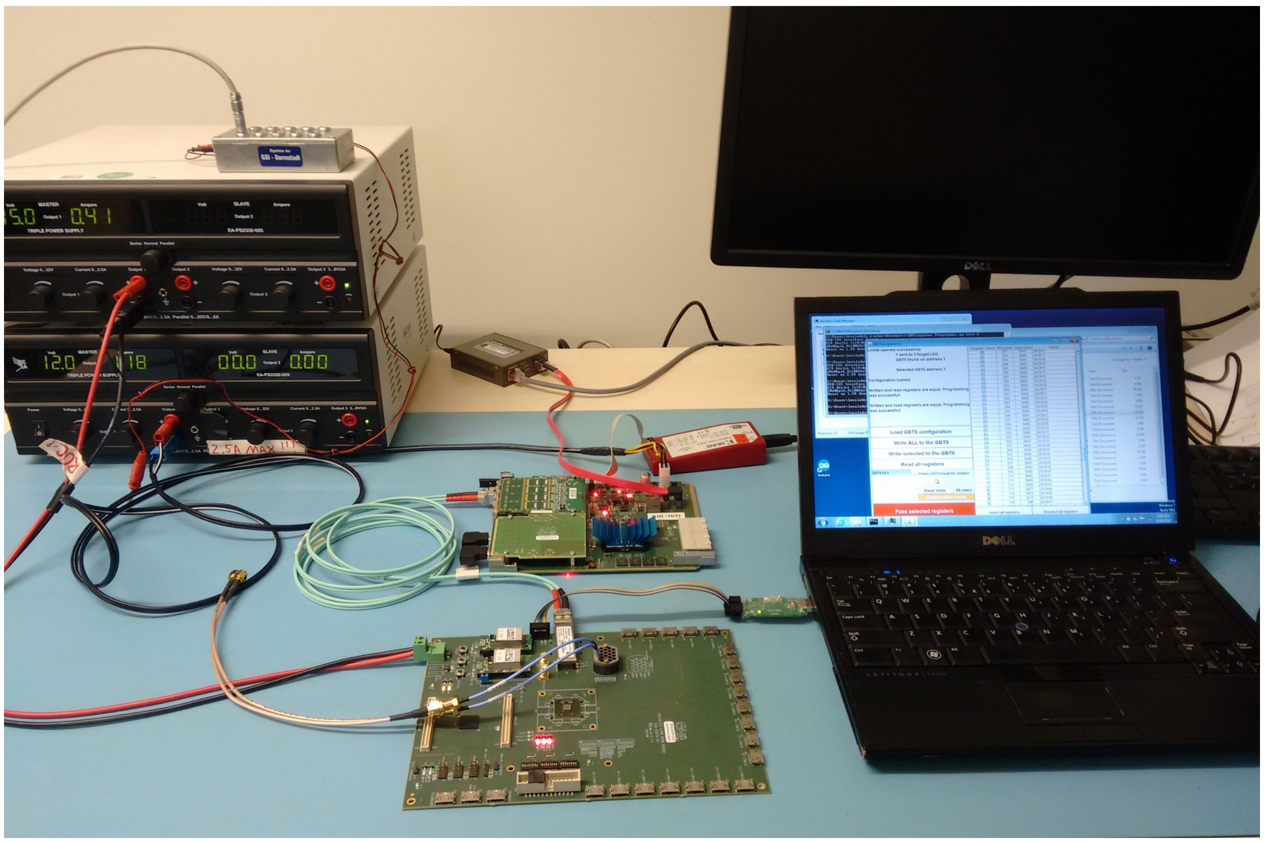
FMC connector with all **frontend connectivity**

- GBTx E-Links
- required and useful SCA functionality
- flexibly connect any FEE prototype



Joerg Lehnert. CBM Electronics meeting

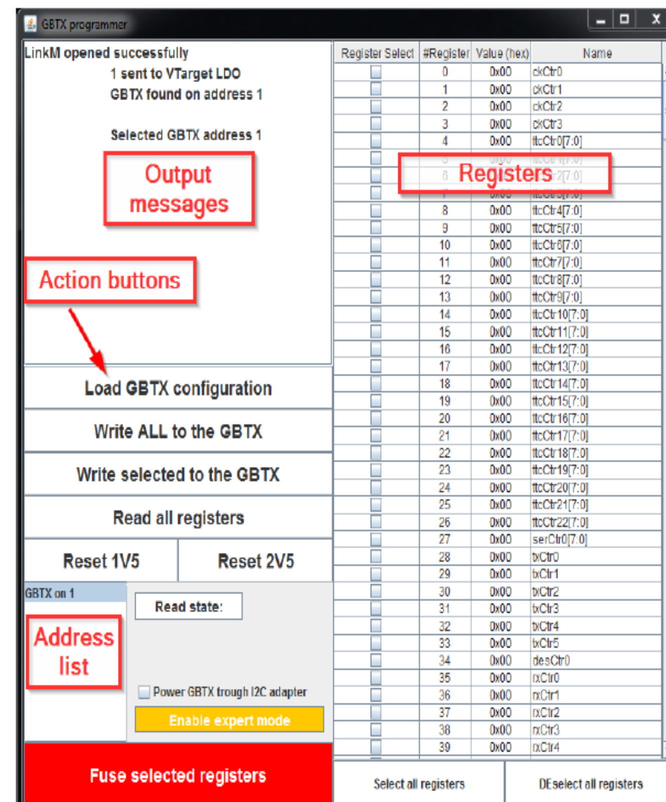
Towards VLDB tests (experimental setup)



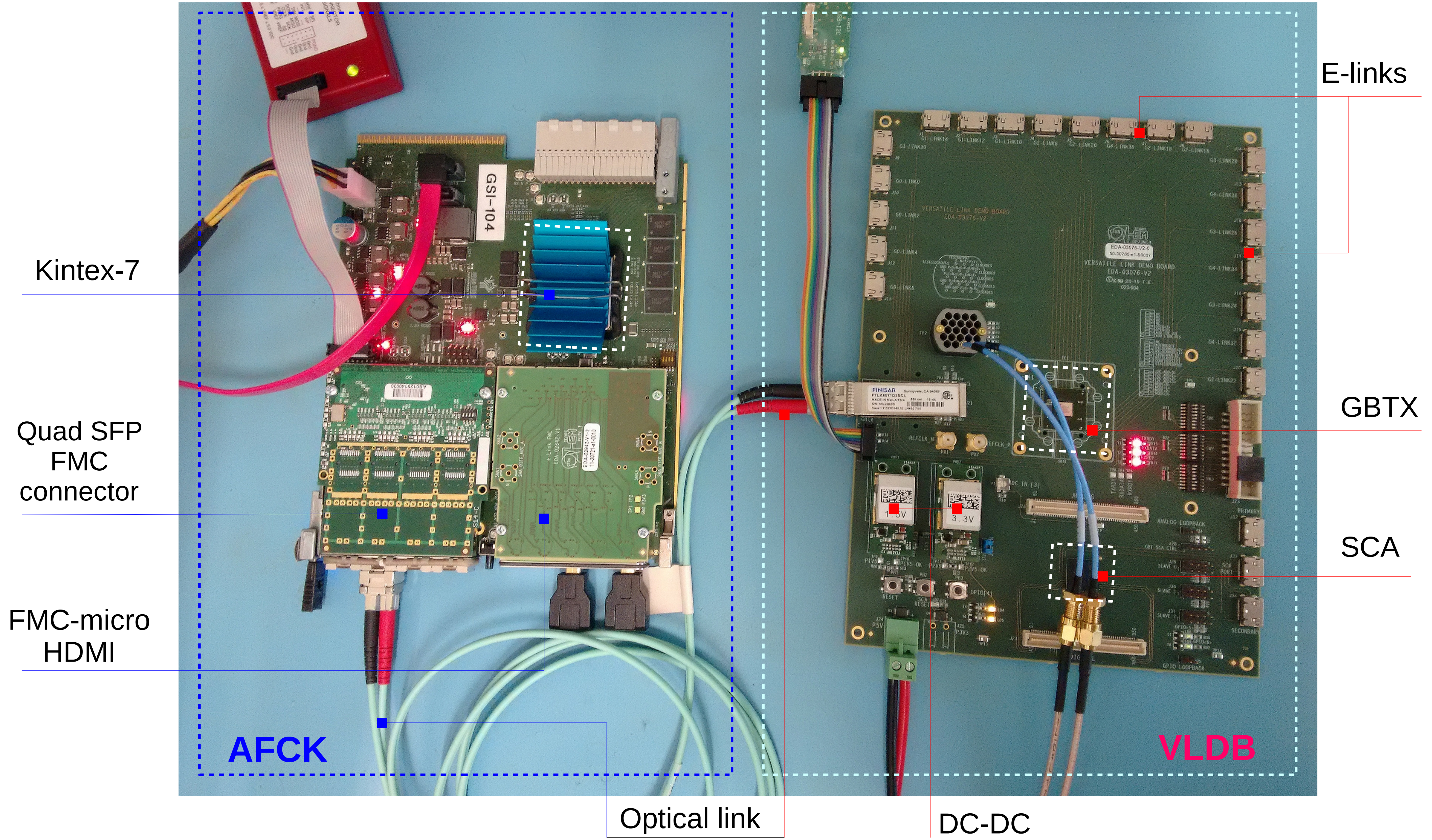
Optical data path for the VLDB-AFCK test setup

VLDB configuration and control via I2C using the GBT Java programmer

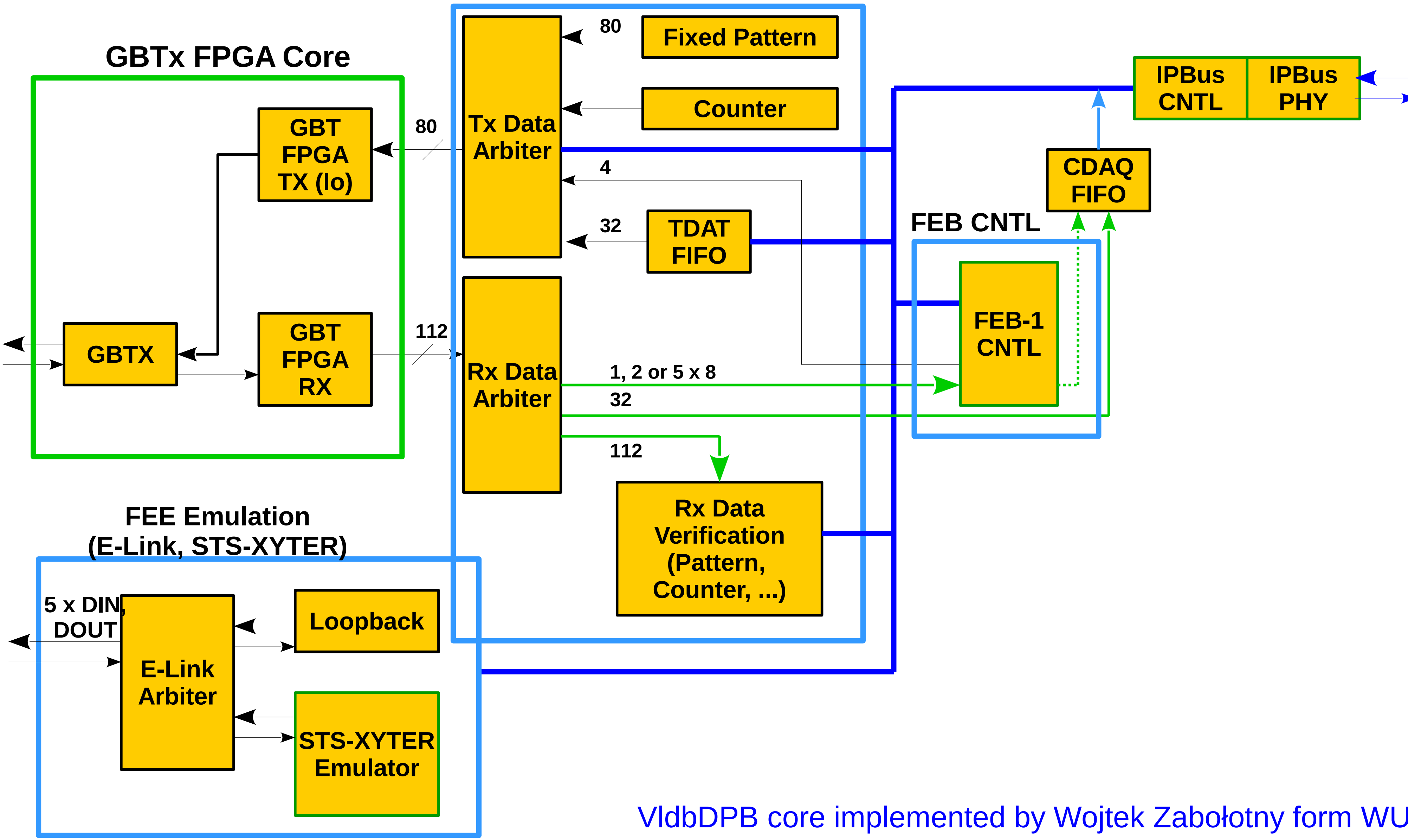
https://www.cern.ch/gbtx-configuration



Towards VLDB tests (experimental setup)



DPB functionality for VLDB testing



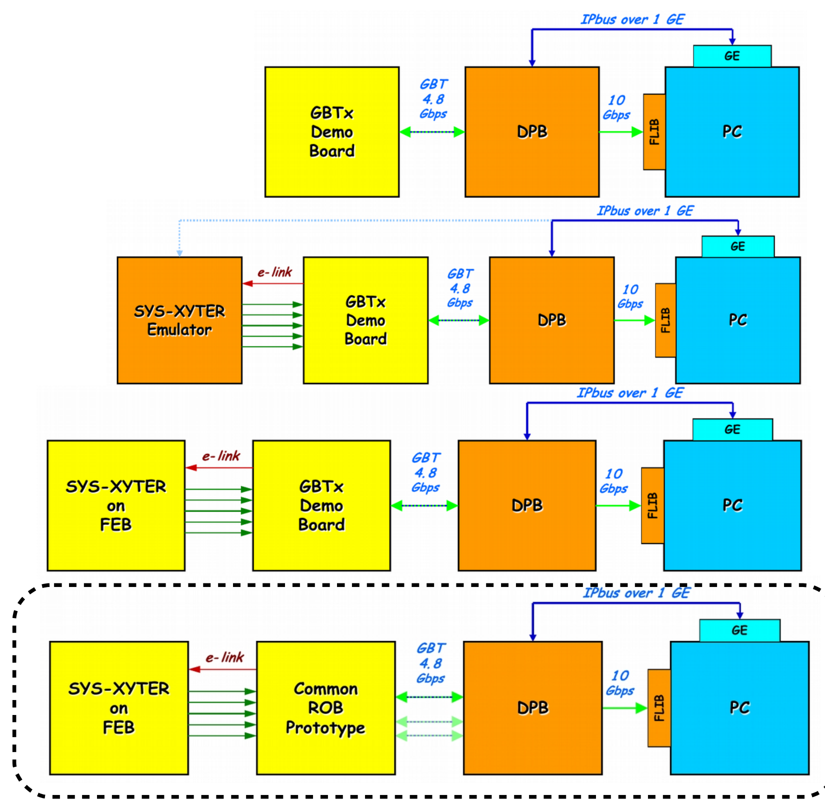
VldbDPB core implemented by Wojtek Zabołotny form WUT.

Status & Outlook

Modular DPB-AFCK firmware:
- common functionality and system for evaluating different tasks and specific blocks
- for ongoing test & development activities and towards full DAQ chain:
  - STS-XYTER FEBs or emulator.
  - VLDB (with HDMI FEBs) or C-ROB (with proper FMC for several FEBs)
  - Specific FEB through the proper FMC connector (n-XYTER based readout chain).

VLDB: → Operational
- Configured by Java programmer.
- Established optical link with AFCK

Optical data path → Operational
- Tested downlink with fixed pattern and counters.
- Tested data roundtrip with GBTx loopbacks.
- IPBus control and tests.
- Software test: python/Root-C++.
  - Reading and writing registers.
  - Define the transmitted pattern.
  - LED write test.
  - Data Tx and Rx reset.



Walter F.J. Muller. CBM DAQ Coordination

Status and Outlook

Next steps:

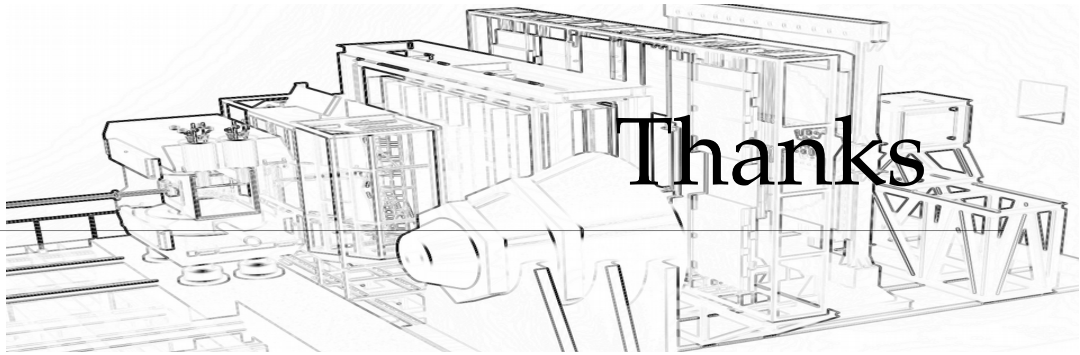
Test readout chains:

- VLDB E-links interface (E-Link data path).
- STS-XYTER FEBs or Emulator (Full data and control path over STS protocol)

Outlook to Fall 2016:

- FEBs with STS-XYTER v2.
- C-ROB.

this is a common effort shared by many...



Backup

C-ROB

TOF

- Connect 1 C-ROB to 24 GET4
- 24 E-Links up (80 Mbps)
- 24 E-Links down (80 Mbps; effectively 20 Mbps)
- No E-link (or phase adjustable) clock
- C-ROB with master GBTx only
- Two FMC (HPC) connectors (70% utilization)

MUCH

- Connect 1 C-ROB to 9 MUCH FEB
- 36 E-Links up (@ 320 Mbps)
- 9 x 160 Mbps E-Links down
- 9 x 160 MHz phase adjustable clock