# „ Test systems of the STS/MUCH-XYTER2 ASIC - from wafer-level to in-system verification”

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Department of Measurement and Electronics
Microelectronics Team

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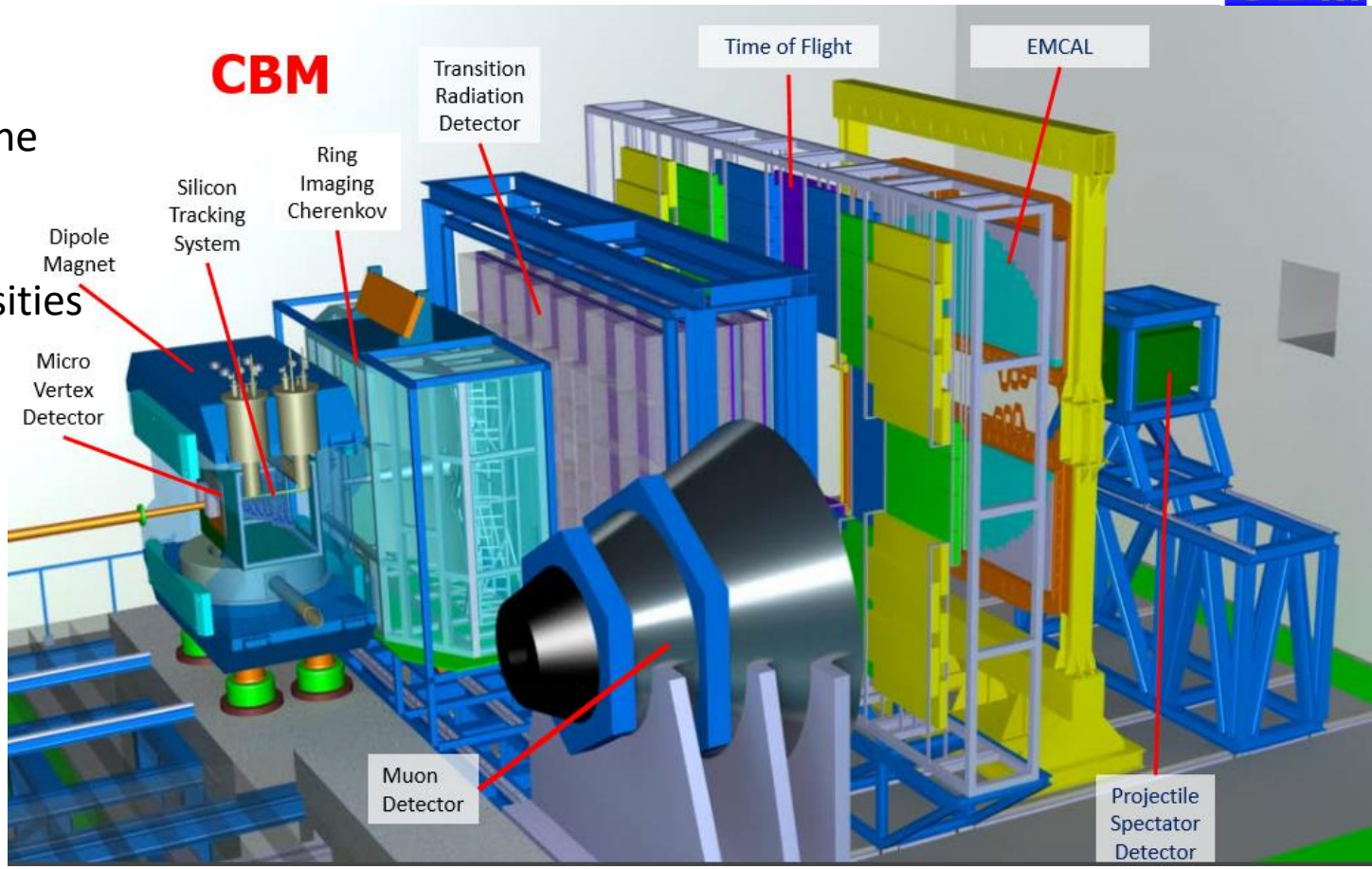
# Agenda

1. Introduction to CBM experiment, STS detector architecture, DAQ structure
2. STS module construction (detector + microcable + ASIC + FEB board)
3. Motivation
4. STS-XYTER2 ASIC & project roadmap
5. Proposed test procedures & methodologies
6. Proposed test systems for each stage
7. Summary & further steps

# CBM Experiment - outline

**Goal:** exploration of the QCD phase diagram in the region of very high baryon densities




- up to 10 MHz interactions
- **self-triggering** front-end chip
- radiation doses

**STS: track reconstruction and momentum determination of charged particles in 1T dipole field, 8 detector stations (30cm – 100 cm from target)**

# STS Detector

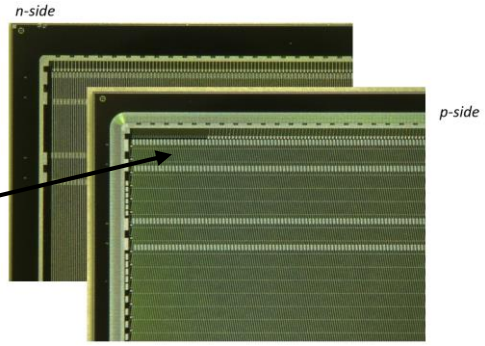
- **Silicon Tracking System (STS)**

– **double–sided, micro-strip sensors**, 1024 channels per side, 7.5°stereo angle, **strip pitch of 58 $\mu$m**, sensor lengths 20 - 60 mm, 300 $\mu$m silicon thickness,

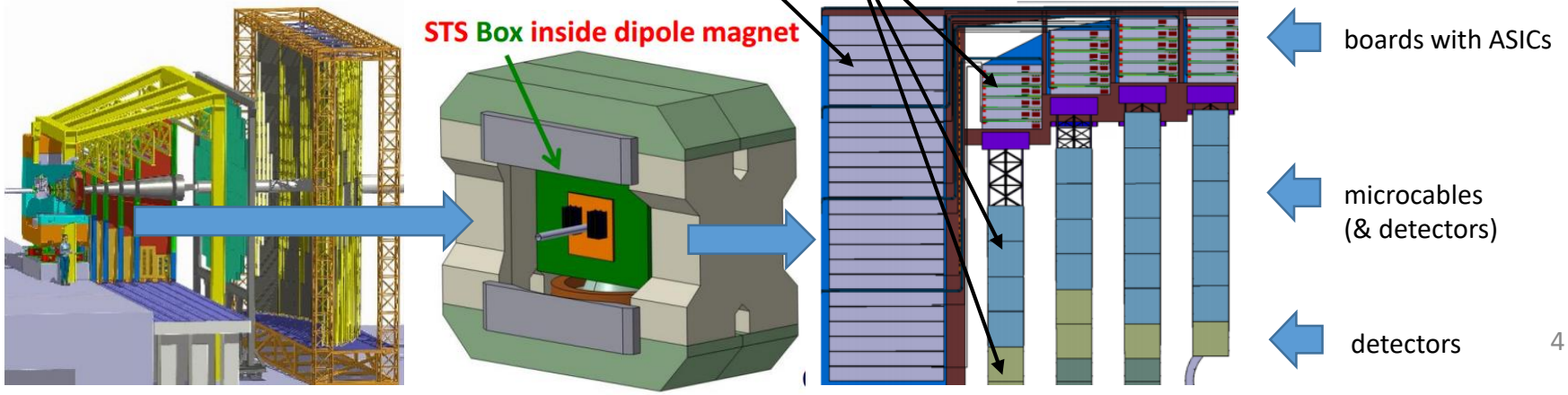
– sensors read out through multi-line micro-cables (sandwiched polyimide-Aluminum layers of several 10 $\mu$m thickness).

– readout electronics (STS-XYTER2 chips) located at the perimeter of the detector stations on FEB boards (8 chips/board).

– Data concentrators (GBTx-based ROB boards) also located nearby

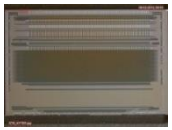
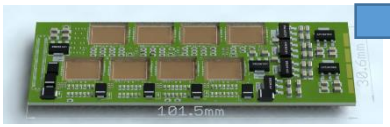


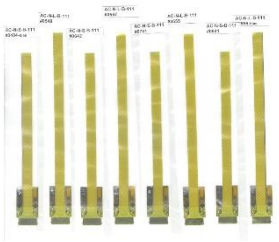




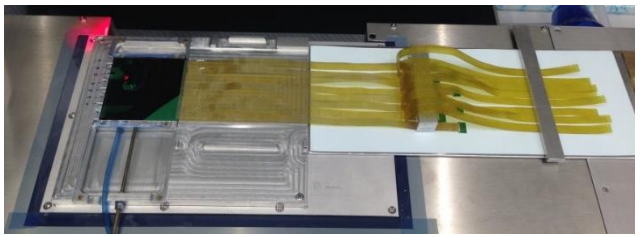
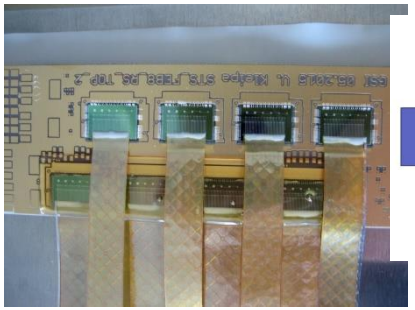
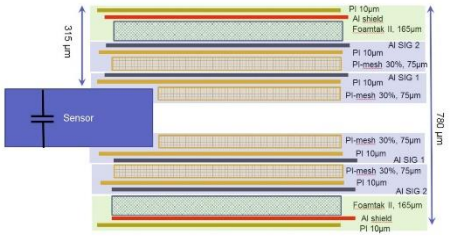
# STS modules assembly

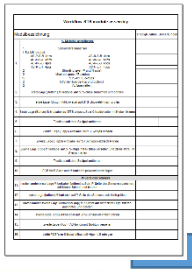
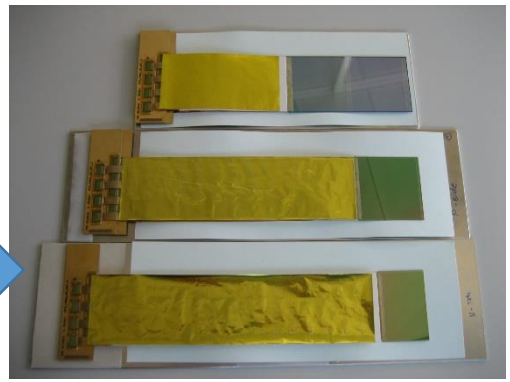
C. Simons, D. Soyk, R. Visinka, O. Vasylyev/ GSI Detector Laboratory & I. Tymchuk and team/ LED Technologies of Ukraine : Status of STS-module assembly at GSI, 27th CBM week 2016

Ingredients for single module:
1 Detector (1024 strips/side)
16 STS-XYTER2 chips
32 microcables
2 Front-end boards
2 shielding layers and spacers

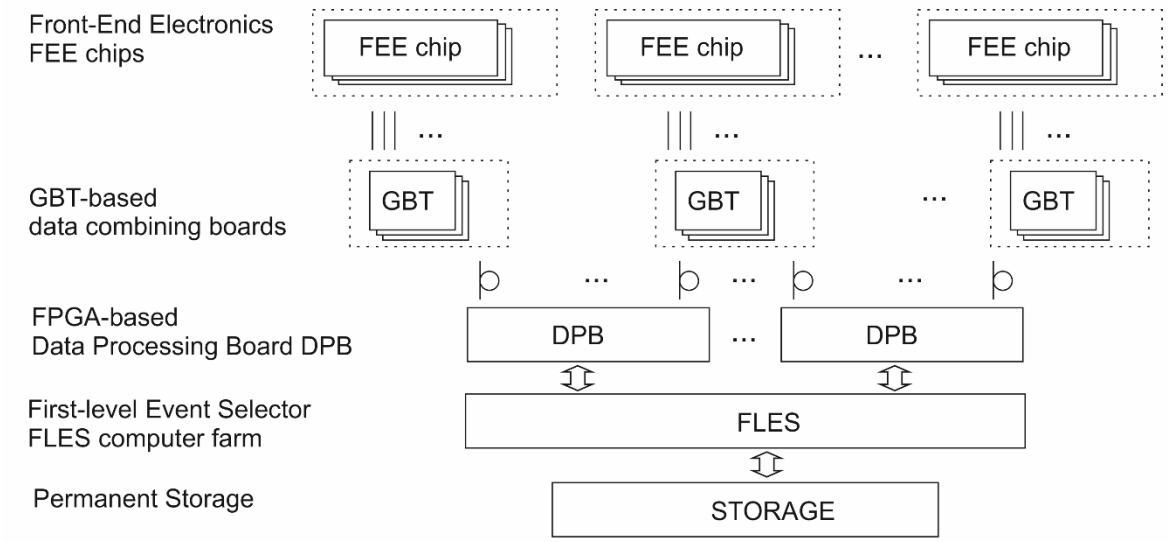



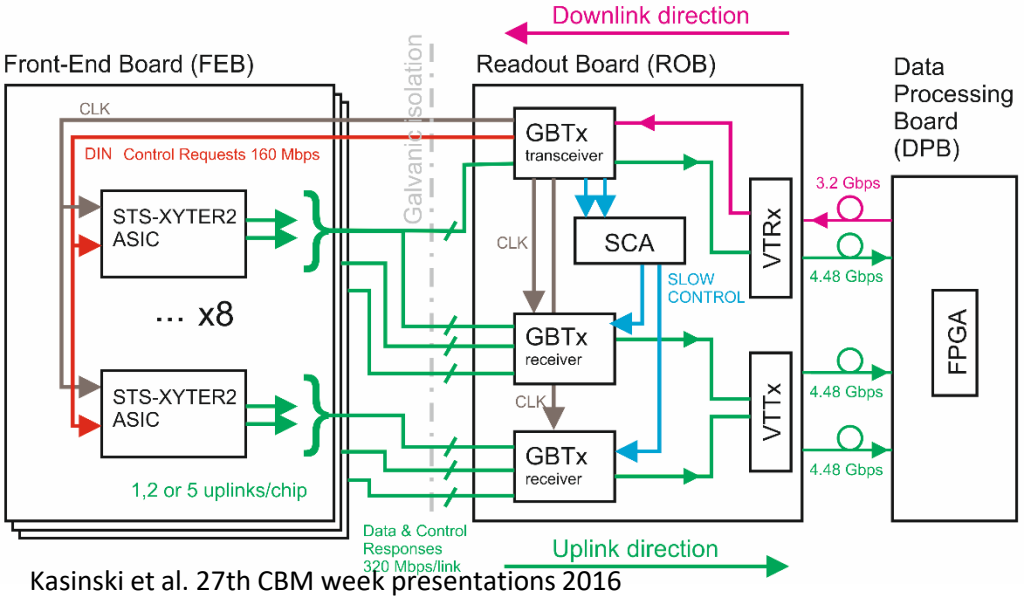
Complex & lenghty assembly process
Alignment & TAB bonding
(cable to sensor, cable to chip)
Glueing to FEB, wire-bonding,
Encapsulating, (row-by-row)
Attaching spacers and shielding to cables
Tight QA requirements.
Many tools involved.

STS metrics:
>1 790 000 channels
>14 000 ASICs
1752 FEBs
600 ROBs
78 DPB s


Motivation: Sucessful module assembly is a challenge – many things can go wrong in between.
Process cannot be fully automated. Some thing can be reworked though... (if the problem is detected early enough)
**This requires effective testing procedures and hardware on each step.**

# STS DAQ & Protocol



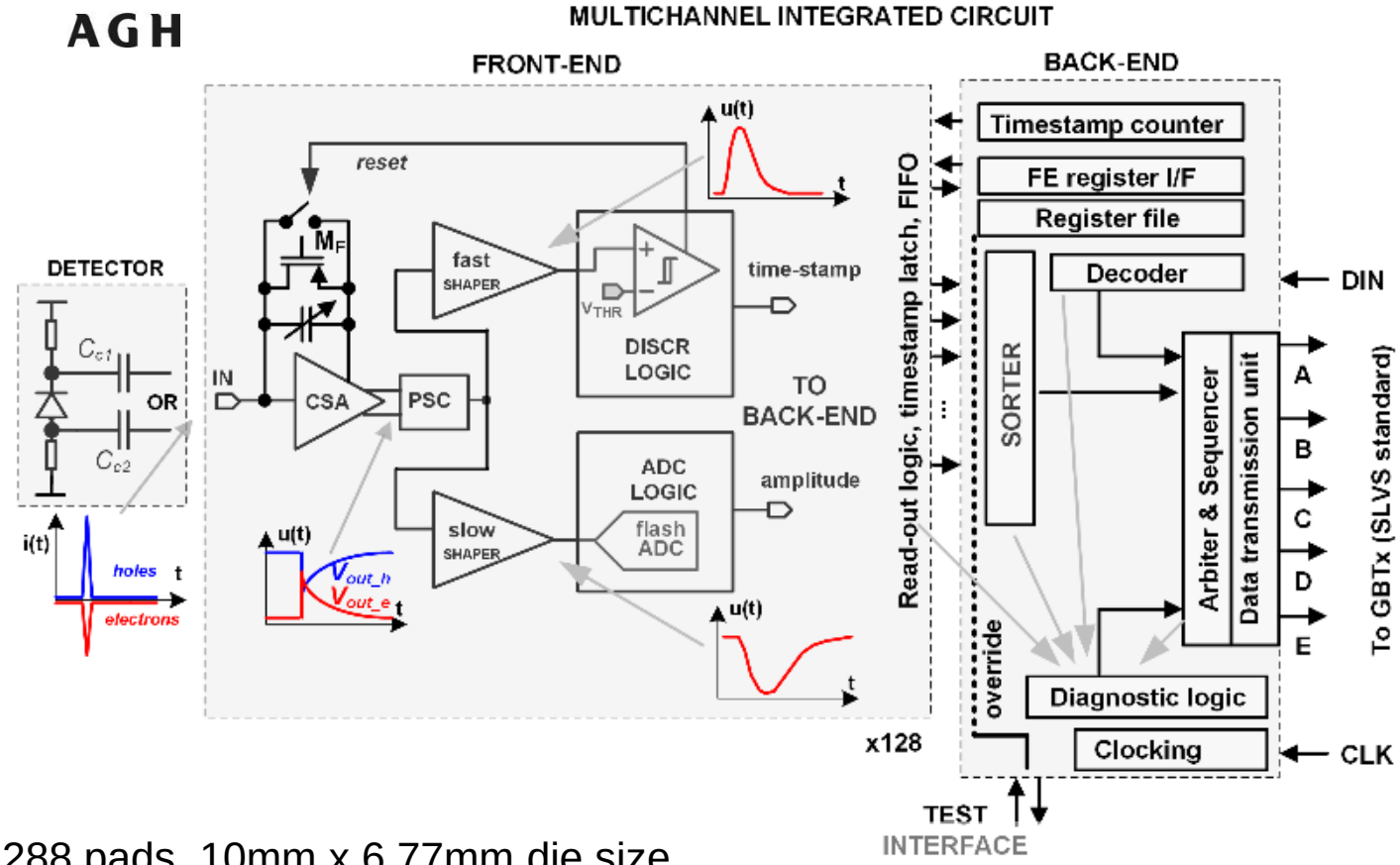



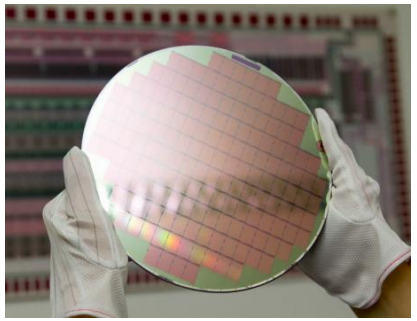

**Chips are operated via GBTx e-links and dedicated protocol STS-HCTSP.**
**Control requests BW:** 2.6 Mframes/s (shared among 8 chips)
**Scalable readout BW:** 9.41 – 47 Mhit/s/chip

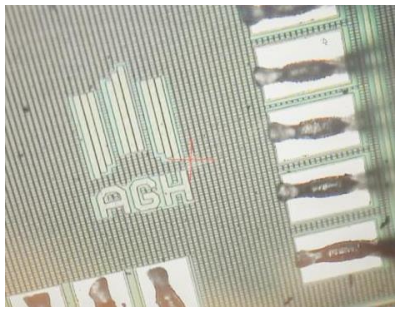
Front-end. register access,
DAQ control,
Throttling features,
Debugging features,
SEU monitoring,
others…

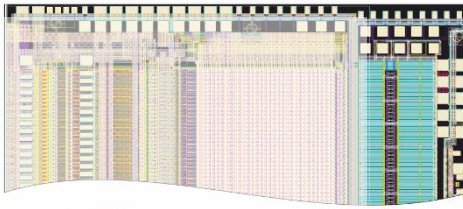

Kasinski et al. 27th CBM week presentations 2016
Kasinski, Zabolotny et al. NIM A. (during review, 2016)
Kasinski, Zabolotny, Szczygiel, „Interface and protocol development for STS read-out ASIC in the CBM experiment at FAIR, Proc. SPIE 2014.

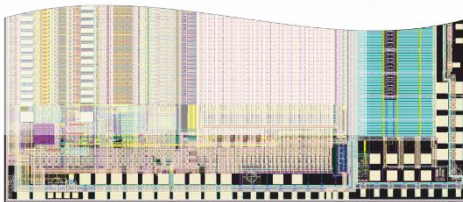
# STS-XYTER2 Front-end ASIC overview





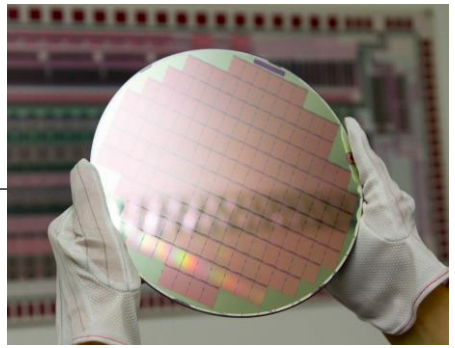




288 pads, 10mm x 6.77mm die size
130 channels + 2 diagnostic channels
4420B of AFE configuration (16 global DACs + switches + in-channel ctrl)
68 Verilog models, 10700 lines of code
54400 gates (after triplication), 12600 flops
1+ year of development

Developed by: K. Kasinski, R. Kleczek, R. Szczygiel, P. Otfinowski, AGH University

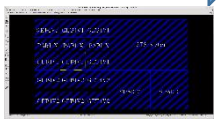
# Simplified project lifecycle



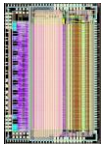
## PROTOTYPE SERIES

STS-XYTER2 ASIC TAPE-OUT 06.2016

Engineering run (MPW within CBM)



20 Wafers = 1 test wafer >900 ASICs (diced)



Performance evaluation
Yield problems identification
(what is likely to fail:
- chip-chip mismatch?
- wafer-wafer mismatch?
- yield problems? Where?
- others?

(dedicated PCB & wafer probe card)

Fix errors/bugs in the ASIC.
**Updated test plans**
for production series.

## PRODUCTION SERIES

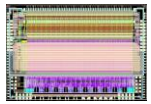
STS-XYTER2.1 ASIC TAPE-OUT 2017?

Dedicated run CMOS UMC 180 nm

min. 25000 chips ~60 wafers

WAFER-LEVEL TEST
(Good-Known Die)
Chip ID assignment.

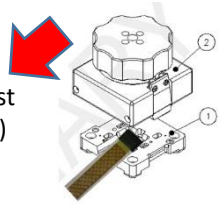
Wafer thinning
+ Stealth Laser Dicing



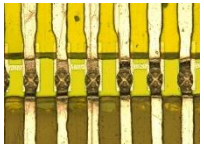
Selected dies tested on dedicated test PCB at AGH

Detailed performance evaluation

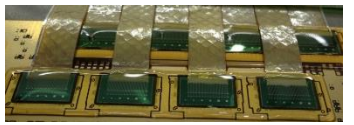
Detector module assembly #1



Intermediate test (pogo probe jig)



Rework selected traces
(if necessary)



Detector module assembly #2

Full detector module test (in-system)

Experiment assembly

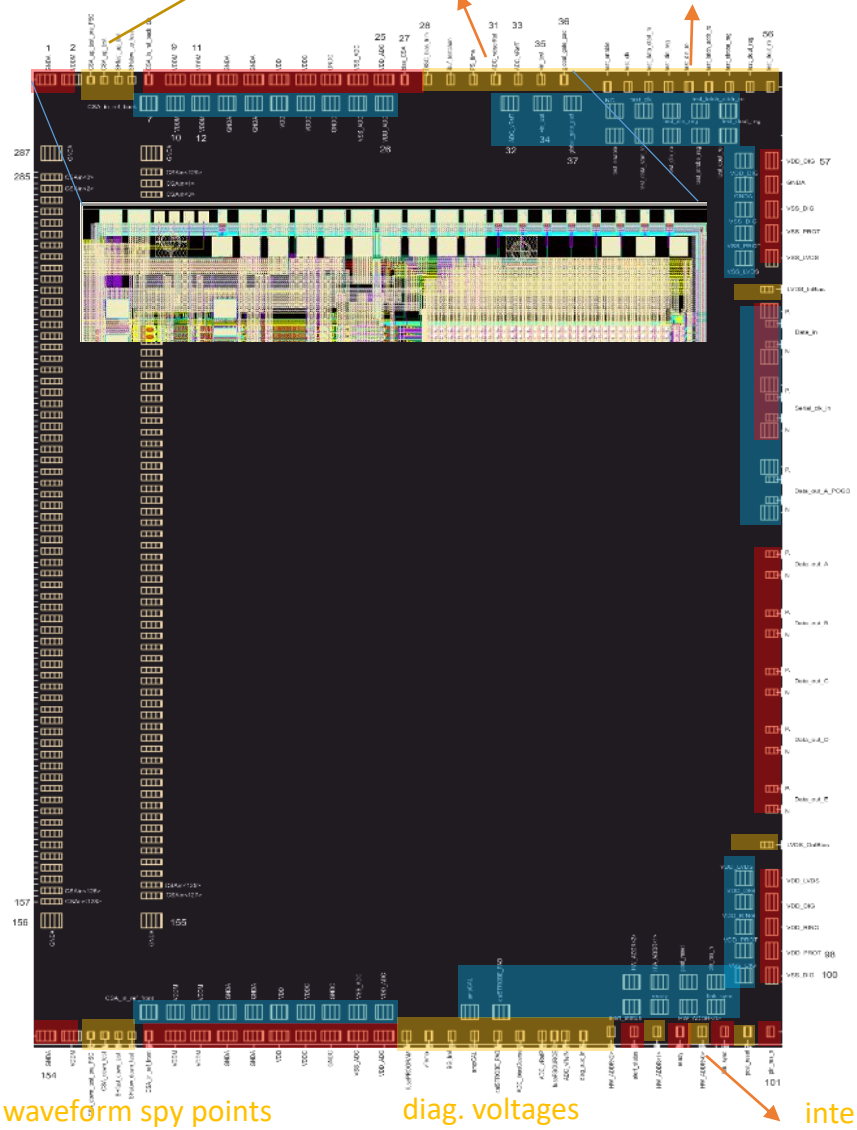
In-system tests & Commissioning

Operation

Ageing-related adjustments

Many test levels (and setups)
Different requirements for each test.

# Connectivity during tests

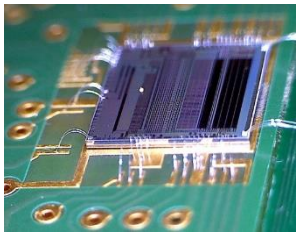



## Wafer-level:

Matrix of needles on dedicated wafer probe card.
Motorized X-Y-Z-Theta positioning chuck.
All pins accessible.

## Chip-on-board:

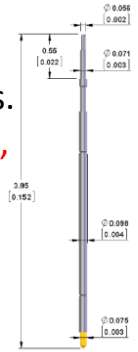
Wire-bonding to the dedicated TEST PCB.
All pins accessible.

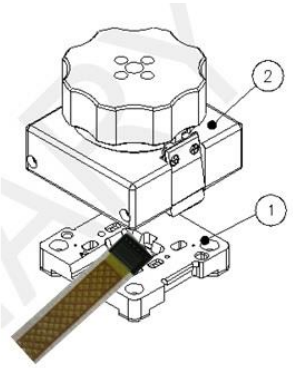


## Inter-assembly:

Pogo-probe test jig / bed of needles.
Most pads available (no waveforms, no diagnostic potentials).

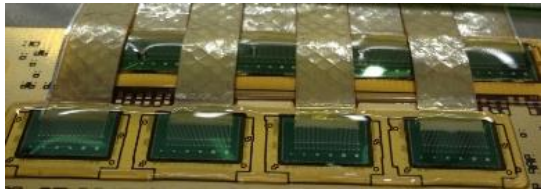
150x150 um pads, 250um pitch





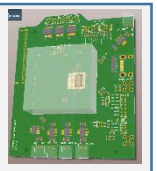

## In-system:

Wire-bonding to the FEB board. Only essential pins available (no diagnostic pads, no test interface).



# Test stages & test objectives

**PROTOTYPE DIE-ON-BOARD TEST**

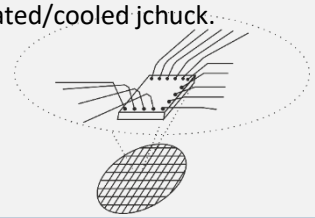


Test & measure **everything** possible.
Verify **each** functionality.
Test vs. temperature.
-> Search for bugs.
-> Search for weak points what is prone to mismatch or yield -> what needs special attention during production!

UPDATE PRODUCTION TEST LIST / PROCEDURES

**PROTOTYPE WAFEL-LEVEL TEST**

Check wafer probe card design.
Check test procedures.
**Check system before going for high-volume.**
**Temperature-related measurements** with heated/cooled jchuck.



**PRODUCTION WAFER-LEVEL TEST**

**Determine GKD Good-Known Die.**
Check everything within a short time!
Assign fusebit ID.
Calibrate chip (@Temp).

**Time is crucial!**

25000 chips
~400 chips/wafer
~62 wafers.

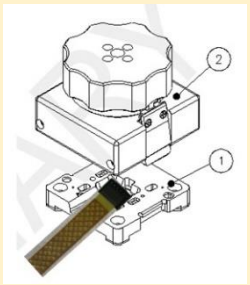
**PRODUCTION DIE-ON-BOARD TEST**

**Test & measure everything** possible including characterization **with sensor.**

**Time not important**
(few selected dies will be tested this way)

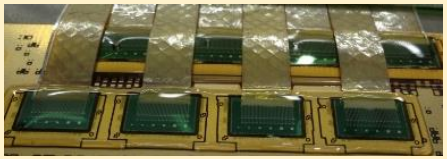
**PRODUCTION INTER-ASSEMBLY TEST**

Check if each channel is connected to the cable with sensor.
If not, rework channel.




**PRODUCTION POST-ASSEMBLY TEST**

Check if all channels work correctly after full module was assembled.
**(limited analog characterization with test pulser)**
**Calibration of channels at particular temperature.**



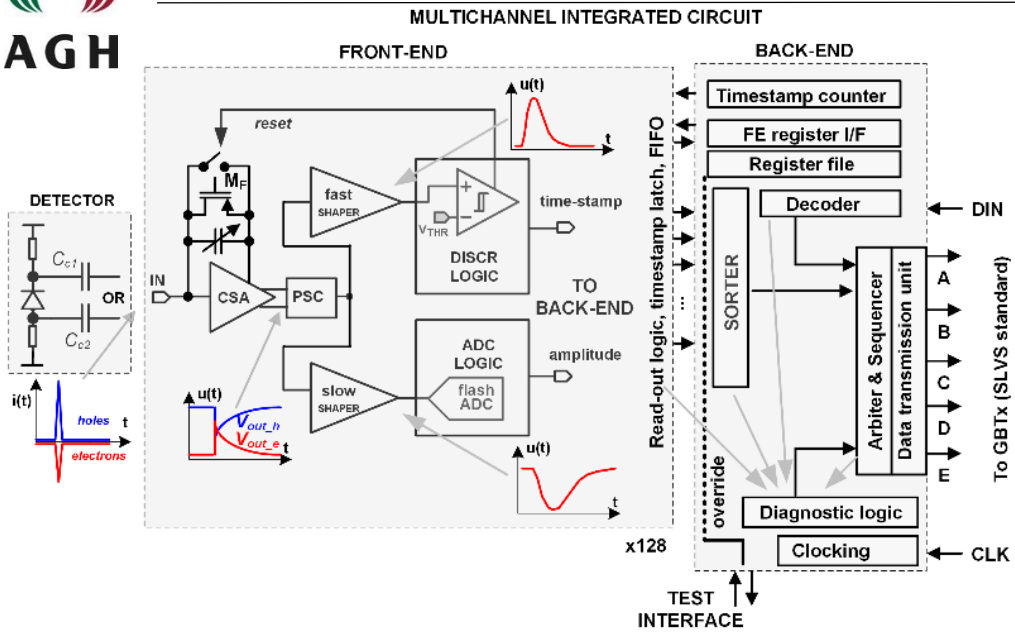
~3.5 min/chip = 23.3 h/wafer = 1 wafer/day = 62 days
~ 1 min/chip = 7h/wafer = 2-3 wafers/day = 21 - 31 days
~ 30s/chip = 3.5h/wafer = 3-6 wafers/day = 11 - 31 days

This means essentially:
no multi-temperature measurements
limited measurements requiring analog waveform acquisition
at wafer-level...

**IN-SYSTEM TUNING**

Calibrate all channels with internal pulser at target operation temperature
**(approx. -7 degC)**

# Test coverage




STX-XYTER2 is a complex chip.
Every transistor is subject to mismatch, process variation and yield problems.

100% test coverage not possible.

How to test it to minimize risk of selecting bad die?

**Coverage examples:**

**General condition:** uninitialized/initialized power consumption

**Digital:** ability to establish link, access registers, use internal test features, but not all mechanisms can be tested

**Registers:** (full custom rad-hard, synthesized): random w/r

**Current-steering DACs:** precisely measure current consumption vs. DAC value

**Voltage - biasing DACs:** dedicated diagnostic points, otherwise: tricky...

**ADC calibration:** dedicated external pin for efficient calibration of each ADC.

**Calibration pulser**: dedicated external pin (possibility to override with ext. gen)

} Essential for effective calibration of the chip

**General performance of channel:**

gain [mV/fC], (**direct**: test channel only, **indirect (via 6-bit ADC):** all channels)

peaking / rise time [ns] (only test channels),

time-walk [ns/fC], time jitter [ns rms],

discharge time constant / feedback resistance [ns] (only test channels)

noise (fast & slow paths**), direct**: test channels only, **indirect** (via hit counters: s-curves): all channels

**Important: DEFAULT settings (for optimal performance) differ vs. temperature!**

Each test / parameter to be extracted needs a test procedure, hardware, classification thresholds and test automation software

# Test procedures

- ✓ Smoke test
- ✓ Band-gap reference
- ✓ General Good/No Good test
- ✓ Test interface startup
- ✓ Front-end register's random test via TEST I/F
- ✓ Current-steering DACs
- ✓ Potential-steering DACs
- ✓ Pulser check
- ✓ 1st back-end test
- ✓ Link initialization test
- ✓ Back-end random register test
- ✓ Link masking test
- ✓ Front-end register's random test via back-end
- ✓ Full-chip default values
- ✓ 1st CSA test with pulser
- ✓ 1st PSC test with pulser
- ✓ Check Rfb settings
- ✓ 1st Shfast test with pulser
- ✓ 1st Shslow test with pulser
- ✓ ADC calibration
- ✓ All channels' Shfast path test
- ✓ All channel's Shslow path test
- ✓ All channel's trimming
- ✓ Noise measurements on configured system
- ✓ CSA reset test
- ✓ CSA speed test
- ✓ ESD protection leakage test
- ✓ Assign ID number
- ✓ .... more

**Requirements for test HW:**
All hardware programmable, preferably modular & compact.

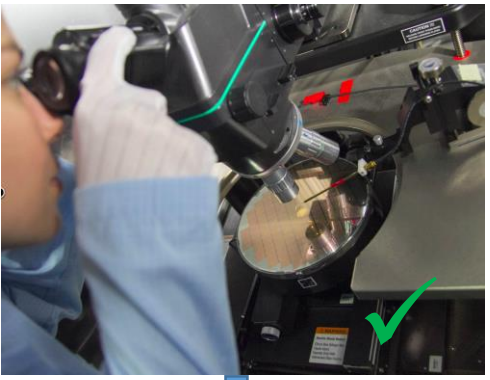
- **DC voltage measurements** (0-1.8V, 12-bit min.)
- **Current sourcing & measurements** (min. 4 - pref. 6 channels, min. 0-2 V, min. 0-0.6 A/domain, min. 200 nA resolution)
- **Waveform acquisition** (min. 9 – pref. 11 channels, BW: min. 1 GHz – pref. 3 GHz, ext. trigger)
- **Waveform generation** (min. 2 channels, min. $t_r$=10ns, 0-1.8V, min. 10-bit resolution, trigger out)
- Communication devices:

**TEST INTERFACE/CTRL BITS:**
(11 DIO, 1.8V CMOS, f=20MHz)/(4 DO, 1.8V CMOS) simple, custom serial protocol
**GBTx E-LINK INTERFACE:**
(2 CLK/DIN, 5 DOUT pairs, LVDS/SLVS, 320Mbps) dedicated serial protocol STS-HCTSP

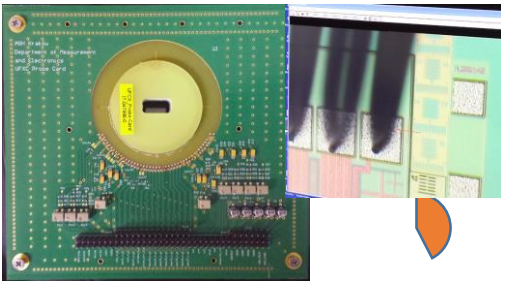
Test scope:
Initial tests
Biasing-related tests
Digital-related tests
Channel operation tests

# HW platform selection

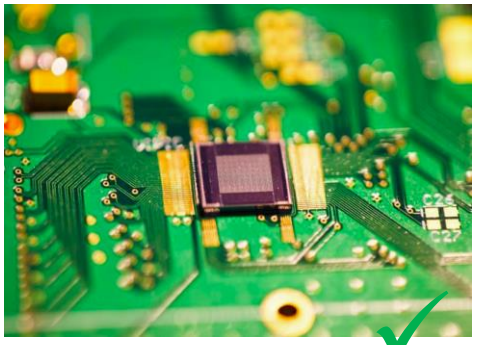
Cascade Microtech probe station



Custom wafer probe card



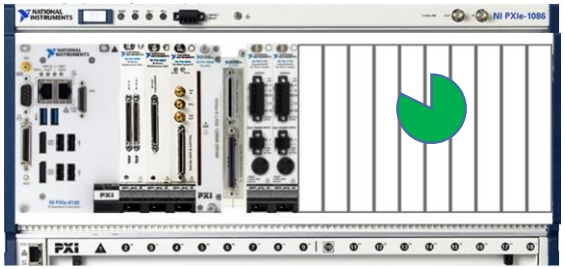
Custom test PCBs



Individual Oscilloscope, power supplies, DAQ card, generator, FPGA communication system

Too bulky

NI PXIe modular system



Compact, all-in-one
High-performance HW, Synchronization
Full Labview compatibility
Expensive

Chassis + Controller: 7 slot, NI PXIe-8135, 2.3 GHz Quad-core 8 GB RAM.
DAQ card NI 6259 - 32 AI ±2V 16-bit, 4 AO ±5V 16-bit 2.8 MS/s @1ch, 2 MS/s @2ch
SMU NI 4144 – 3-CH, ±6V, +-0.5A ...
Digitizer ... + analog switches
Signal generator

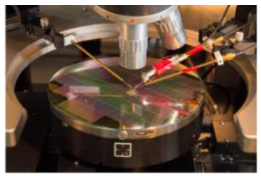
FlexRIO Virtex-5 FPGA card + Interface Module
NI 6583 – Mixed logic: 32 CMOS 1.2-3.3V, 19 LVDS pairs 200 MHz
NI 6587 – High speed 16 LVDS pairs, 810 MHz (no single ended)

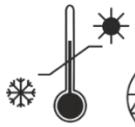
Communication? Tricky but possible.

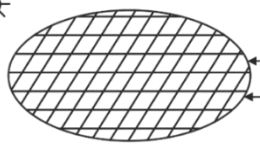
AFCK-based system developed at WUT can be also used!

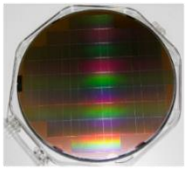
# Wafer-level test hardware options

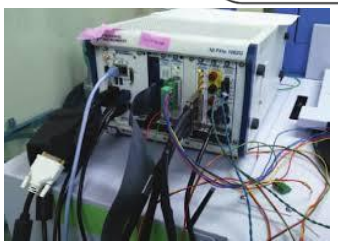
## NI PXI only

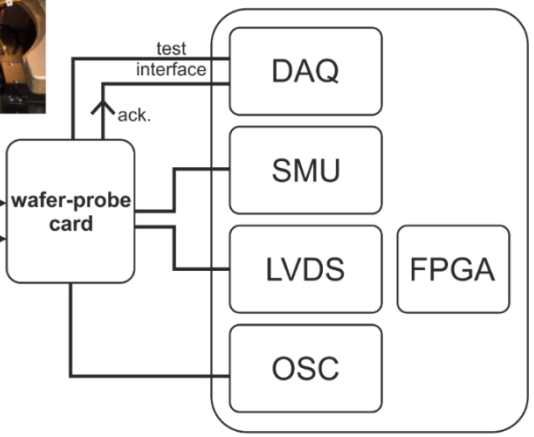








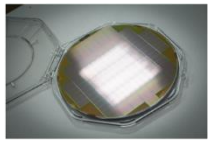


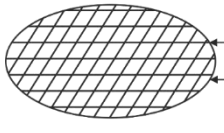


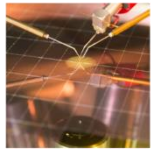

PROS:
- Compact, all-in-one, well synchronized
- Full suport of National Instruments
- Modules are available / servicable

CONS:
- problematic interfacing (adapter module selection)
- necessary to implement fully-featured protocol suport in Virtex-5 in LabVIEW environment.

## NI PXI + AFCK





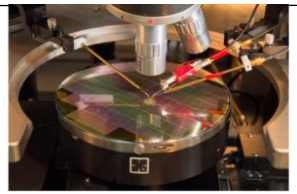





PROS:
- Interface needs not to be reimplemented
- interface similar to the final one

CONS:
- no longer compact, robust architecture. (requires instrument crate or special handling, power supply etc.)
- possible compatibility issues (drivers, functionality, availability of hardware, etc.)

# Wafer-level testing -> GOOD KNOWN DIE & ID fusebit

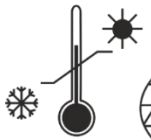


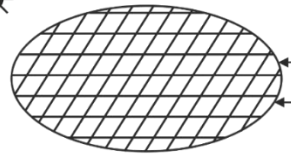
**Trade-off**

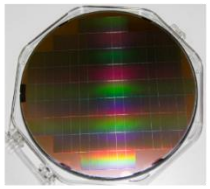
Test coverage

VS.

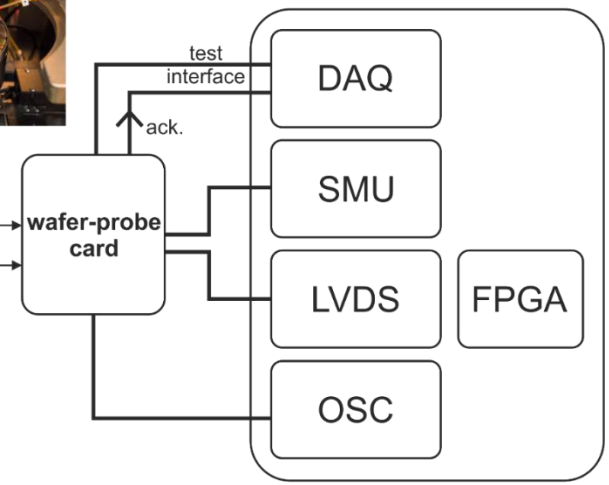
Test time

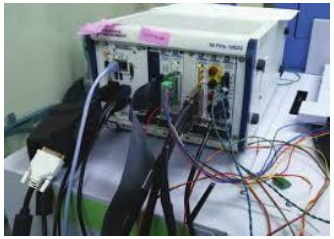






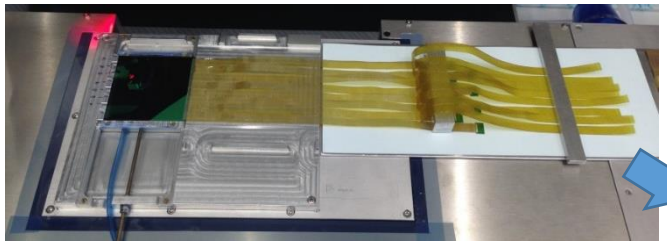
**Temperature controlled chuck ONLY ON LIMITED number of wafers.**



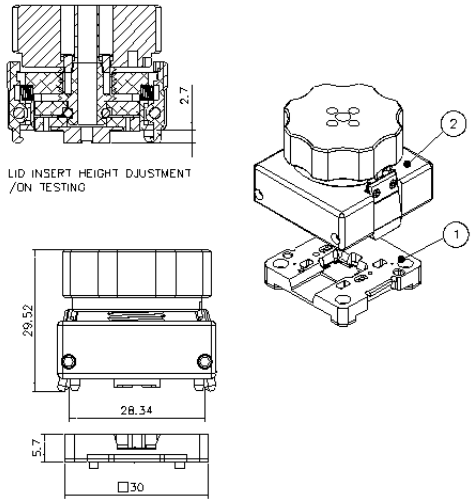



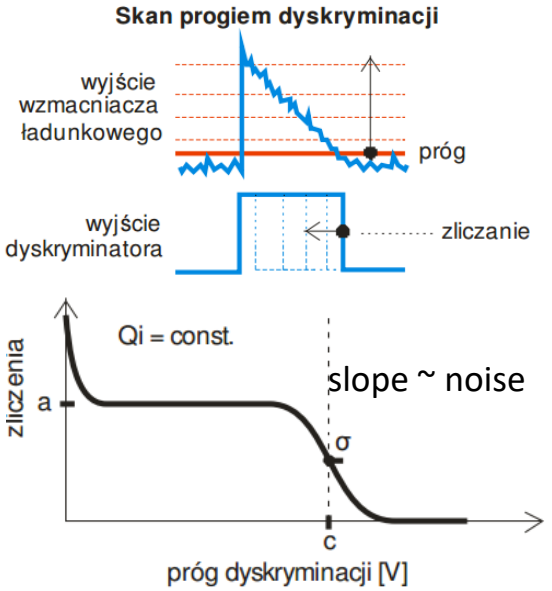
- ✓ Smoke test
- ✓ Band-gap reference
- ✓ General Good/No Good test
- ✓ Test interface startup
- ✓ Front-end register's random test via TEST I/F
- ✓ Current-steering DACs
- ✓ Potential-steering DACs
- ✓ Pulser check
- ✓ 1st back-end test
- ✓ Link initialization test
- ✓ Front-end random register test
- ✓ Link masking test
- ✓ Front-end register's random test via back-end
- ✓ Full-chip default values
- ✓ ADC calibration
- ✓ 1st CSA test with pulser
- ✓ 1st PSC test with plser
- ✓ Check Rfb settings
- ✓ 1st Shfast test with pulser
- ✓ 1st Shslow test with pulser
- ✓ All channels' Shfast path test
- ✓ All channels' Shslow path test
- ✓ All channels' trimming
- ✓ Noise measurements on configured system
- ✓ CSA reset test
- ✓ CSA speed test
- ✓ ESD protection leakage test
- ✓ Assign ID numer
- ✓ More? ....

# Test station assembly- intermediate tests



Is the noise higher (due to the larger C) in all channels?




Calibration value read from database.
Problem: temperature!

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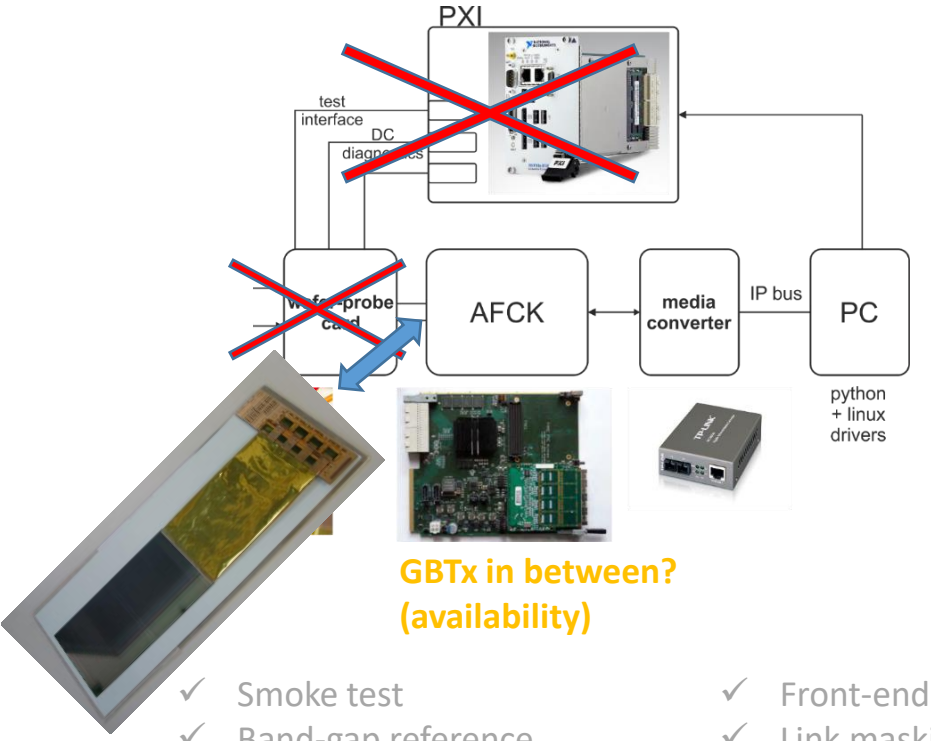
- ✓ Assign ID number

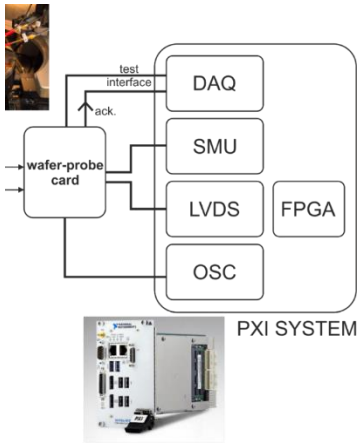
# In-system tests

## Post-module Assembly

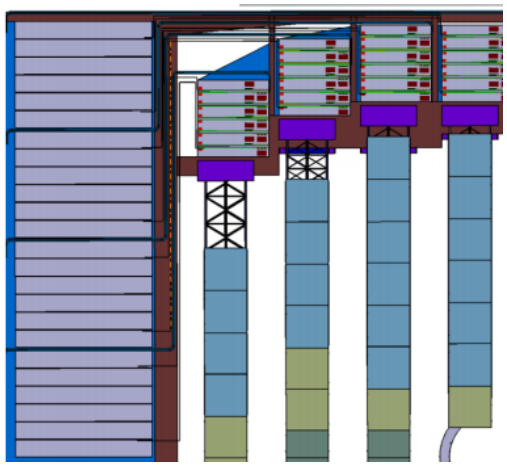



GBTx in between? (availability)

**AFCK-only or NI PXI only**




## Post Experiment Assembly full-system startup



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- ✓ Noise measurements on configured system
- ✓ CSA reset test
- ✓ CSA speed test
- ✓ ESD protection leakage test
- ✓ Assign ID number

# Summary

- Quality Assurance requires **high yield** of module assembly

(approx. 1% of channels per module can fail)

- High tech + complicated supply chain + assembly procedures require :

efficient test systems & procedures at various levels of experiment subsystems assembly.

- **HW proposal is ready** based on previous, successful experiences (wafer-level, chip-on-board testing)
- **Test procedures are proven** based on previous prototypes but need refinement after 1st ASICs are on the bench
- **Few open points:**
  - Testing environment & time limit affecting the test procedures / tests that can be performed
  - Communication with chip (NI Virtex card or AFCK system or BOTH?)
  - How the automated test software (NI LabVIEW) should effectively communicate with AFCK?

References:


C. Simons et al., „Status of STS-module-assembly at GSI", 27th CBM Week

W. Zabolotny, K. Kasinski, R. Szczygiel, „Tests of the STS-XYTER model and protocol", 27th CBM Week.

W. Zabolotny, K. Kasinski, R. Szczygiel „Tests of the STS-XYTER model and protocol", 27th CBM Week.

K. Kasinski, R. Kleczek, „A flexible, low-noise charge-sensitive amplifier for particle tracking applications", (will be presented on 2016 MIXDES conference)

K. Kasinski, R. Kleczek, R. Szczygiel, „*Front-end readout electronics considerations for Silicon Tracking System and Muon Chamber", Journal of Instrumentation 2016 vol. 11 C02024*

P. Otfinowski, P. Grybos, R. Szczygiel, K. Kasinski, „Offset correction system for 128-channel self-triggering readout chip with in-channel 5-bit Energy measurement functionality" Nuclear Instruments & Methods A 2015 vo. 780 p. 114-118.

R. Kleczek, K. Kasinski, R. Szczygiel, P. Otfinowski, P. Grybos, „Noise optimization of the time and Energy measuring ASIC for Silicon Tracking System", Proceedings of MIXDES 2015.

K. Kasinski, R. Kleczek, C. J. Schmidt, „Optimization of the microcable and detector parameters towards low noise in the STS readout system", Proc. SPIE vol. 9662.

K. Kasinski, W. Zabolotny, J. Lehnert, C. J. Schmidt, W. F. J. Mueller, R. Szczygiel, „STS-HCTSP, an STS hit & control transfer synchronous protocol" CBM Progress report 2014.

K. Kasinski, R. Kleczek, R. Szczygiel, P. Grybos, P. Otfinowski, „Towards the STS-XYTERv2, a silicon strip detector readout chip for the STS", CBM Progress report 2014.