“Test systems of the STS/MUCH-XYTER2 ASIC - from wafer-level to in-system verification”

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01.06.2016
Agenda

1. Introduction to CBM experiment, STS detector architecture, DAQ structure
2. STS module construction (detector + microcable + ASIC + FEB board)
3. Motivation
4. STS-XYTER2 ASIC & project roadmap
5. Proposed test procedures & methodologies
6. Proposed test systems for each stage
7. Summary & further steps
Goal: exploration of the QCD phase diagram in the region of very high baryon densities

- up to 10 MHz interactions
- **self-triggering** front-end chip
- radiation doses

STS: track reconstruction and momentum determination of charged particles in 1T dipole field, 8 detector stations (30cm – 100 cm from target)
• **Silicon Tracking System (STS)**
  - double–sided, micro-strip sensors, 1024 channels per side, 7.5° stereo angle, strip pitch of 58 µm, sensor lengths 20 - 60 mm, 300 µm silicon thickness,
  - sensors read out through multi-line micro-cables (sandwiched polyimide-Aluminum layers of several 10 µm thickness).
  - readout electronics (STS-XYTER2 chips) located at the perimeter of the detector stations on FEB boards (8 chips/board).
  - Data concentrators (GBTx-based ROB boards) also located nearby
STS modules assembly


Ingredients for single module:
1 Detector (1024 strips/side)
16 STS-XYTER2 chips
32 microcables
2 Front-end boards
2 shielding layers and spacers

Complex & lengthy assembly process
Alignment & TAB bonding
(cable to sensor, cable to chip)
Glueing to FEB, wire-bonding,
Encapsulating, (row-by-row)
Attaching spacers and shielding to cables
Tight QA requirements.
Many tools involved.

STS metrics:
>1 790 000 channels
>14 000 ASICs
1752 FEBs
600 ROBs
78 DPB s

Motivation: Successful module assembly is a challenge – many things can go wrong in between.
Process cannot be fully automated. Some thing can be reworked though... (if the problem is detected early enough)
This requires effective testing procedures and hardware on each step.
Chips are operated via GBTx e-links and dedicated protocol STS-HCTSP.  
**Control requests BW**: 2.6 Mframes/s (shared among 8 chips)  
**Scalable readout BW**: 9.41 – 47 Mhit/s/chip

Front-end. register access,  
DAQ control,  
Throttling features,  
Debugging features,  
SEU monitoring,  
others...

Kasinski et al. 27th CBM week presentations 2016  
Kasinski, Zabolotny et al. NIM A. (during review, 2016)  
STS-XYTER2 Front-end ASIC overview

MULTICORE INTEGRATED CIRCUIT

288 pads, 10mm x 6.77mm die size
130 channels + 2 diagnostic channels
4420B of AFE configuration (16 global DACs + switches + in-channel ctrl)
68 Verilog models, 10700 lines of code
54400 gates (after triplication), 12600 flops
1+ year of development

Developed by: K. Kasinski, R. Kleczek, R. Szczygiel, P. Otfnowski, AGH University
Simplified project lifecycle

**PROTOTYPE SERIES**

- **STS-XYTER2 ASIC**
  - **TAPE-OUT 06.2016**
  - Engineering run (MPW within CBM)
  - 20 Wafers
  - 1 test wafer
  - >900 ASICs (diced)

- **Performance evaluation**
  - Yield problems identification
    - what is likely to fail:
      - chip-chip mismatch?
      - wafer-wafer mismatch?
      - yield problems? Where?
      - others?
      - (dedicated PCB & wafer probe card)

- **Fix errors/bugs in the ASIC.**
  - Updated test plans for production series.

**PRODUCTION SERIES**

- **STS-XYTER2.1 ASIC**
  - **TAPE-OUT 2017?**
  - Dedicated run CMOS UMC 180 nm
  - min. 25000 chips
    - ~60 wafers
  - WAFER-LEVEL TEST
    - (Good-Known Die)
    - Chip ID assignment.
  - Wafer thinning + Stealth Laser Dicing
  - Detector module assembly #1
  - Intermediate test (pogo probe jig)
  - Detector module assembly #2
  - Full detector module test (in-system)

**Many test levels (and setups)**
**Different requirements for each test.**

- Ageing-related adjustments
- Operation
- In-system tests & Commissioning
- Experiment assembly

- **Detailed performance evaluation**
Connectivity during tests

Wafer-level:

Chip-on-board:
Wire-bonding to the dedicated TEST PCB. All pins accessible.

Inter-assembly:
Pogo-probe test jig / bed of needles. Most pads available (no waveforms, no diagnostic potentials).
150x150 um pads, 250um pitch

In-system:
Wire-bonding to the FEB board. Only essential pins available (no diagnostic pads, no test interface).
Test stages & test objectives

**PROTOTYPE DIE-ON-BOARD TEST**
Test & measure everything possible. Verify each functionality. Test vs. temperature.
- Search for bugs.
- Search for weak points what is prone to mismatch or yield -> what needs special attention during production!

**UPDATE PRODUCTION TEST LIST / PROCEDURES**

**PROTOTYPE WAFER-LEVEL TEST**

**Determine GKD Good-Known Die.**
Check everything within a short time!
 Assign fusebit ID.
 Calibrate chip (@Temp).

**Time is crucial!**
25000 chips
~400 chips/wafer
~62 wafers.

~3.5 min/chip = 23.3 h/wafer = 1 wafer/day = 62 days
~ 1 min/chip = 7h/wafer = 2-3 wafers/day = 21 - 31 days
~ 30s/chip = 3.5h/wafer = 3-6 wafers/day = 11 - 31 days

This means essentially:
no multi-temperature measurements
limited measurements requiring analog waveform acquisition at wafer-level...

**PRODUCTION DIE-ON-BOARD TEST**

Test & measure everything possible including characterization with sensor.

**Time not important**
(few selected dies will be tested this way)

**PRODUCTION INTER-ASSEMBLY TEST**
Check if each channel is connected to the cable with sensor.
If not, rework channel.

**PRODUCTION POST-ASSEMBLY TEST**
Check if all channels work correctly after full module was assembled.
(limited analog characterization with test pulser)
Calibration of channels at particular temperature.

**IN-SYSTEM TUNING**
Calibrate all channels with internal pulser at target operation temperature (approx. -7 degC)
STX-XYTER2 is a complex chip. Every transistor is subject to mismatch, process variation and yield problems.

100% test coverage not possible.

How to test it to minimize risk of selecting bad die?

Coverage examples:

**General condition:** uninitialized/initialized power consumption

**Digital:** ability to establish link, access registers, use internal test features, but not all mechanisms can be tested

**Registers:** (full custom rad-hard, synthesized): random w/r

**Current-steering DACs:** precisely measure current consumption vs. DAC value

**Voltage - biasing DACs:** dedicated diagnostic points, otherwise: tricky...

**ADC calibration:** dedicated external pin for efficient calibration of each ADC.

**Calibration pulser:** dedicated external pin (possibility to override with ext. gen)

**General performance of channel:**

- gain [mV/fC], (direct: test channel only, indirect (via 6-bit ADC): all channels)
- peaking / rise time [ns] (only test channels),
- time-walk [ns/fC], time jitter [ns rms],
- discharge time constant / feedback resistance [ns] (only test channels)
- noise (fast & slow paths), direct: test channels only, indirect (via hit counters: s-curves): all channels

**Important:** DEFAULT settings (for optimal performance) differ vs. temperature!
Test procedures

Requirements for test HW:
All hardware programmable, preferably modular & compact.

- **DC voltage measurements** (0-1.8V, 12-bit min.)
- **Current sourcing & measurements** (min. 4 - pref. 6 channels, min. 0-2 V, min. 0-0.6 A/domain, min. 200 nA resolution)
- **Waveform acquisition** (min. 9 – pref. 11 channels, BW: min. 1 GHz – pref. 3 GHz, ext. trigger)
- **Waveform generation** (min. 2 channels, min. \(t_r=10\text{ns}, 0-1.8V, \text{min. 10-bit resolution, trigger out}\))

Communication devices:
**TEST INTERFACE/CTRL BITS:**
(11 DIO, 1.8V CMOS, f=20MHz)/(4 DO, 1.8V CMOS) simple, custom serial protocol

**GBTx E-LINK INTERFACE:**
(2 CLK/DIN, 5 DOUT pairs, LVDS/SLVS, 320Mbps) dedicated serial protocol STS-HCTSP

Test scope:
Initial tests
Biasing-related tests
Digital-related tests
Channel operation tests
HW platform selection

Individual Oscilloscope, power supplies, DAQ card, generator, FPGA communication system

Cascade Microtech probe station

Custom wafer probe card

Custom test PCBs

NI PXIe modular system

Chassis + Controller: 7 slot, NI PXIe-8135, 2.3 GHz Quad-core 8 GB RAM.
DAQ card NI 6259 - 32 AI ±2V 16-bit, 4 AO ±5V 16-bit 2.8 MS/s @1ch, 2 MS/s @2ch
SMU NI 4144 – 3-CH, ±6V, ±-0.5A ...
Digitizer ... + analog switches
Signal generator

FlexRIO Virtex-5 FPGA card + Interface Module
NI 6583 – Mixed logic: 32 CMOS 1.2-3.3V, 19 LVDS pairs 200 MHz
NI 6587 – High speed 16 LVDS pairs, 810 MHz (no single ended)

Communication? Tricky but possible.
AFCK-based system developed at WUT can be also used!
Wafer-level test hardware options

PROS:
- Compact, all-in-one, well synchronized
- Full support of National Instruments
- Modules are available / servicable

CONS:
- Problematic interfacing (adapter module selection)
- Necessary to implement fully-featured protocol support in Virtex-5 in LabVIEW environment.

PROS:
- Interface needs not to be reimplemented
- Interface similar to the final one

CONS:
- No longer compact, robust architecture.
  (Requires instrument crate or special handling, power supply etc.)
- Possible compatibility issues (drivers, functionality, availability of hardware, etc.)
Wafer-level testing -> GOOD KNOWN DIE & ID fusebit

Trade-off

Test coverage vs. Test time

Temperature controlled chuck ONLY ON LIMITED number of wafers.

✓ Smoke test
✓ Band-gap reference
✓ General Good/No Good test
✓ Test interface startup
✓ Front-end register’s random test via TEST I/F
✓ Current-steering DACs
✓ Potential-steering DACs
✓ Pulser check
✓ 1st back-end test
✓ Link initialization test
✓ Front-end random register test
✓ Link masking test
✓ Front-end register’s random test via back-end
✓ Full-chip default values
✓ ADC calibration
✓ 1st CSA test with pulser
✓ 1st PSC test with plser
✓ Check Rfb settings
✓ 1st Shfast test with pulser
✓ 1st Shslow test with pulser
✓ All channels’ Shfast path test
✓ All channels’ Shslow path test
✓ All channels’ trimming
✓ Noise measurements on configured system
✓ CSA reset test
✓ CSA speed test
✓ ESD protection leakage test
✓ Assign ID numer
✓ More? ....
Test station assembly - intermediate tests

Is the noise higher (due to the larger C) in all channels?

- Smoke test
- Band-gap reference
- General Good/No Good test
- Test interface startup
- Front-end register’s random test via TEST I/F
- Current-steering DACs
- Potential-steering DACs
- Pulser check
- 1st back-end test
- Link initialization test
- Front-end random register test
- Link masking test
- Front-end register’s random test via back-end

- Full-chip default values
- 1st CSA test with pulser
- 1st PSC test with plser
- Check Rfb settings
- 1st Shfast test with pulser
- 1st Shslow test with pulser
- ADC calibration
- All channels’ Shfast path test
- All channels’ Shslow path test
- All channels’ trimming
- Noise measurements on configured system
- CSA reset test
- CSA speed test
- ESD protection leakage test
- Assign ID number

Problem: temperature!

Calibration value read from database.

slope ~ noise

Is the noise higher (due to the larger C) in all channels?
In-system tests

Post-module Assembly

✓ Smoke test
✓ Band-gap reference
✓ General Good/No Good test
✓ Test interface startup
✓ Front-end register’s random test via TEST I/F
✓ Current-steering DACs
✓ Potential-steering DACs
✓ Pulser check
✓ 1st back-end test
✓ Link initialization test
✓ Front-end random register test
✓ Link masking test
✓ Front-end register’s random test via back-end
✓ Full-chip default values
✓ 1st CSA test with pulser
✓ 1st PSC test with plser
✓ Check Rfb settings
✓ 1st Shfast test with pulser
✓ 1st Shslow test with pulser
✓ ADC calibration
✓ All channels’ Shfast path test
✓ All channels’ Shslow path test
✓ All channels’ trimming
✓ Noise measurements on configured system
✓ CSA reset test
✓ CSA speed test
✓ ESD protection leakage test
✓ Assign ID number

AFCK-only or NI PXI only

Post Experiment Assembly full-system startup

GBTx in between? (availability)
Quality Assurance requires high yield of module assembly (approx. 1% of channels per module can fail)

High tech + complicated supply chain + assembly procedures require:

- efficient test systems & procedures at various levels of experiment subsystems assembly.

- **HW proposal is ready** based on previous, successful experiences (wafer-level, chip-on-board testing)

- **Test procedures are proven** based on previous prototypes but need refinement after 1st ASICs are on the bench

- **Few open points:**
  - Testing environment & time limit affecting the test procedures / tests that can be performed
  - Communication with chip (NI Virtex card or AFCK system or BOTH?)
  - How the automated test software (NI LabVIEW) should effectively communicate with AFCK?
References:
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