Preparation of COTS TMS570 MCU for use in Ionizing Radiation Environments

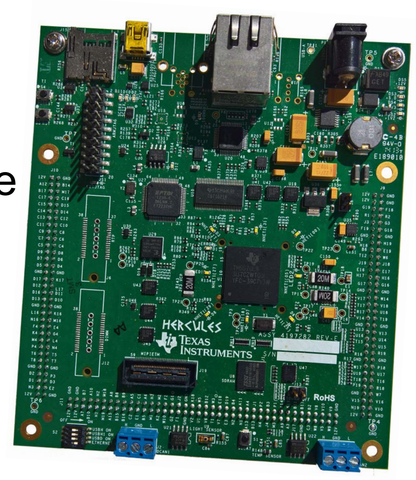
Jano Gebelein, Pritesh Gudge and Udo Kebschull

Infrastructure and Computer Systems for Data Processing (IRI), Goethe University Frankfurt

ABSTRACT Development and irradiation test of a post-production dynamic memory scrubbing routine for the CPU-coupled SRAM of the COTS TMS570 dual-CPU µC ASIC to prevent error accumulation at runtime for use in particle detector control systems. The techniques combine hardware/software co-design concepts, resulting in low design complexity, high performance and high reliability. The current implementation successfully corrects all SBUs with a mean time of 5.5 ms.

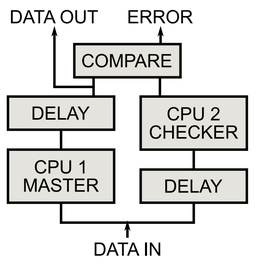
DUT BOARD Hercules Development Kit & Texas Instruments BGA

- Hercules TMDS570LS31HDK
- 64 Mbit ISSI BGA DRAM (max. 256 Mbit exchangeable)
- Sensors: Brightness, Temperature
- Interfaces: CAN, USB, JTAG, SD
- Voltage: 5V - 12V DC
- Current: 130 mA @ full speed
- Dimensions: 12,5 x 10,9 cm
- Dimensions: 4.9” x 4.3”

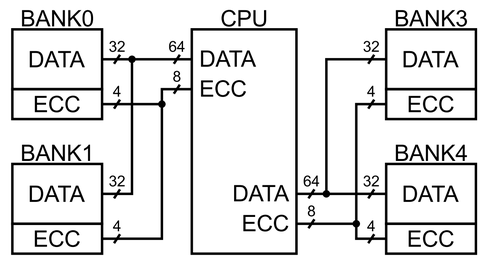


MICROCONTROLLER

- Texas Instruments TMS570LS3137
- ARM Cortex-R4F 32-bit RISC CPU
- 180 MHz dual-pipeline lockstep CPU
- Safety for CPU, DRAM, SRAM, Flash
- ECC on SRAM and Flash memory
- Real-time features, timers, ADCs
- Double-pipelined memory interface



Lockstep Mode



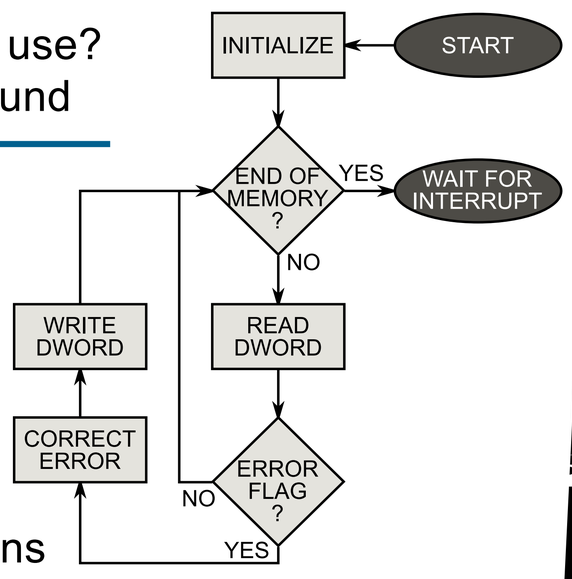
TMS570 RAM Interface

EMBEDDED SRAM

- 64bit double word extended by 8 bit SECDED ECC
- Physical address interleaving → MBU mitigation
- Drawback #1: error detection only on 'read' cmd
- Drawback #2: error correction only on 'write' cmd
- Drawback #3: no update in standby → error accumulation
- **Problem**: How to protect against error accumulation in long-term use?
- **Solution**: Manually run Read-Modify-Write operations in background

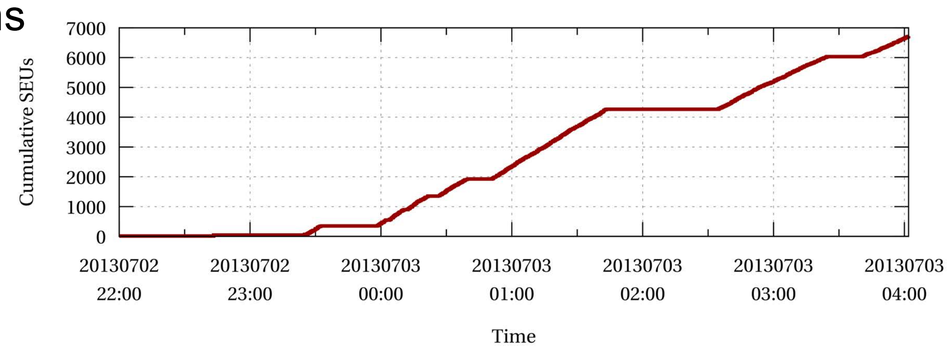
ALGORITHM of the dynamic memory scrubber

- initiated by user-configurable CPU timer (1ms to 100s)
- time interval depending on environmental radiation conditions
- continuously cycles whole memory to prevent SBU accumulation
- erroneous words flagged by CPU and corrected by algorithm
- run-time optimization: 'write' cmd only if 'read' cmd reveals SBU
- load-optimization: designed in Assembler with ARMv7R instructions



BEAM TEST VALIDATION at the COSY proton accelerator in Jülich, Germany

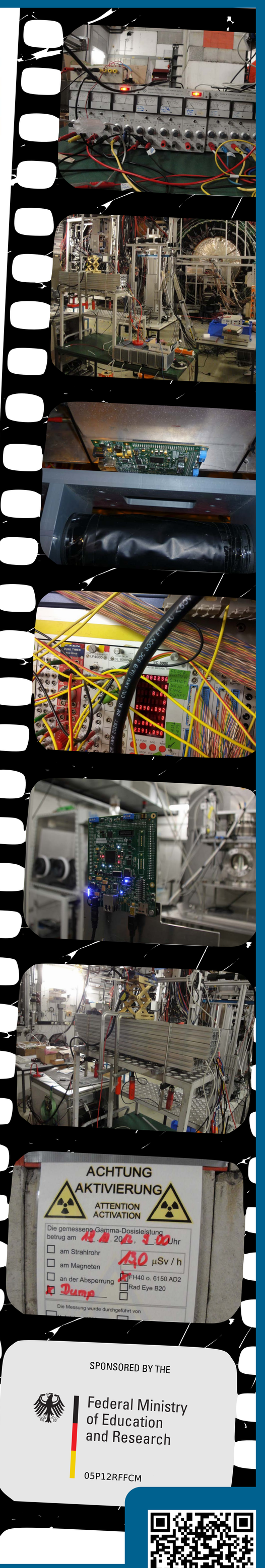
- Mean time for 256KB SRAM refresh: 5.5ms
- Particle Energy: 2 GeV protons
- Particle Flux: $5 \cdot 10^6$ $p^+ \cdot s^{-1} \cdot cm^{-2}$
- Irradiation angle: 90°
- Total irradiation period: 14h
- Total device resets: 11 (incl. 5 MBU)
- Total corrected SRAM SBUs: 13216
- SBU counter of longest run (6h with 6722 corrected SBUs) shown here ↗



CONCLUSIONS & APPLICATION SCENARIO

- COTS microcontroller's dual pipeline in lockstep mode performs great with fast hadrons
- Embedded SRAM performs great when operated with dynamic memory scrubbing
- Automotive grade µC provides long-term support, availability and low price
- TMS570 capable of operating RTEMS and EPICS in particle physics environment
- Flash memory contains static bootloader only (charge pumps will break)
- Latest configuration image dynamically loaded via Ethernet
- Device ready to be used in Detector Control System (DCS)

→ Custom DCS-Board for GSI/FAIR currently under development



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Contact: gebelein@iri.uni-frankfurt.de