6-bit low power area efficient SAR ADC for CBM MUCH ASIC

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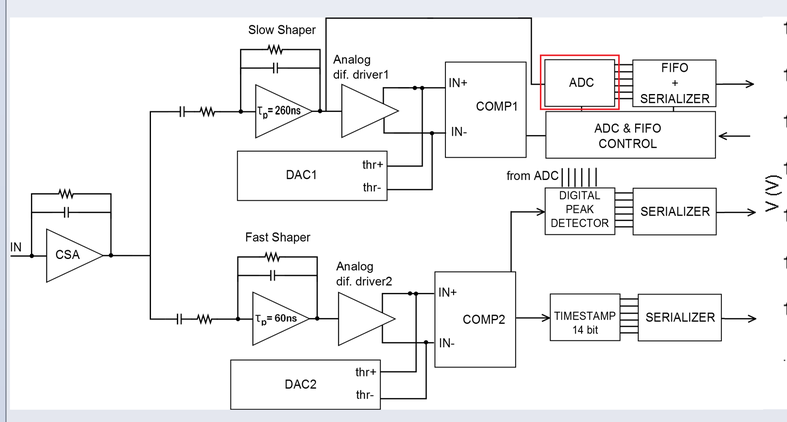
Abstract

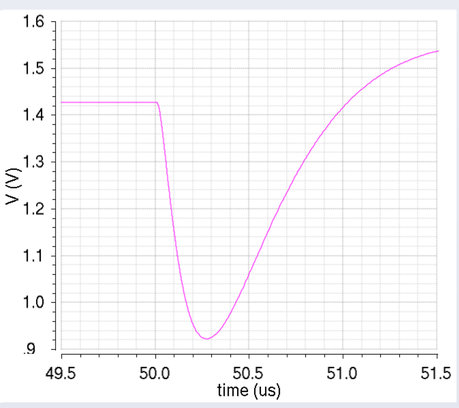
The paper describes a SAR ADC, elaborated for digitizing the shaper signal of the read-out CBM MUCH ASIC. The MUCH ASIC was designed and prototyped by means of the 180 nm CMOS MMRF process of UMC (Taiwan). Each channel of ASIC consists of a CSA, fast and slow shapers, discriminator, ADC and a digital peak detector. ADC has a power consumption of 1.5 mW at 40 Ms/s and an occupied area of 0.0162 mm^2 for using an ADC in a multichannel structure.

Introduction

Nowadays in multichannel read-out ASICs for physical experiments there is observed a trend to digitizing the signal from detector at an early stage and signal processing in digital domain (digital peak detector, digital filtration, base-line correction etc.). It becomes necessary to use the ADC in each channel of read-out ASIC and quite rigid specifications are set to ADCs in terms of power consumption and occupied area.



ADC in MUCH ASIC structure



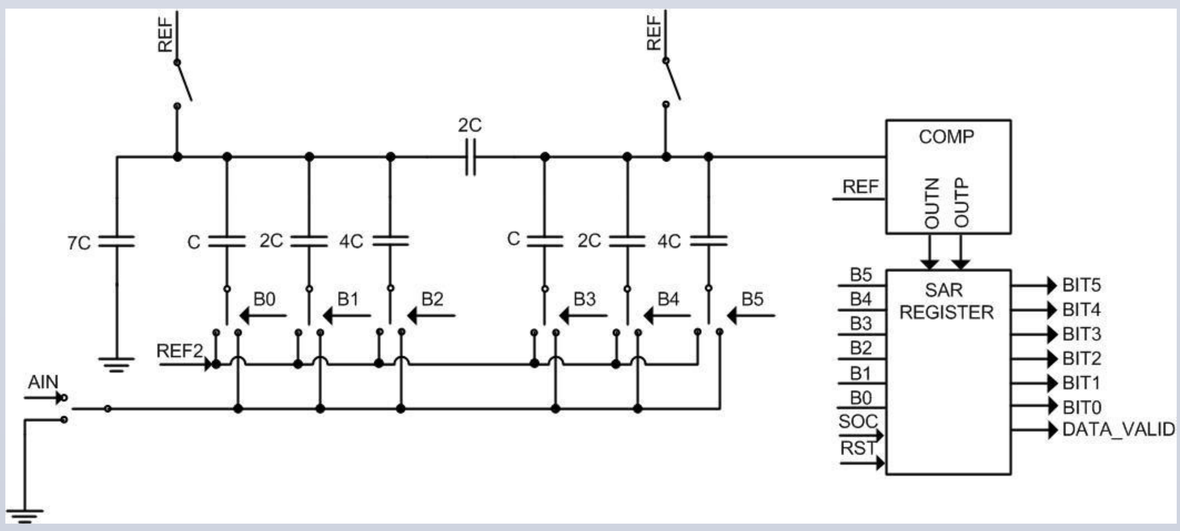
Shaper output

The ADC was designed for a prototype read-out ASIC for the GEM detectors muon chambers of the CBM experiment. Each channel of the ASIC consists of a CSA, followed by two chains: fast and slow. The slow chain is needed to determine the detector signal amplitude and consists of a shaper, discriminator, ADC and digital peak detector. Fast chain consists of a shaper and discriminator. It determines the timestamp. When the discriminator in fast chain generates a signal, the digital logic sends the sequence of “start of conversion” pulses to ADC. Digital peak detector tracks the ADC code and determines the maximum amplitude of shaper response.

Architecture

The ADC has been built by the conventional SAR architecture. It consists of: capacitor matrix, successive approximation register, comparator and analog switches. For reduction of occupancy area, the capacitor matrix has two stages. In result the matrix has an overall capacitance of 0.92 pF (the least capacitor of matrix equals 40 fF) instead of 1.56 pF for the one stage matrix. That reduces the area of the ADC by one and a half times.

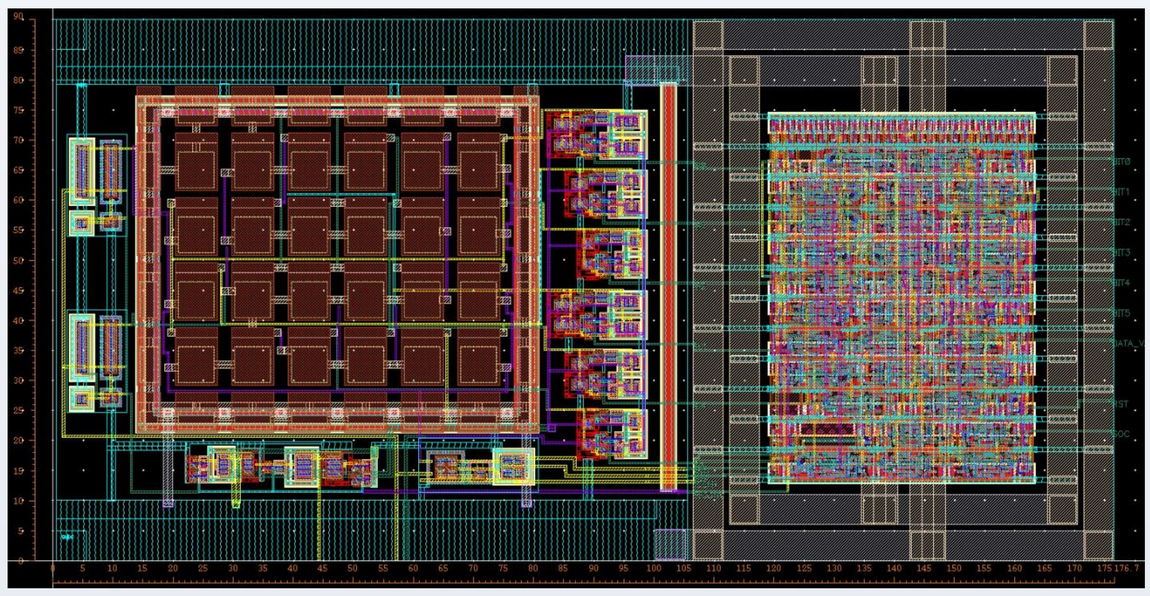
The ADC has a single-ended input and asynchronous internal clock, being equal to 500 MHz. The clock is generated by a built-in ring oscillator. That allows to achieve a 40 Ms/s rate of ADC.



ADC architecture

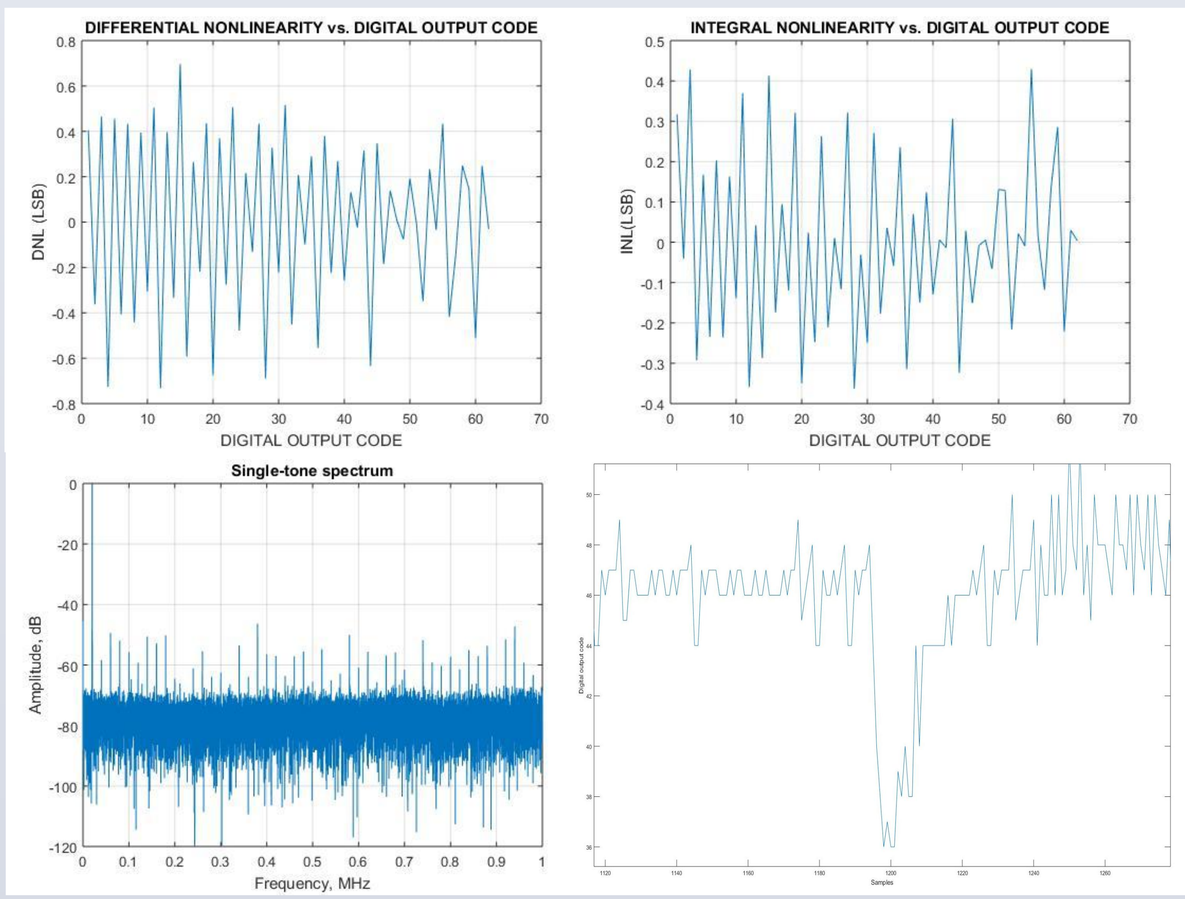
Layout

The ADC layout occupies an area of 0.0162 mm^2. The layout height of 90 um is selected to fit the analog chain geometry of the multichannel ASIC structure.



Measurement results

The ASIC has been manufactured in the 180 nm CMOS UMC MMRF process via Europractice. For experimental study the samples were packaged into CPGA 120 and a test board with the corresponding socket was developed. The first experimental results have been received for the ASIC at lab conditions. They confirmed the functionality of the ADC. The experimental result has shown INL=0.45 LSB, DNL=0.7 LSB for static requirements and ENOB=5.3 at 1 Ms/s. Power consumption is equal to 1.5 mW.



Specifications

ENOB	5.3 at 1 Ms/s
SFDR	49.86 dB
SINAD	33.97
SNR	34.21
INL	0.45 LSB
DNL	0.7 LSB
Power consumption	1.5 mW at 40 Ms/s

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