Adaption of Low Cost Safety COTS MCU For Low Level Radiation Applications in Accelerator Facilities

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Introduction

Automotive Texas Instruments CortexR4F/R5F TMS570 is a low cost alternative MCU for radiation environments.

Previous work: Scrubbing mechanisms for internal SRAM using the ECC module.

Aim: MCU must run EPICS IOC or similar SCADA.

Problem: Small amount of flash program memory.

Approach: Execute program from an external SDRAM memory with error mitigation.

TMS570 Safety Features

- SEC-DED ECC in internal SRAM (up to 512KB) and in Flash program memory (up to 4MB)
- CRC module for peripheral memories
- Lockstep dual core mechanism

Other Features

- Direct Memory Access (DMA)
- External Memory Interface (EMIF)

CRC Module

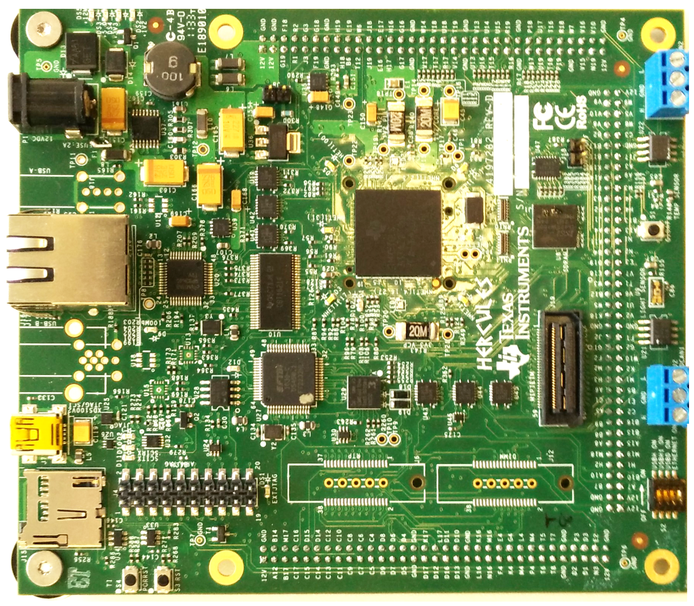
- Signature is computed with original data and stored in a memory location
- CRC module calculates again signature using DMA for data reading and compares it with the signature stored previously
- Procedure loops, if faulty data is found, the faulty sector's address is stored in a CRC module register

DMA Module

- Can be Software or Hardware triggered
- Data can be copied with different structures with no CPU usage

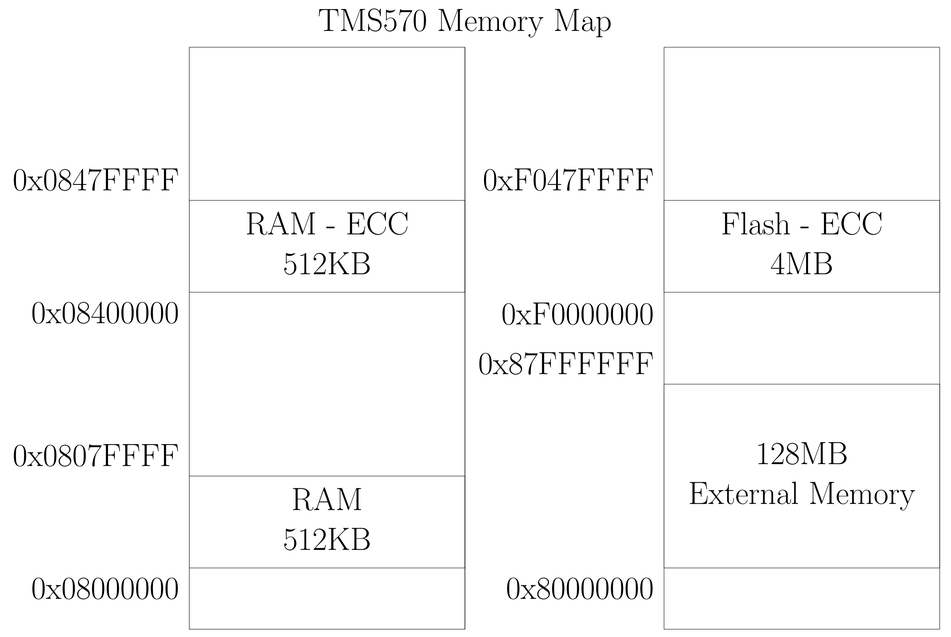
EPICS IOC

- Tested in the TMS570 CortexR4F over RTEMS Beta BSP
- TI TMS570 Hardware Development Kit used for tests shown below



External Memory Program Execution

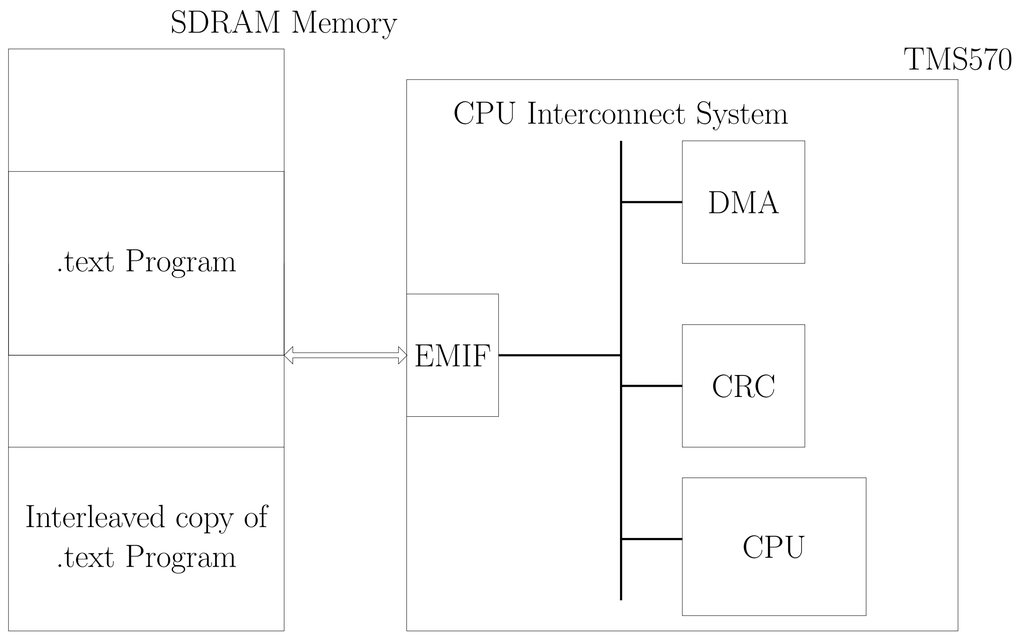
For programs > 4MB, an external memory is necessary



The problem with external compatible memories is, they barely have mechanisms against SEE's.

Concept

1. Program the DMA to copy .text program data in a different order of 8 words (interleaved) to an unused memory location
2. Signatures of the original data and interleaved copy are computed
3. Interleaving helps to detect burst errors due to a large memory affected area
4. In the case the CRC detects an error, the original data can be retrieved from the interleaved copy



Program variables correctness is important too

Aim: Heap and the stack should be protected too with error mitigation.

Problem: A rather time- spaced CRC will not help to protect them.

Approach: Use open source RTEMS for debugging and modifying Operative System. Introduce CRC routines in the malloc or create task mechanism. Optionally make an interleaved copy of the heap and stack to recover variable data at clue points of execution.

Conclusions

As the necessity of general small control boards increases in physics experiments, low price COTS with resilience mechanisms shall be considered. A COTS MCU is proposed to be used for low radiation environments where Even Upsets are prone to occur. The MCU has a lockstep mechanism which executes the same instruction in two cores and compare the result, issuing an error if the results are not equal. A scrubbing algorithm for the internal SRAM memory was already implemented in former works by reading from and writing to memory while using the MCU SEC-DED ECC error detection mechanism. Nevertheless there is still a problem to overcome, which is the small amount of program memory available. The TMS570 CortexR4F was already tested, as a part for this work, running an EPICS IOC from a larger external memory. EPICS IOC is an openly used firmware to control parameters in physics experiments facilities. Furthermore this work focuses on assuring the integrity of external memories for reliable large program execution, which is not possible in the ECC Flash due to its limited 4MB capacity. By using modules included in the MCU it is shown that is possible to back up the information, detect errors and recover from them in external memories using minimal CPU resources while running normally. In future work it will be assumed that several units of Detector Control Boards are used in an experiment. Using more than one board leads us to consider backing parts of the information in several boards, such that if one fails, its tasks can be retrieved or they can be executed by a different board.