System-Level Considerations of the Front-End Readout ASIC in the CBM Experiment from the Power Supply Perspective

Krzysztof KASIŃSKI[1], Piotr KOCZOŃ[2], Samuel AYET[2], Sven LÖCHNER[2], Christian J. SCHMIDT[2]

kasinski@agh.edu.pl P.Koczon@gsi.de

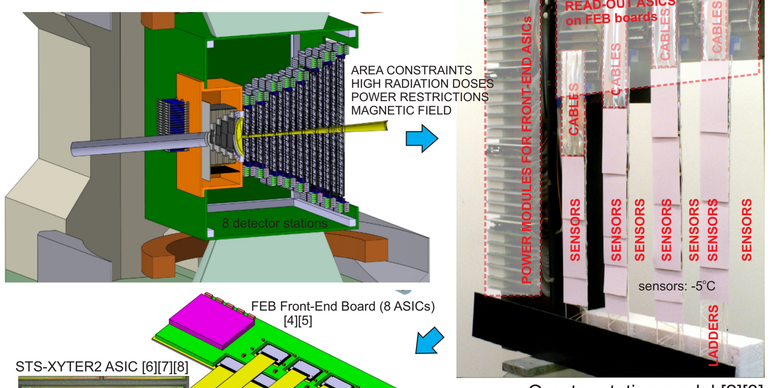
[1] AGH University of Science and Technology Department of Measurement and Electronics, Poland

[2] GSI Helmholtzzentrum für Schwerionenforschung / FAIR - center - www.gsi.de / www.fair-center.eu

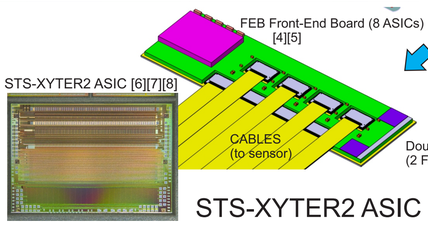
Introduction

New fixed target experiments using high intensity beams up to 10 AGeV from SIS100 synchrotron presently being constructed at FAIR/GSI center are under preparation. Most of the readout electronics and power supplies are expected to suffer very high flux of nuclear reaction products and have to be radiation hard up to 3 MRad and sustain up to 10^14/cm^2 of 1 MeV neutron equivalent in their life time. Moreover, the minimum ionising particles under investigation leave very little signals in the sensors therefore very low noise level amplitude measurements are required by the front-end electronics for effective tracking. Sensor and interconnecting microcable capacitance and series resistance in conjunction with intrinsic noise of the charge sensitive amplifier are dominant noise sources in the system, however, single-ended architecture of the amplifiers used in the charge processing channels implies potential problem with noise contribution from the power supply sources. Strict system-level constraints leave very little freedom in selecting power supply structure optimal with respect to: power efficiency, power density on modules and cooling capabilities, but also noise injection to the front-end via the power supply lines. Noise level simulations of front end ASIC´s (STS/MUCH-XYTER2) and measurements´ results of power supply and conditioning electronics (selected DC/DC converter and LDO regulators) will be presented together with power supply structure in the Silicon Tracking System.

STS Silicon Tracking System DETECTOR [1]

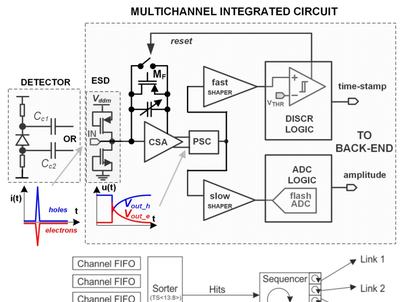


Quarter-station model [2][3]



Double-sided sensors
(2 FEBs per sensor > ground potentials differ by 250 V)

STS-XYTER2 ASIC



Brief ASIC summary:

- 128 channels (time & amplitude measurement)
- CSA + 2 SHAPERS + 5-bit ADC + timing latch
- single-ended architecture (low PSRR)
- back-end with data bandwidth 9.41 - 47 MHit/s
- compatibility with GBTx-based read-out [9] via dedicated STS-HCTSP protocol [10]
- UMC 180 nm CMOS MM/RF process
- tab-bonded to cable, wire-bonded to PCB
- 10 mm x 7.8 mm die
- mixed-mode design:
  low-noise AFE & 320 MHz back-end
- Power domains:
  VDDM: 1.2 V low-noise analog
  VDD: 1.8 V low-noise analog
  VDDC: 1.8 V discriminator supply
  VDD_ADC: 1.8 V ADC supply
  VDD_DIG: 1.8 V back-end power supply
  VDD_LVDS: 1.8 V differential tx/rx power supply

NEED FOR:

FEASIBLE POWER BUDGET

RELIABLE, RAD-HARD & LOW-NOISE POWER SUPPLY

NOISE-OPTIMIZED LAYOUT OF PCB

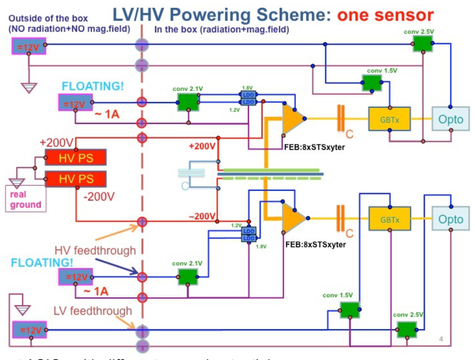
POWER-SUPPLY & ASIC CO-DESIGN

EFFECTIVE PDN (POWER DELIVERY NETWORK) ON ASIC

SYSTEM POWERING SCHEME [12][13]

Key constraints/assumptions:

- sensors are biased with up to 400 V
- necessity of low-noise power supply for the ASICs (at least 2 separate voltages)
- readout ASIC's inputs are AC-coupled with sensor's strips
  (but voltage across C needs to be small)



- Two groups of readout ASICs with different ground potentials.
- AC-coupled data links are used.
- Data concentrators (GBTx boards and DPB FPGA boards) use real ground.
- DC/DC + LDO structure is preferable for ASIC power supply (low-noise)

POWER BUDGET

- STS-XYTER2 uses UMC 180 nm CMOS process with nominal 1.8 V power supply,
- Input transistor is the most power consuming device in the ASIC,
- Input transistor can have separate (lower) power supply potential - also preferable from the noise coupling POV.
- Lower voltage = lower power / ASIC -> BUT this is just pushing the problem further...
- Selection of the potential option can be optimized (for optimal POWER DELIVERY)
- Optimization for largest VDDM current at lowest total Power Consumption in the system
- ASSUMPTION: Power is delivered by 2 DC-DC converters + Individual LDOs
- DC/DC maximum output current: 4 A (based on FEASTMP)
- DC/DC maximum effectiveness is below ~2-3 A (based on FEASTMP)

▪ Two cases groups: A (lower VDDM potential: 1.2V), B (VDDM same as others)
▪ Cases 1 through 4: Input MOS current.

VDDM potential current / power (1.2V or 1.8V) — Auxiliary ASIC circuits current consumption (1.8V)

Case	VDDM voltage (V)	Input MOS current (A)	Aux. VDDM consumption (A)	I_vddm chip (A)	P_vddm at chip (W)	VDDA/VDDC/VDDADC/VDDDD voltages (V)	I_vdda chip (A)	I_vddc chip (A)	I_vddadc chip (A)	I_vddd chip (A)	I_vddlvds chip (A)
A1	1,2	0,001	0,0005	0,195	0,234	1,8	0,1	0,0003	0,15	0,1	0,03
A2	1,2	0,002	0,0005	0,325	0,39	1,8	0,1	0,0003	0,15	0,1	0,03
A3	1,2	0,0032	0,0005	0,481	0,5772	1,8	0,1	0,0003	0,15	0,1	0,03
A4	1,2	0,004	0,0005	0,585	0,702	1,8	0,1	0,0003	0,15	0,1	0,03
B1	1,8	0,001	0,0005	0,195	0,351	1,8	0,1	0,0003	0,15	0,1	0,03
B2	1,8	0,002	0,0005	0,325	0,585	1,8	0,1	0,0003	0,15	0,1	0,03
B3	1,8	0,0032	0,0005	0,481	0,8658	1,8	0,1	0,0003	0,15	0,1	0,03
B4	1,8	0,004	0,0005	0,585	1,053	1,8	0,1	0,0003	0,15	0,1	0,03

Input MOS current sweep

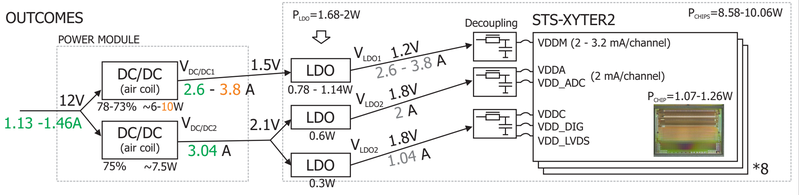
Analog Comparator ADC Back-end Tx/Rx

Currents Powers ASICs Power (FEB PCB) LDO input voltages LDO input voltages

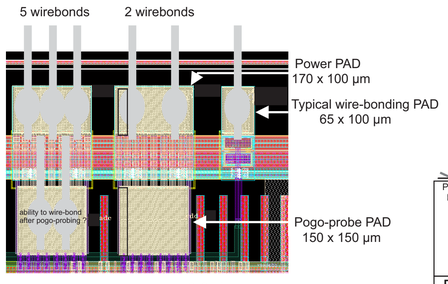
I_analog chip (A)	I_digital chip (A)	P_analog chip (W)	P_digital chip (W)	P all 8 chips (W)	V at LDO1 (V)	V at LDO2 (V)	I at LDOs type 1 (A)	I at LDOs type 2 (A)	P at LDO type 1 (W)	P at LDO type 2 (W)	Ptotal FEB (W)	
0,25	0,1303	0,45	0,23454	7,34832	1,5	2,1	1,56	3,0424	0,468	0,91272	8,72904	
0,25	0,1303	0,45	0,23454	8,59632	1,5	2,1	2,6	3,0424	0,78	0,91272	10,28904	Design Target
0,25	0,1303	0,45	0,23454	10,09392	1,5	2,1	3,848	3,0424	1,1544	0,91272	12,16104	
0,25	0,1303	0,45	0,23454	11,09232	1,5	2,1	4,68	3,0424	1,404	0,91272	13,40904	
0,25	0,1303	0,45	0,23454	8,28432	2,1	2,1	1,56	3,0424	0,468	0,91272	9,66504	11%
0,25	0,1303	0,45	0,23454	10,15632	2,1	2,1	2,6	3,0424	0,78	0,91272	11,84904	15%
0,25	0,1303	0,45	0,23454	12,40272	2,1	2,1	3,848	3,0424	1,1544	0,91272	14,46984	19%
0,25	0,1303	0,45	0,23454	13,90032	2,1	2,1	4,68	3,0424	1,404	0,91272	16,21704	21%

Analog Digital

OUTCOMES

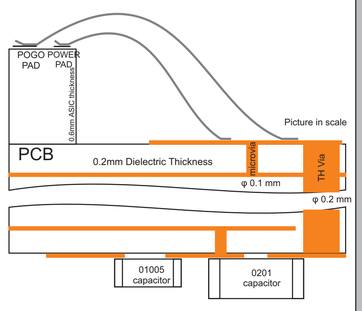


ASIC POWER PADS



NUMBER OF WIREBONDS	ESR (Ω)	ESL (nH)	IR drop @100mA (mV)
1	0.8	1	80
2	0.4	0.5	40
5	0.16	0.2	16

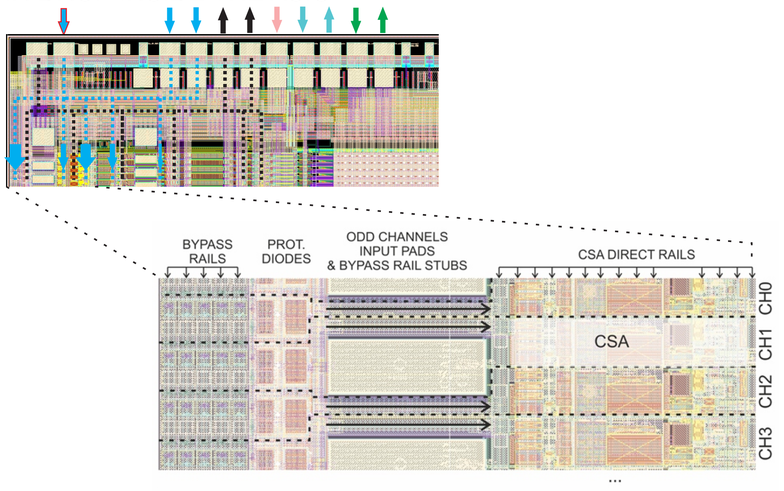
Approximate values for φ=18µm, Al, 2mm



POWER DOMAIN	VOLTAGE	CURRENT	NUMBER OF PADS	CURRENT PER PAD	IR DROP 2 bonds/PAD	IR DROP 5 bonds/PAD
VDDM	1.2 V	0.32 - 0.48 A	4-6	0.053 - 0.12 A	20 - 48 mV	8.5 - 19 mV *
VDD	1.8 V	0.1 A	2	0.05 A	20 mV	7 mV
GNDA	0 V	0.42 - 0.58 A	4-6	0.07 A - 0.145 A	28 - 58 mV	10 - 20 mV *
VDDC*	1.8 V	0.012 A	2	0.006 A	2.4 mV	0.85 mV
VDD_ADC*	1.8 V	0.15 A	2	0.075 A	30 mV	10.5 mV
VDD_DIG*	1.8 V	0.1 A	3	0.033 A	13 mV	4.6 mV
VDD_LVDS*	1.8 V	0.03 A	1	0.03 A	12 mV	4.2 mV

*return pads: same count - not mentioned *worst cases considered below

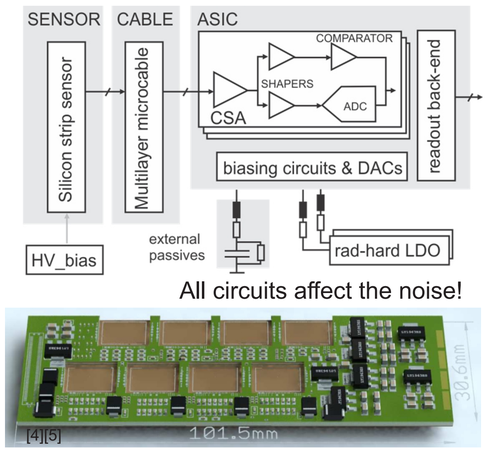
IR DROP INSIDE THE ASIC

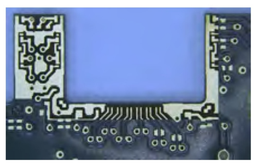


Power line	R_{unit}	ΔV_{64} for I_D=2mA
VDDM (1.2V) no bypass	10.9 mΩ	45.3 mV
VDD (1.8 V) no bypass	17.9 mΩ	**4.46 mV** @ 120 µA/channel
GNDA (0 V) no bypass	11.25 mΩ	46.8 mV
VDDM incl. bypass	4.51 mΩ	**18.7 mV**
GNDA incl. bypass	6.11 mΩ	**25.4 mV**

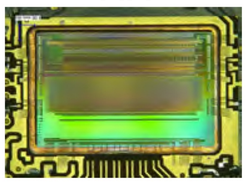
$$\Delta V_n=(1+n)/2\cdot n\cdot R_{unit}\cdot I_N$$

NEIGHBORHOOD OF READOUT ASIC

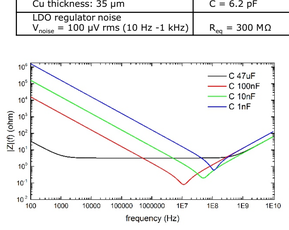




[4][5]



Component	Model parameters
1 nF X7R 6.3 V 01005 (0.4 mm × 0.2 mm)	C = 1 nF ESR = 0.6 Ω, ESL = 1 nH
10 nF X5R 6.3 V 01005 (0.4 mm × 0.2 mm)	C = 10 nF ESR = 0.2 Ω, ESL = 2 nH
100 nF X5R 6.3 V 0201 (0.6 mm × 0.3 mm)	C = 100 nF ESR = 0.08 Ω, ESL = 3 nH
47 µF 2.5 V Tantalum 2.05 mm x 1.35 mm TAJP476M002RNJ	C = 47000 nF ESR = 3.2 Ω ESL = 2.4 nH
Al Wire-bond Diameter: 18 µm, Length: 2 mm	L= 1 nH R = 0.8 Ω
Via to power plane diameter: 0.15 mm, FR4 laminate thickness: 1.55 mm	L = 1.5 nH R = 2.1 mΩ C = 1.21 pF
Simplified PCB power trace Length: 50 mm, Width: 20 mil Cu thickness: 35 µm	L = 13 nH R = 0.2 Ω C = 6.2 pF
LDO regulator noise V_{noise} = 100 µV rms (10 Hz -1 kHz)	R_{eq} = 300 MΩ



Physical restrictions limit freedom in PDN design on the PCB:
- very tight area around the ASICs
- very high density of signals
- thermal connection to heatsink in PCB under the chip is required (milled opening prevents routing)

RESTRICTED: ROUTING, VIAS, DECOUPLING
(e.g. just 1 via per power group)

Need for simulation framework for estimating the noise contribution from:
- detector
- cable
- Power Distribution Network

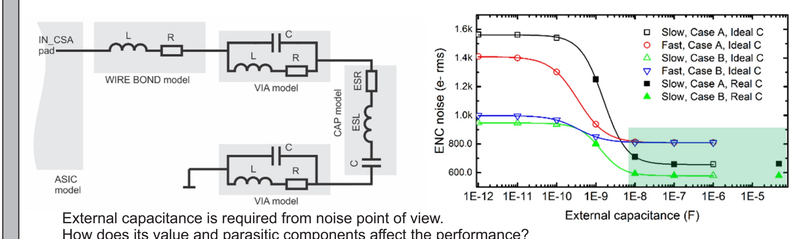
Early stage analysis:

Source	Contribution to the ENC of the system Case A	Case B
Sensor series resistance (main channel)	16.89 %	48.33 %
CSA input transistor (main channel)	20.06 %	15.16 %
CSA cascode branch transistors (main channel)	10.57 %	10.9 %
VDDM supply LDO (100uV rms, 1kHz BW)	34.4 %	6.07 %
CSA current source NMOS transistor (main channel)	7.29 %	5.48 %
Sensor series resistance (neighbors)	< 0.2 %	4.84 %
CSA input transistors (neighbor channels)	< 0.2 %	0.98 %
CSA feedback transistor (main channel)	0.41 %	0.52 %
Detector cable resistance (main channel)	3.71 %	0.47 %
Other sources	6.27 %	7.25%

Case A (2.2 cm sensor, 50 cm cable), Case B (18.6 cm sensor, 5 cm cable).
Folded cascode, I_B=1mA

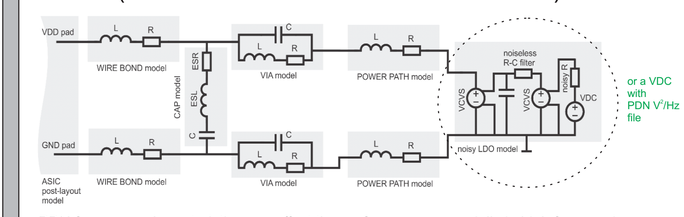
Outcomes:
- sensor series resistance needs to be minimized (changes made to sensor design)
- cable resistance vs. capacitance ratio can be optimized (traces' width & dielectric selection)
- attention to the LDO noise power density
- careful design of the PCB & selection of decoupling capacitors & wire-bonds

EXTERNAL FILTER FOR CURRENT REFERENCE

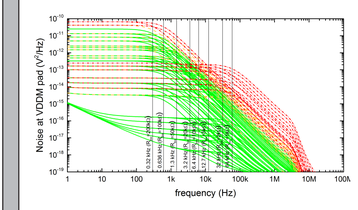


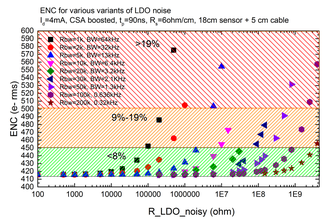
External capacitance is required from noise point of view.
How does its value and parasitic components affect the performance?

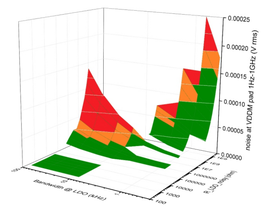
PDN (POWER DISTRIBUTION NETWORK)



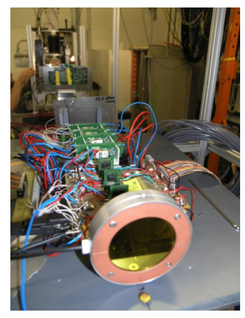
PDN frequency characteristics can affect the performance, especially in high frequencies.
How many wire-bonds shall be used/
How many vias? What type and how many decoupling capacitance will be enough?

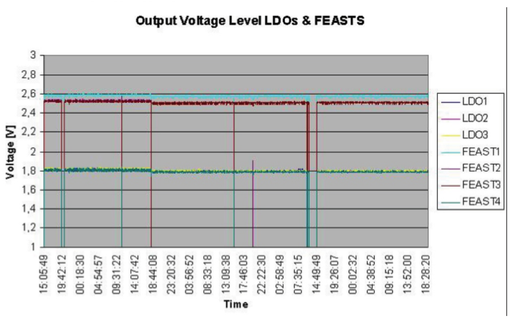






DC-DC Converter Selection [14][15][16]





Tests with 3 GeV protons at Research Center Jülich's sychrotron facility COSY.
DC-DC converters selected for evaluation:

- VICORS P048T24AL → failed at 50 mT (built-in inductance)
- B048F012T30 → abandoned (100krad by manufacturer)
- ISL75051SRH → failure after 0.55 10^{12} p/cm²
- LTC3605 (10 samples) → failure below 4.3 10^{9} p/cm²
- LTC3610 (3 samples) → failure below 4.3 10^{9} p/cm²
- LM259S (4 samples) → survived 4 10^{12} p/cm² →
- FEASTMP (4 samples) → 92% downto 80% at 0.7 T
- LTM4619 / LT3610 ? → 97% downto 84% at 0.7 T
- LM2596 → 96% downto 93% at 0.7 T
- Yutaka Electric YSD812

No fast transients were observed.

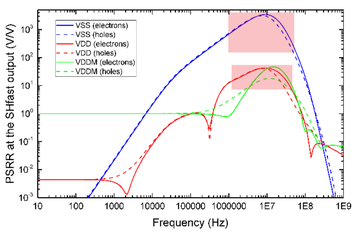
FEASTMP [18]
- V_{in} 5V - 12V
- 4A load capability (10W)
- TID >200Mrad (Si)
- Magnetic field > 4 T

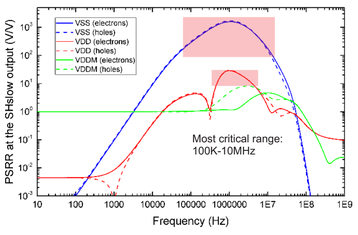
LDO - Linear Voltage Regulators

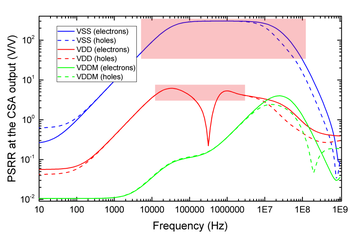
Need for low-noise, RAD-hard LDOs capable of feeding the ASICs on FEB.

▪ Single-ended architectures (noise & power restrictions).
▪ CSA in NMOS-based (more susceptible to GND variations).
▪ Shapers are PMOS-based (more susceptible to VDDM variations).
PSRR analysis reveals weak points of the circuits.

VSS results are pessimistic (placement of simulation AC source).
Sensor ground has good connection with readout electronics
(tab-bonded cable directly to ASIC - little current flow).





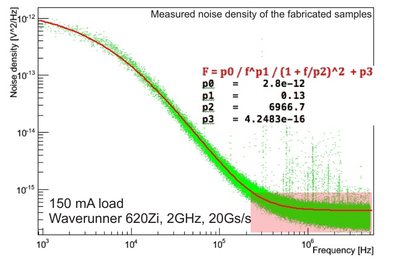


LDO noise spectrum is very important.
PDN can effectively reduce the noise.
Difficulty: correct model of the PDN.

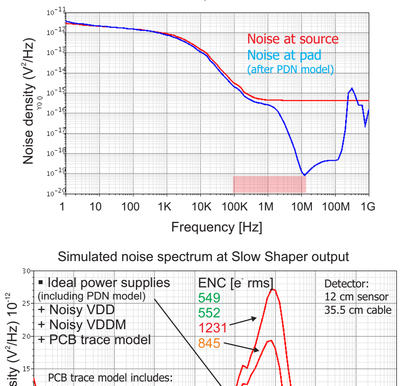
- full-custom design in India (H.S. Jatana, D. Sehgal, V. Aneesh, A. Koul, Semi-Conductor Laboratory Department of Space, Government of India)
- ASIC - LDO co-design for noise reduction within the worst PSRR regions of the Front-End electronics

Nominal V_{IN}= 2.2V - 3.6 V
Nominal V_{OUT}= 1.8V
Full load current = 150 mA
Temperature range: -40°C; +125°C
Dropout voltage @ full load: < 0.4V

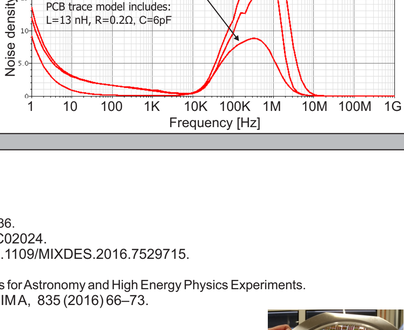
PROTOTYPE LDO LVR noise density



Simulated noise spectrum at Power Line



Simulated noise spectrum at Slow Shaper output



Acknowledgement

This work was supported in part by GSI Helmholtzzentrum für Schwerionenforschung and by Ministry of Science and Higher Education,

[1] J. Heuser et al., **Silicon Tracking System (STS): technical design report for the CBM**, Germany (2013).
[2] P. Koczoń, J. Kunkel, D. Soyk, C. J. Schmidt, **„A mechanical model of an STS station for the study of cable routing"**, CBM Progress Report 2013, GSI (2014), p. 48.
[3] J. Kunkel, S. Belogurov, J. Sanchez Rosado, **„Status of the CBM STS CAD design"**, CBM Progress Report 2014, GSI (2015), p. 53.
[4] V. Kleipa, C. Simons, D. Soyk, J. Carpenter, C. J. Schmidt, **„A front-end electronics test board for the CBM Silicon Tracking System"**, CBM Progress Report 2014, GSI (2015), p. 39.
[5] V. Kleipa, C. J. Schmidt, C. Simon, D. Soyk, **„A front-end electronics boards to test the assembly procedure of modules for the CBM Silicon Tracking System"**, CBM Progress Report 2013, GSI (2014), p. 36.
[6] K. Kasinski, R. Kleczek, R. Szczygiel, **Front-end readout electronics considerations for Silicon Tracking System and Muon Chamber**, J. Instrum. 11 (2016). doi:10.1088/1748-0221/11/02/C02024.
[7] K. Kasinski, R. Kleczek, **A flexible, low-noise charge-sensitive amplifier for particle tracking application**, 2016 Mix. - 23rd Int. Conf. Mix. Des. Integr. Circuits Syst., 2016: pp. 124–129. doi:10.1109/MIXDES.2016.7529715.
[8] K. Kasinski, R. Kleczek, R. Szczygiel, P. Otfinowski, C. J. Schmidt, **„STS-XYTER2, a prototype detector readout chip for the CBM-STS and -MUCH"**, GSI Scientific Report 2015, GSI (2016), p. 7.
[9] J. Lehnert, **„The GBT based readout concept for the Silicon Tracking System of the CBM experiment"**, Proc. Wilga 2015 - XXXVI-th IEEE-SPIE Joint Symposium on Photonics, Web Engineering, Electronics for Astronomy and High Energy Physics Experiments.
[10] K. Kasinski, R. Szczygiel, W. Zabolotny, J. Lehnert, C. J. Schmidt, W.F.J. Müller, **A protocol for hit and control synchronous transfer for the front-end electronics at the CBM experiment,** NIM A, 835 (2016) 66–73.
[12] C. J. Schmidt, P. Koczoń, **„Low and High voltage powering concept for the CBM Silicon Tracking System"**, CBM Progress Report 2014, GSI (2015), p. 43.
[13] P. Koczoń, B. Ernst, C. J. Schmidt, **„Low and high voltage power supply for STS detector electronics"**, CBM Progress Report 2013, GSI (2014), p. 37.
[14] S. Loechner, P. Koczoń, A. Rost, **„Radiation Hardness Tests of Electronic Components for CBM-STS low voltage power supply"**, GSI Scientific Report 2015, GSI (2016), p. 11.
[15] S. Loechner, P. Koczoń, A. Rost, **„Radiation hardness tests on electronic components for low voltage power supply of the CBM Silicon Tracking System"**, CBM Progress Report 2014, GSI (2015), p. 42.
[16] S. Loechner, J. Fruehauf, H. Graf, J. Hoffmann, P. Koczon, S. Manz, M. Witthaus, **„CBM proton beam test for electronic components"**, CBM Progress Report 2013, GSI (2014), p. 94.
[17] S. Loechner, P. Koczoń, **„A monitoring system for radiation hardness tests of electronic components for future FAIR experiments"**, CBM Progress Report 2014, GSI (2015), p. 10.
[18] http://project-dcdc.web.cern.ch/project-dcdc/Default.html -> **FEASTMP Documentation**
[19] C. Rivetta, F. Arteche, F. Szoncso, **„Noise Immunity Analysis of the Forward Hadron Calorimeter Front-end Electronics"** - CERN
[20] B. Allongue, J. Elias, P. Fontaine, S. Lusin, C. Rivetta, P. Robl, G. Stefanini, F. Szoncso, **„Design Considerations of Low Voltage DC Power Distribution fo CMS Sub-Detectors"**,
[21] F. Arteche, C. Rivetta, „EMC Diagnosis and corrective actions for silicon strip tracker detectors", SLAC-PUB-11886 (2006).
[22] DiBene II, **„Fundamentals of Power Integrity in Computer Platforms and Systems"**, Wiley 2016.