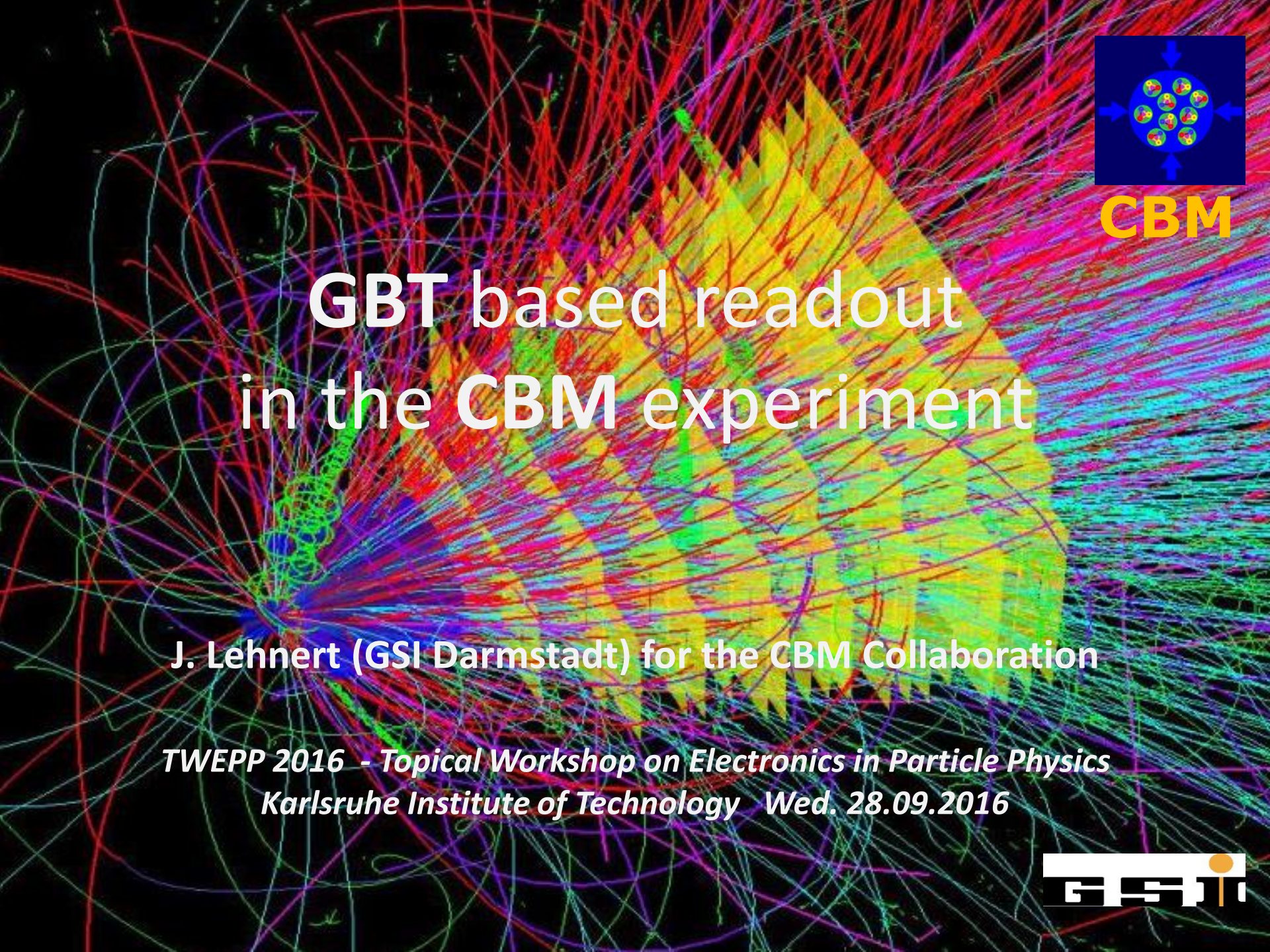
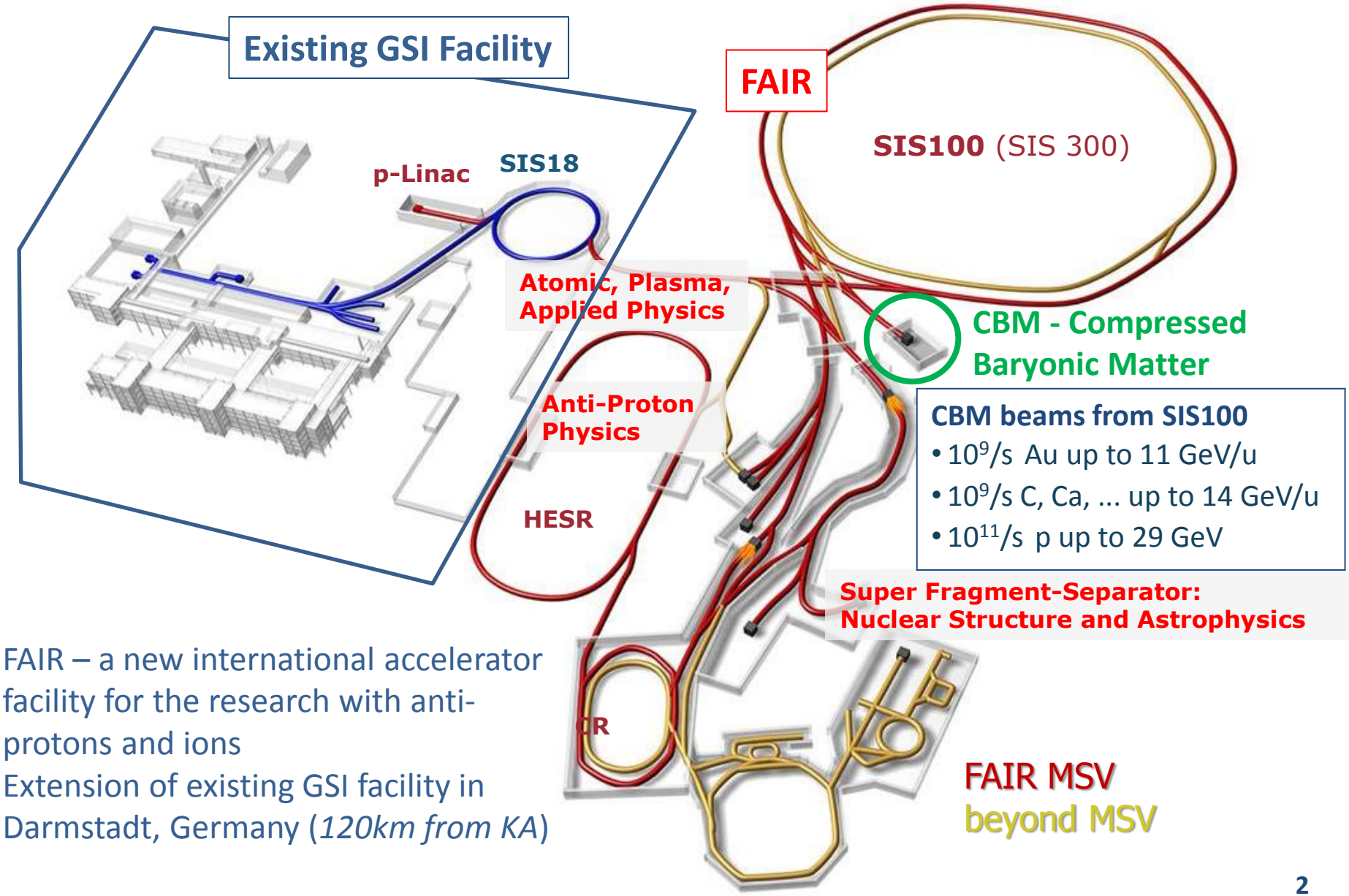


GBT based readout in the CBM experiment

J. Lehnert (GSI Darmstadt) for the CBM Collaboration

TWEPP 2016 - Topical Workshop on Electronics in Particle Physics
Karlsruhe Institute of Technology Wed. 28.09.2016

FAIR - Facility for Antiproton & Ion Research



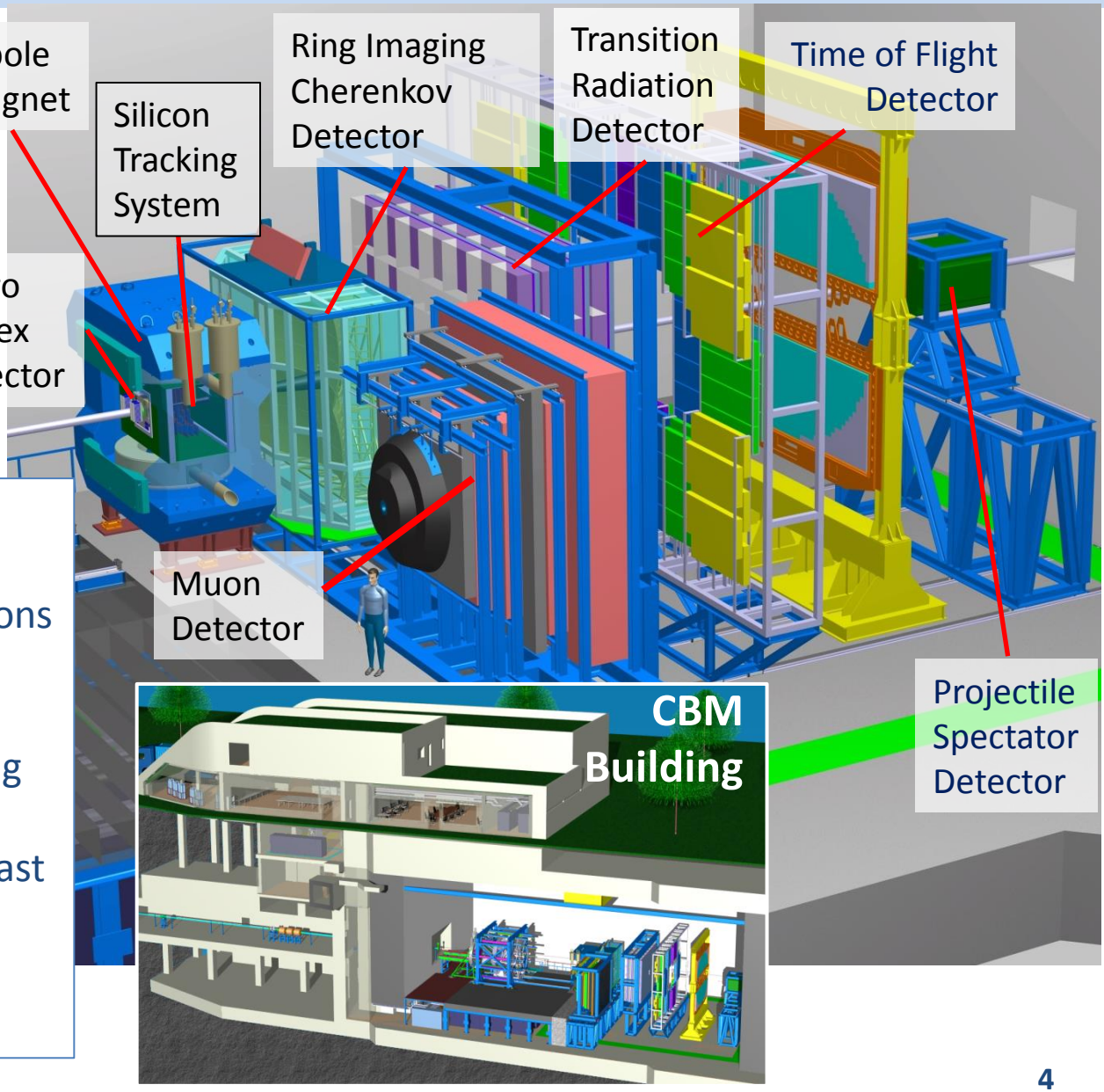
- FAIR – a new international accelerator facility for the research with anti-protons and ions
- Extension of existing GSI facility in Darmstadt, Germany (*120km from KA*)

FAIR Construction Site

GSI and construction site of FAIR, 2015

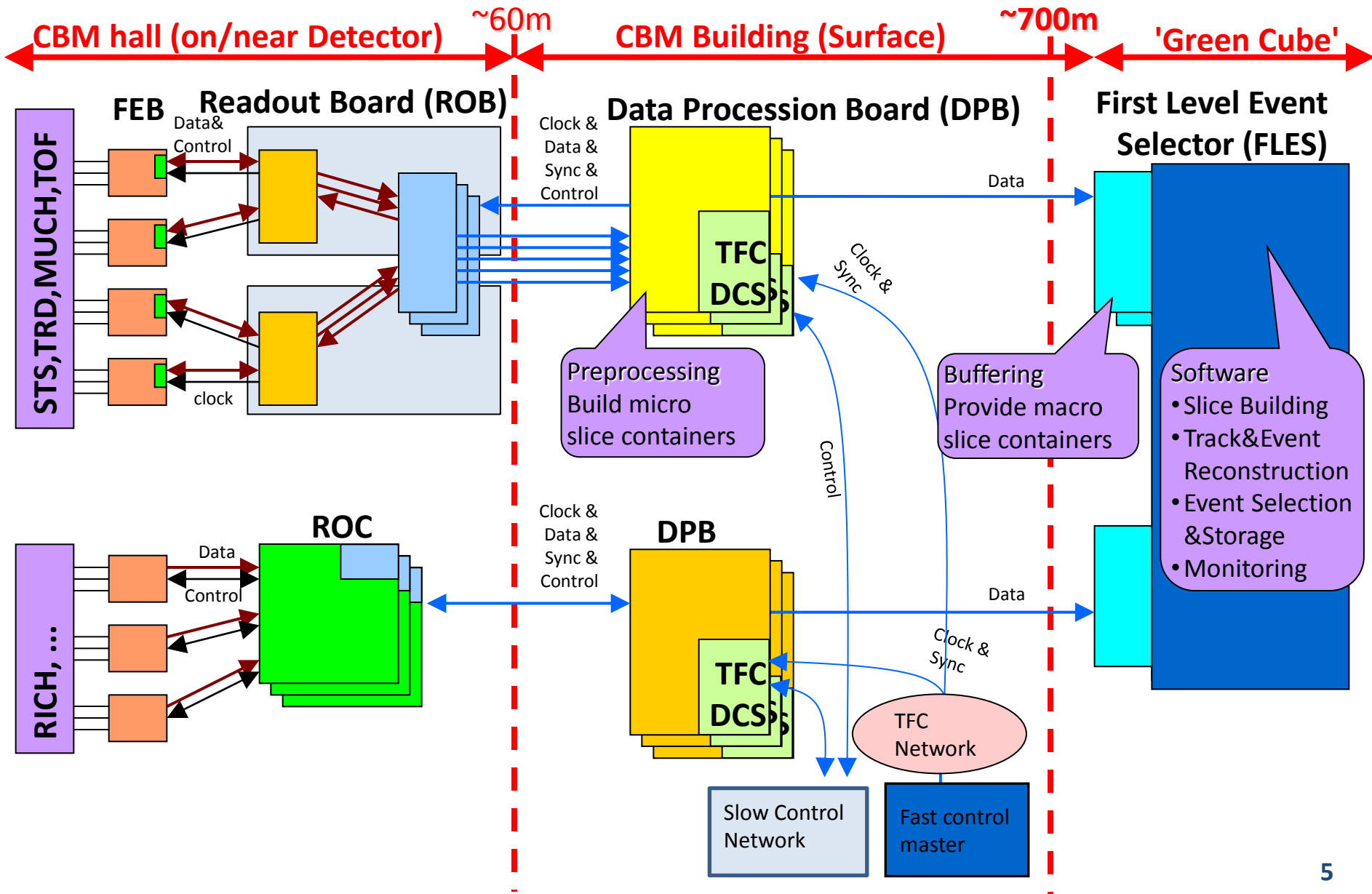
The CBM Experiment

Goal:
- exploration of the QCD phase diagram in the region of very high baryon densities
- access to rare probes

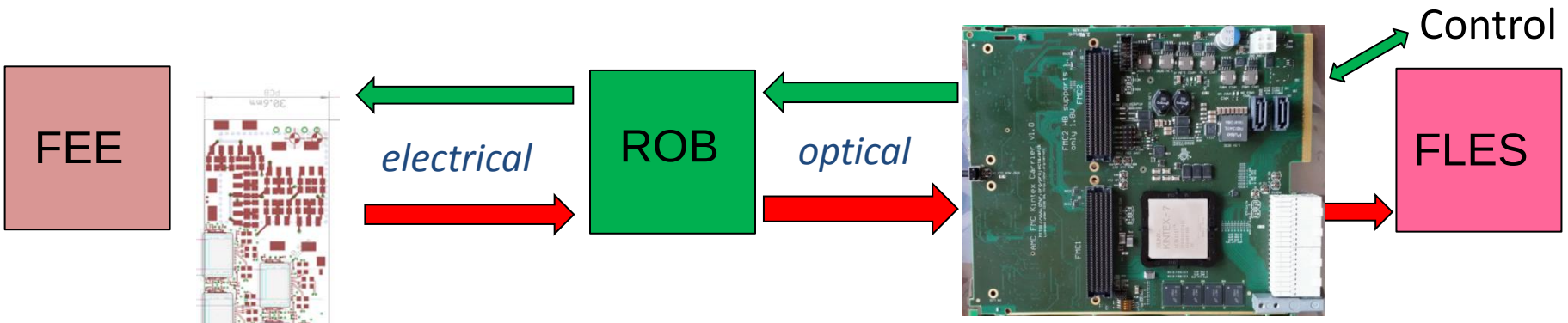


Features
- fixed target experiment
- up to 10 MHz Au+Au interactions
- self-triggering front-end electronics
- Free-streaming data processing and acquisition system
- 4D event reconstruction and fast selection algorithms
- high granularity and radiation tolerant detectors and FEE

Readout and Data Acquisition System



Building Blocks of the Readout Chain



STS FEB
Design Study

Frontend Boards (FEB)
detector specific functionality and designs of ASICs and boards

Integrated with or located close to detector elements

Readout Boards (ROB)
Similar functionality
- ***data aggregation***
  - ASICs: several ten thousand electrical links
- data readout
  - ***optical readout interface***
- FE ASIC control path
- clock distribution and synchronization

⇩

CERN GBTX / Versatile Link

DPB Prototype: AFC-K
WUT Warsaw; TWEPP2015

Data Processing Board (DPB)
CBM *common hardware platform*:
- FPGA based
  - data formatting
  - preprocessing
- timing and control interfaces
- interface to FLES (FLIB)
- in CBM building (surface)

GBT Based Readout Systems

- Why?
  - Radiation: lifetime doses up to several 100kRad
  - Magnetic field (STS)
- Who?
  - STS and MUCH: **STS/MUCH-XYTER**
  - TRD: SPADIC
  - TOF: GET4
- What?
  - Frontend ASICs with E-Link interfaces
  - ROB stage with
    - "master" GBTx with VTRX providing down- and uplink
    - 0-3 units of (2 transmitter GBTX + VTTx) depending on detector specific and local requirements in terms of readout bandwidth
  - Common DPB FPGA implementing the backends for FE ASIC and GBTX control
  - Dedicated communication protocols between DPB FPGA and FE ASICs
    - **STS-HCTSP** for STS, MUCH
- How?
  3 step procedure
  - tests and prototyping with existing hardware (VLDB)
  - **common CBM prototype: C-ROB**
  - **system specific ROB adaptations**

Poster K. Kasinski, R. Kleczek (AGH) on Wed.

Specifics of GBT Usage in CBM

- GBTX usage in readout systems based on custom frontend ASICs
  - Downlinks: FE control (both slow control and fast control)
    - Downlinks shared among multiple devices
  - Uplinks:
    - Hit data readout
      - STS in large areas rate dominated → 320MHz readout links
      - TOF dominated by number of readout channels → 80MHz readout links
    - Control responses integrated in data stream
  - no trigger distribution
  - Clock and time synchronization
    - Clock distribution to FE ASICs (phase adjustable clocks)
    - Deterministic latency allows for synchronization messages in control stream
- ROBs
  - Common prototype and detector specific ROBs
    - STS, MUCH, TRD: use widebus frames
    - ROBs with typically 3x14 and up to 7x14 uplinks
  - Custom protocols
    - Implemented for STS and MUCH in the STS/MUCH-XYTER v2 ASIC
    - reused for SPADIC2.0; to be fully adapted in rev.2.1
- Misc
  - CBM is no LHC system:
    GBTX for CBM from dedicated production batch with 40MHz (sharp) oscillator
  - AC coupled E-Links (required in case of STS)
  - GBTx emulator

Poster W. Zabolotny (WUT) on Tue.

The CBM Common Readout Board

Common CBM prototype Readout Board (C-ROB)

for prototyping of all GBT based readout chains in CBM

- **Full** GBTx, SCA and Versatile Link **functionality** required for readout and control:
  final ROBs with different form factor, connectors, cooling features, number of functional units

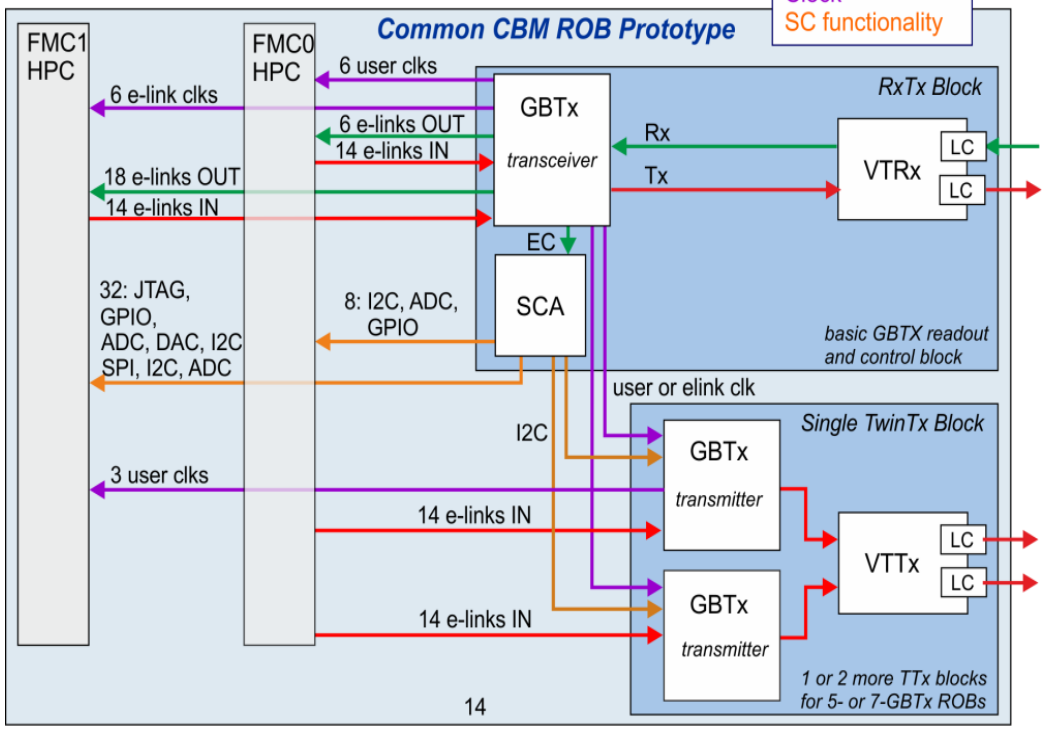
Status:
- Layout in progress
- Expected for end of 2016

- **3 GBTx ASICs**
  - connect up to 40 STS-XYTER devices at 320 Mbps: hit readout, control responses
- 1 Optical Transceiver (**VTRx**) and 1 Twin Transmitter (**VTTx**)
  - 3 optical uplinks
  - 1 optical downlink at 3.2 Gbps for control
- 1 GBT SCA
  - I2C interface for control of slave GBTx
  - additional multi purpose SCA functionality
- **FMC connectors** with **frontend connectivity**

  → flexibly connect various FEE prototypes

  FMC0 – sufficient for STS, MUCH, TRD
  - subset of downlinks, clocks; all 320MHz E-Up-Links
  - Small subset of SCA functionality

  FMC1
  - additional 80MHz E-Links (TOF); more SCA



CROB Applications

	STS	MUCH	TRD	TOF
Readout	**40 E-Links IN at 320 MHz – 1 to 5 FEB; 8 to 40 ASICs**	36 E-Links IN at 320 MHz 9 FEB with 18 ASICs	14 + 1 x (14+14) E-Links IN at 320 MHz (for prototype testing)	24 E-Links IN at 80 MHz 24 ASICs 1 GBTx only
	Widebus frame mode for uplink			
Control & Clock	**5 E-Link OUT (for up to 5 FEBs)**	9 E-Link OUT (for 9 FEBs)	6 E-Link OUT	24 E-Link OUT (for 24 ASICs)
	5 phase adjustable clocks (for up to 5 FEBs)	9 phase adjustable clocks (for 9 FEBs)	6 phase adjustable clocks	
	Alternatively E-Link clocks			
SCA	**I2C for slave GBTx control** Some ADC and GPIO channels for monitoring on ROB			**JTAG + 12 GPIO** for FPGA scrubbing
	FMC0	Uses both FMC	FMC0	Uses both FMC

Modular Test Chains

Usage of

- compatible E-Link interfaces on FMC connectors of both CROB and DPB
- firmware emulators in parallel to hardware devices
- multiple firmware flavors in DPB FPGA backend

allows flexible testing of various aspects of the readout chains:

Example: STS

Purpose	FEB	ROB	DPB Flavor
ASIC protocol testing	STS-XYTER emulator		eDPB
GBTx testing		VLDB	vldbDPB
ASIC chain dry run	STS-XYTER emulator	VLDB	vldbDPB
ASIC testing	STS-XYTER FEB-1		eDPB
ASIC chain	STS-XYTER FEB-1	VLDB	vldbDPB
ASIC functional chain	STS-XYTER FEB-1/8	C-ROB	stsDPB
Final chain	STS-XYTER FEB-8	STS-ROB-3	stsDPB

System Specific ROBs

Readout boards for the various systems

STS

TOF

TRD

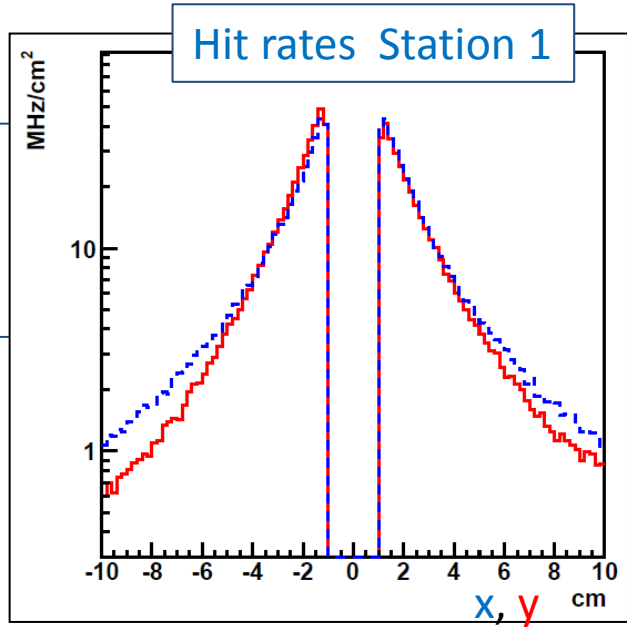
will require adjustments with respect to the C-ROB

for the final readout chains in the CBM setup…

Silicon Tracking System

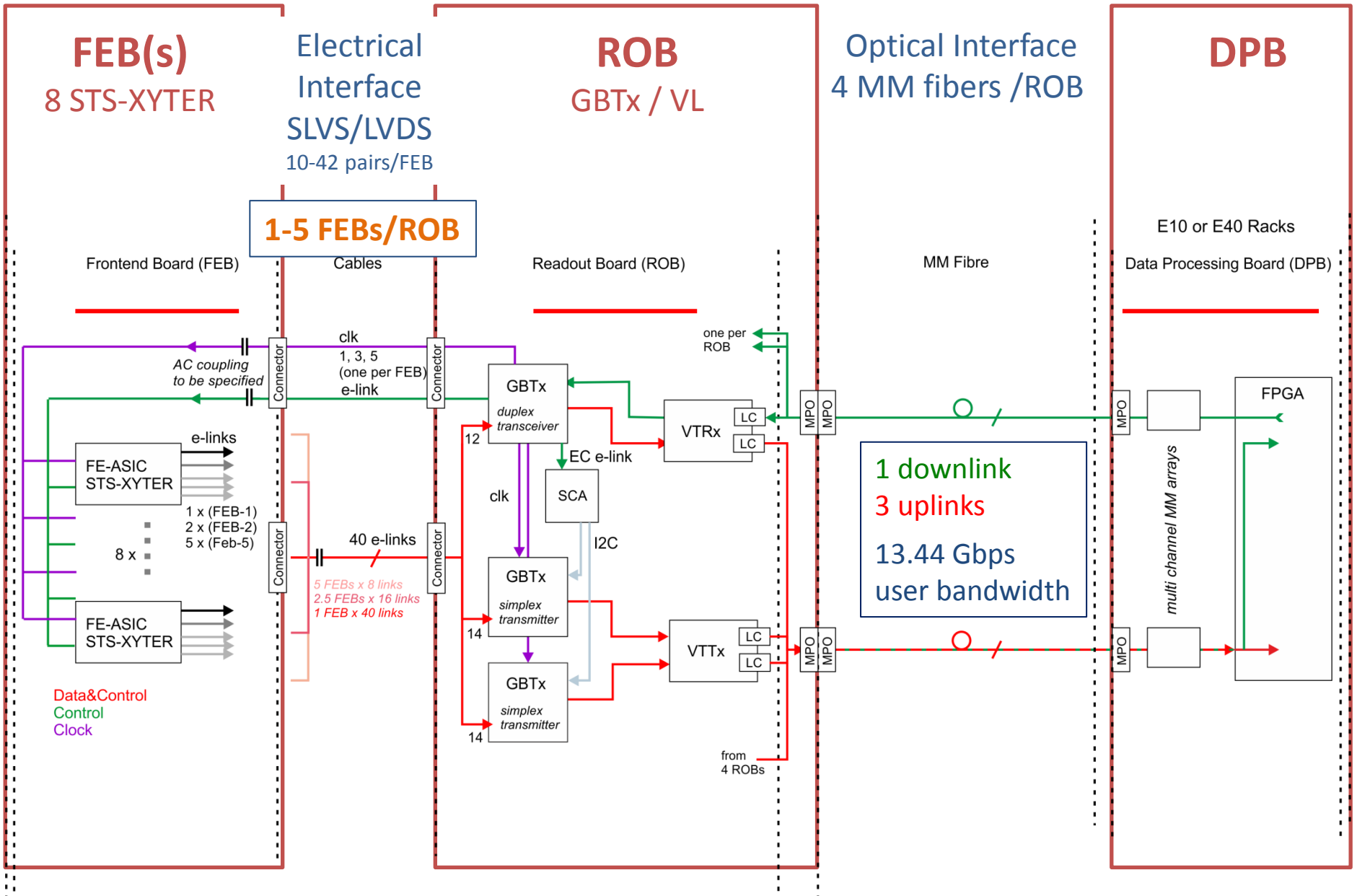
GBT use case

- connect a variable number of frontend ASICs to optical readout links
- Space efficient solution

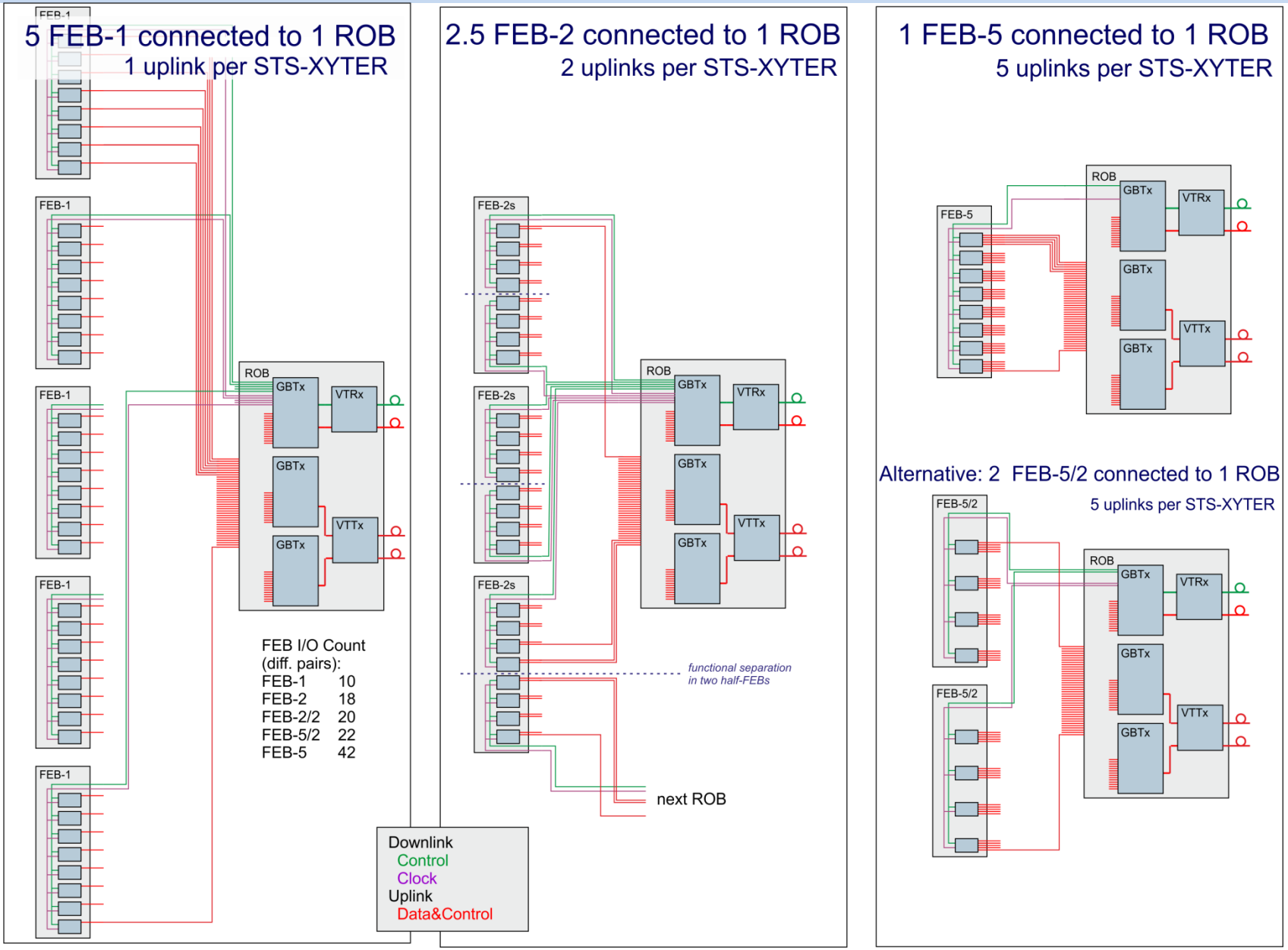


- **STS-ROB-3**, functionally equivalent to C-ROB
  - STS case was starting point for C-ROB
- FEBs with **8 STS-XYTER** ASICs
  - 1 FEB for per 1024 channel strip sensor
  - Sensors of variable length and connected FEBs at individual biasing potential → **AC coupled E-Links** to ROBs
- FEB-ROB Connectivity
  - 40 (of the 42available) E-Links IN on ROB map to 5, 2.5 or 1 FEB per ROB using **1,2 or 5 readout links (1 to 5 links configurable) per ASIC** depending on the data load
  - One control loop per FEB

STS Readout Chain

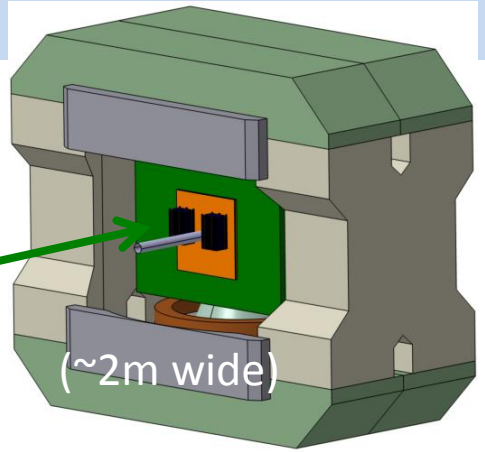


STS FEB-ROB Connectivity



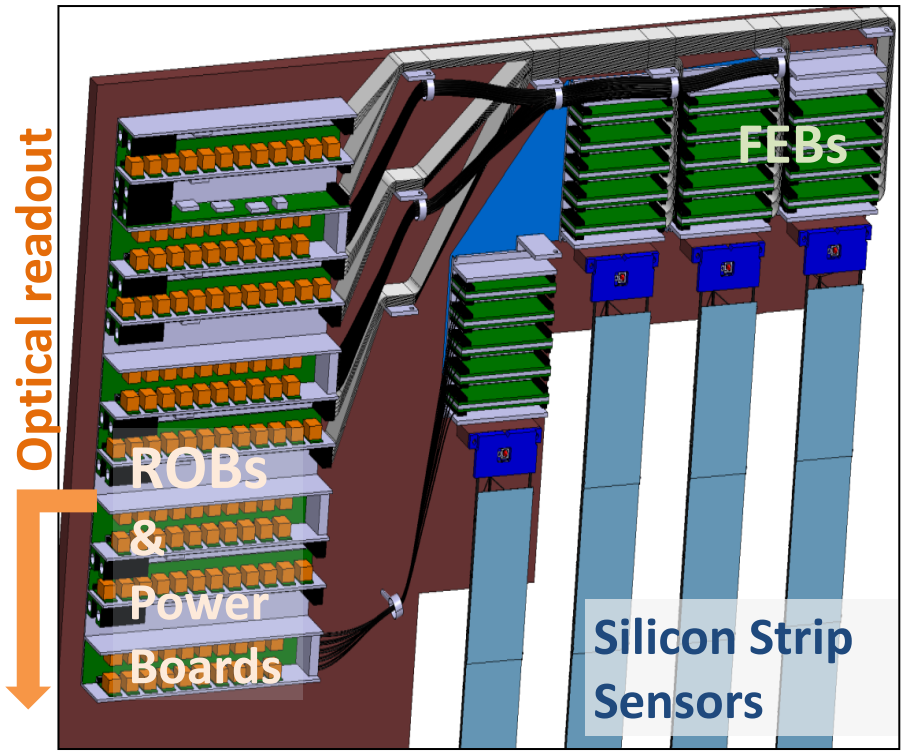
ROB Integration

Integration of STS-ROBs on sides of STS detector box



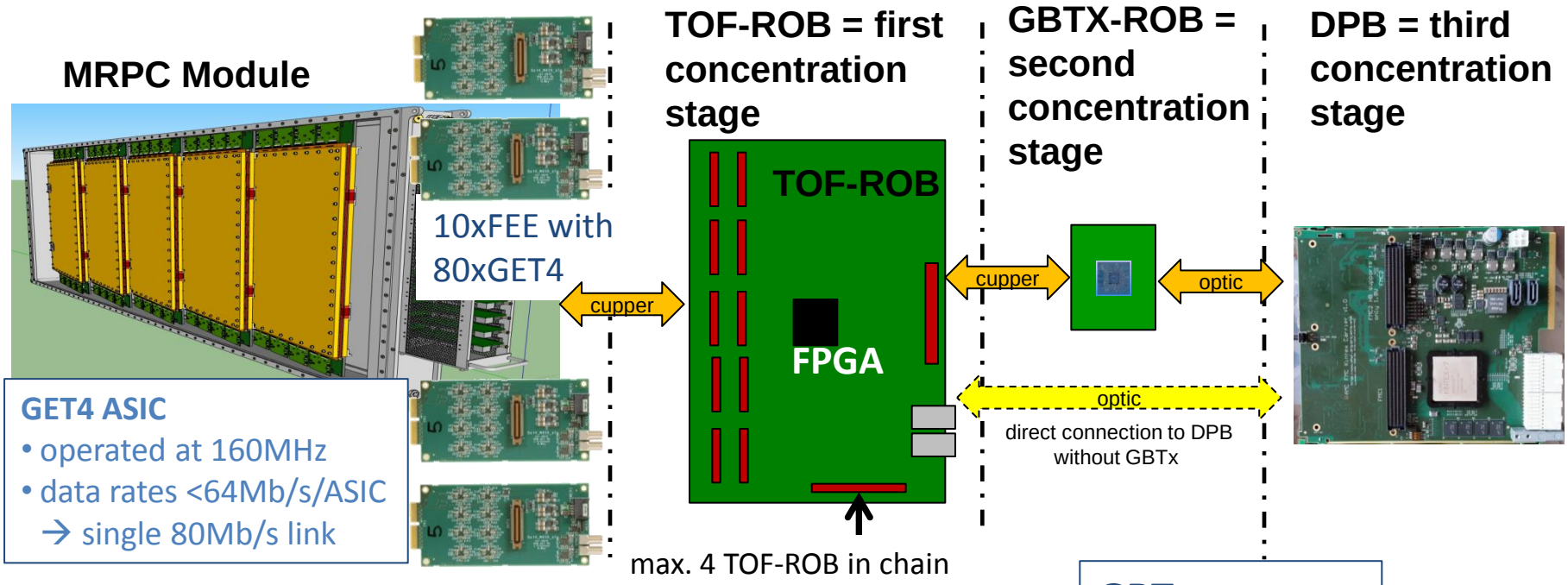
Challenges

- **Radiation**
  - up to 100krad and 5×10^{13} n_{eq}/cm^2 in ROB locations over expected total operation time with SIS100
  - higher in regions of delta electrons
- **Magnetic Field**
  - operation inside 1T dipole magnet
- **Space**
  - ROB size: approx. 83mm between side cooling plates of adjacent units
  - FEB connections: routing volumes and topology, connector size
- **Cooling**
  - sensors operated at <= -5° Celsius
- **Powering Scheme**
  - FEBs operated at individual sensor bias potentials
    → AC coupling of FEB-ROB e-links



Quarter Layer (every 2nd ladder)

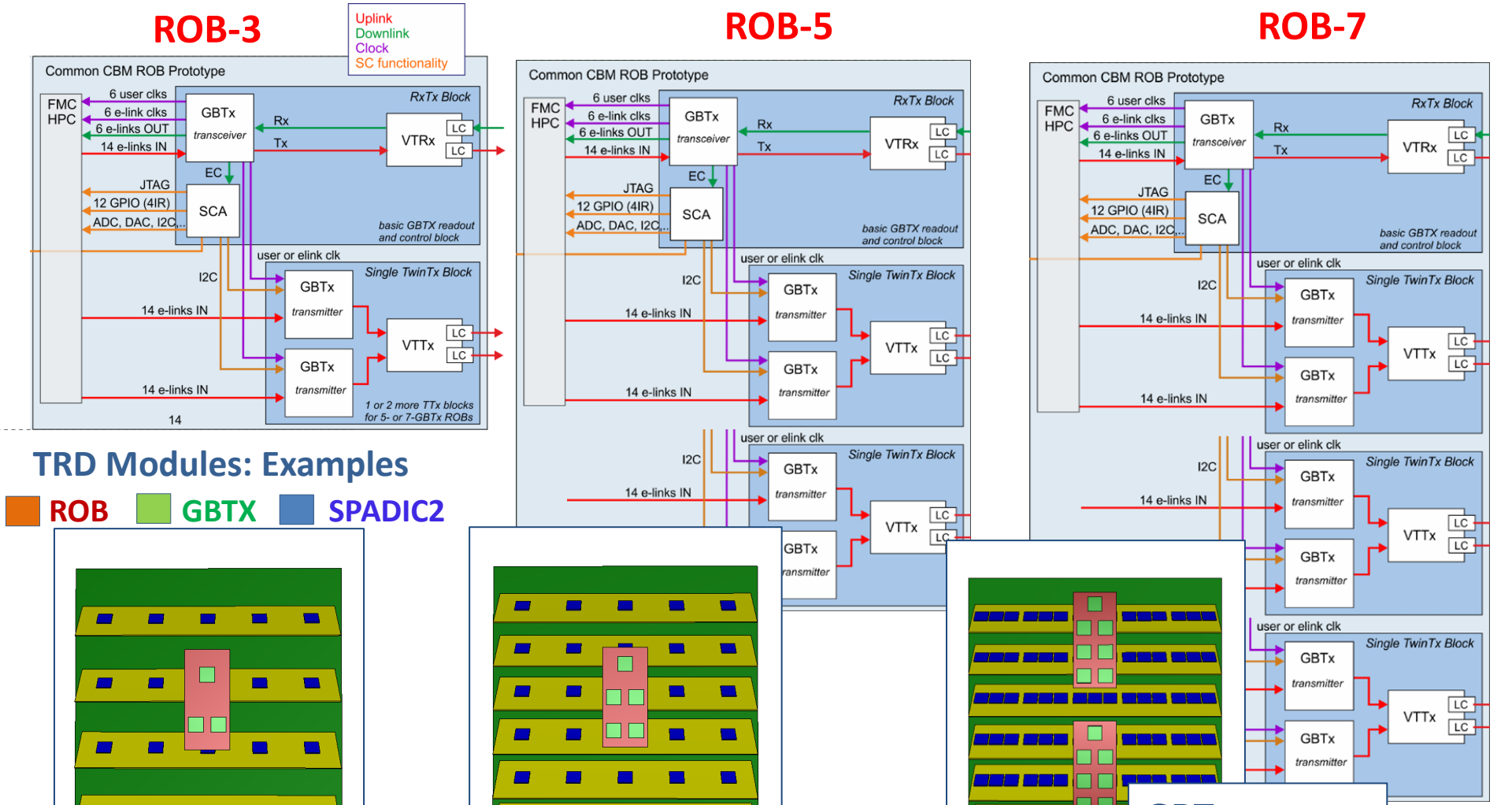
Time of Flight Detector



GBT use cases

1. **Scrubbing** of FPGA in first concentration stage
   - JTAG chain and serial I/O from SCA to FPGAs on 4 TOF-ROB
   - TOF-ROBs placed at larger radial distances for reduced irradiation
2. Second **data concentration** stage
   - readout of up to 4 TOF-ROB units with one GBTX-ROB-1
   - TOF-ROBs in high rate areas (no concentration from multiple TOF_ROBs) may use direct optical link to DPB
   - alternatively use GBTX stage directly as first concentrator and omit FPGA stage

Transition Radiation Detector



TRD Modules: Examples

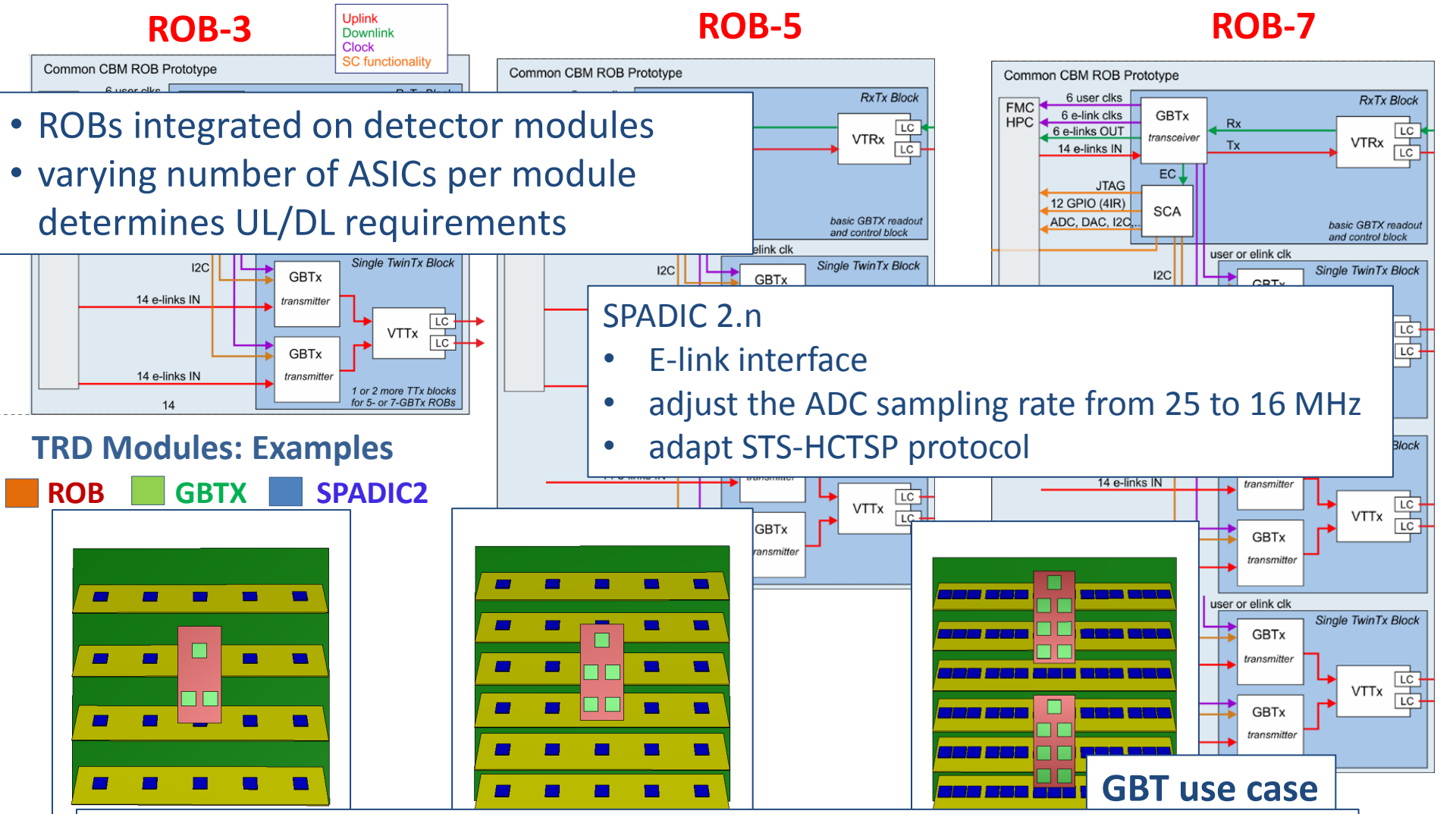
ROB GBTX SPADIC2

GBT use case

Flexible matching of data from individual modules to readout capabilities

- 1 or 2 ROB-3/-5/-7 with **1 to 3 TwinTx blocks**

Transition Radiation Detector



- ROBs integrated on detector modules
- varying number of ASICs per module determines UL/DL requirements

SPADIC 2.n

- E-link interface
- adjust the ADC sampling rate from 25 to 16 MHz
- adapt STS-HCTSP protocol

TRD Modules: Examples

ROB **GBTX** **SPADIC2**

GBT use case

Flexible matching of data from individual modules to readout capabilities

- 1 or 2 ROB-3/-5/-7 with **1 to 3 TwinTx blocks**

Status and Timeline

- **latest ASIC versions** implementing the E-Link interfaces and compatible protocols available ***now*** for testing
- C-ROB available from early 2017 → initial tests of full readout chains
- full prototype readout chains in test beam times with larger detector setups requiring aggregation
- Phase0 (i.e. pre SIS100) experiments
  - 10% of TOF@STAR/RHIC for BES II
  - miniCBM@GSI/SIS18:
    full size detector modules and readout chains up to FLES
- development of detector specific ROBs
- CBM installation and commissioning: 2020/21

GBT Usage in CBM Detectors - Overview

		STS	MUCH (Station 1&2)	TOF	TRD
Technology		Silicon strip	GEM	MRPC	TRD
Frontend ASIC		**STS**/MUCH-XYTER 128 channels *AGH Cracow*	STS/**MUCH**-XYTER 128 channels *AGH Cracow*	GET4 4 channels *GSI*	SPADIC 32 channel *ZITI Univ. Heidelberg*
Readout		1 to 5 E-Links (configurable) at 320MHz		1 E-Link (compatible) at 80 MHz	2 E-Links at 320MHz
Configuration & SC & FC		DL: dedicated E-Link shared by ASICs UL: all E-Links, shared with data		DL: control UL: control in data stream	DL: shared E-Link UL: single E-Link shared with data
Clock		Phase adjustable clock@160MHz		Dedicated distribution of 160MHz clock(tbc)	Phase adjust. Clk or E-Link Clk at 160MHz
Channels		1.8 million	249k	100k	245k
No. E-Links	**DL**	1.800	1.944	25.000 ASIC links	<7.500
	UL	20.000	7.776	25.000 ASIC links	15.000
Versatile Links	**DL**	600	216	<= 625	240
	UL	1.800	648	<=625	1.152
Note: all numbers are for experimental scenario of 1e7 Au+Au@10AGeV (SIS100) unless stated differently					

CBM Contributions to TWEPP 2016

- A. Rost (TU Darmstadt), *A flexible FPGA based QDC and TDC for the HADES and the CBM calorimeters*; Oral Tue. 15:40

- **J. Michel (Univ. Frankfurt), *Electronics for the RICH Detectors of the HADES and CBM Experiments*; Poster I3**
- V. Shumikhin (NRNU MEPhI), *6-Bit Low Power Area Efficient SAR ADC for CBM MUCH ASIC*; Poster F4
- E. Atkin (NRNU MEPHI), *Development of 32-Channel System for Processing Asynchronous Data from the CBM GEM Detectors*; Poster C6
- **W. Zabolotny (Warsaw University of Technology), *Versatile ASIC and Protocol Tester for STS/MUCH-XYTER2 in CBM Experiment*; Poster N4**

- J. Lehnert (GSI), *GBT based readout in the CBM experiment*; Oral Wed. 15:15

- E. Malankin (NRNU MEPhI), *Readout Channel with Majority Logic Timestamp and Digital Peak Detector for Muon chambers of the CBM Experiment*; Poster E3
- K. Kasiński (AGH), *System-Level Considerations of the Front-End Readout ASIC in the CBM Experiment from the Power Supply Perspective*; Poster N5
- **R. Kleczek (AGH),** *Front-End* ***and Back-End Solutions in the CBM STS Readout ASIC*; Poster E1**
- **L. Meder (KIT), *A Versatile Small Form Factor Twisted-Pair TFC FMC for mTCA AMCs*; Poster I8**

Tuesday

Wednesday

... a common readout effort shared by many ...

STS: GSI Darmstadt, WUT Warsaw, AGH Krakow,
MUCH: VECC Kolkata,
TRD: Univ. Heidelberg(ZITI), Univ. Muenster,
TOF: GSI Darmstadt , Univ. Heidelberg(PI), Univ. Frankfurt(IRI),
DAQ: GSI Darmstadt , FIAS Frankfurt , KIT Karlsruhe,

Thank you for your attention!