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A versatile Small Form Factor Twisted-Pair TFC FMC for mTCA AMCs

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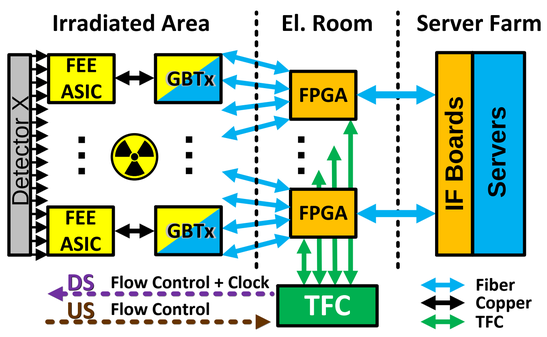
1. The Detector Readout of CBM

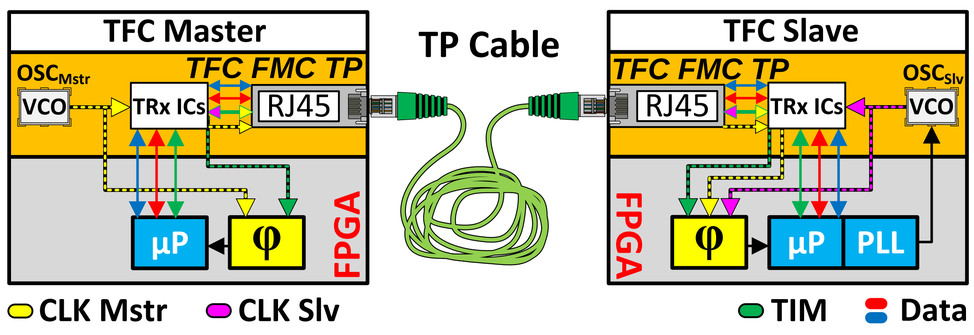


Topology of the planned CBM Detector Readout

- Data transmission between three separated areas through Optical Fiber
- FPGAs in mTCA.4: central layer between data acquisition and post processing
- FEE uses clock derived from Downstream link provided by the GBTx chips
- **Both, FEE and FPGA Layer** need to be operated **synchronously**
- Self-triggered Readout requires **low latency links to a global Flow Control**

These Tasks are addressed by the **Timing and Fast-Control (TFC)**

2. Concept of a TFC System with Twisted-Pair (TP) Cabling



Fundamental TFC Master-Slave Interfacing Approach with Twisted-Pair Link

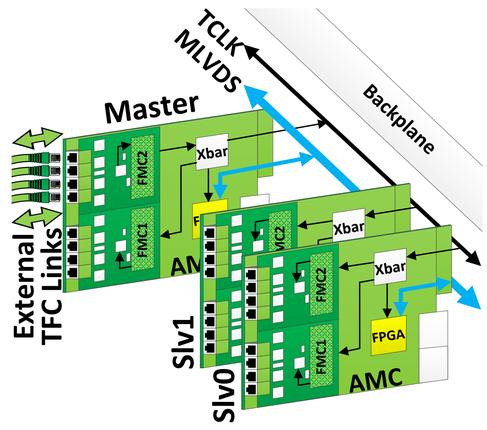
Concept:

- **Two SYNC Layers:**
- SYNC of **Readout Crates**
  ⇒ TFC Master ⟷ TFC Slaves
- SYNC **inside Readout Crate**
  ⇒ TFC Slave ⟷ Readout Boards

TP SYNC Outside Crates:

- **Interfacing PCB** for Connectivity
- **4 Lines**: 1x Mstr-Clk, BIDI TIM and Data
- Phase measurement, **PLL for Slv VCO**
- Regulation: **Freq: Mstr-Clk**, **Phase: TIM**

3. TFC FMC TP in an mTCA Crate

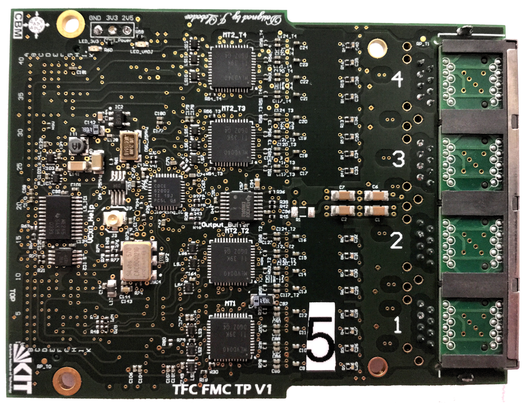


TFC FMC TP mounted on AMCs in an mTCA.4 Crate

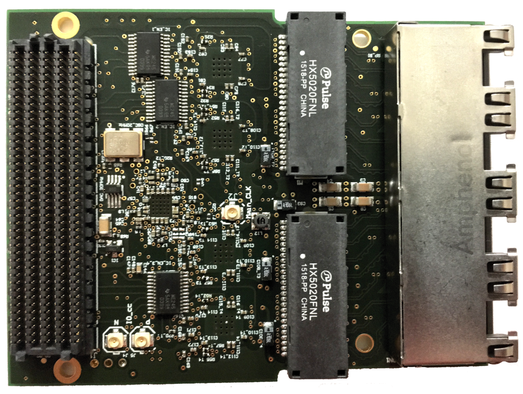
- For compatible AMC cards (like AFCK), TFC FMC TP main clock can be shared
  ⇒ With another FMC on the same AMC
  ⇒ With AMCs in the same crate
- **This allows synchronizing a Readout Crate** (TFC Slave ⟷ DPBs)
- But also to create **Multi-Master TFC Crates** (TFC Master ⟷ TFC Master)
  ⇒ Increases number of Slave crates by **Factor N = #AMCs of Master crate**

4. The TFC FMC TP PCB Prototype Boards

- 6-Layer PCB, close to ANSI/VITA 57.1 Mezzanine Dim. (69 mm x 88.9 mm)
- Galvanically isolated signals, capacitively coupled cable shield ground



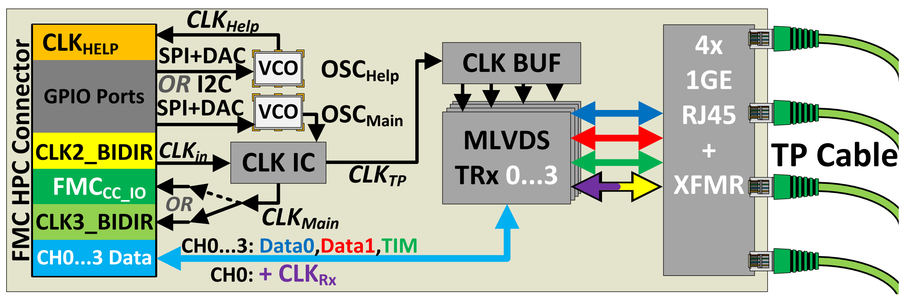
TFC FMC TP Board - Top View



TFC FMC TP Board - Bottom View

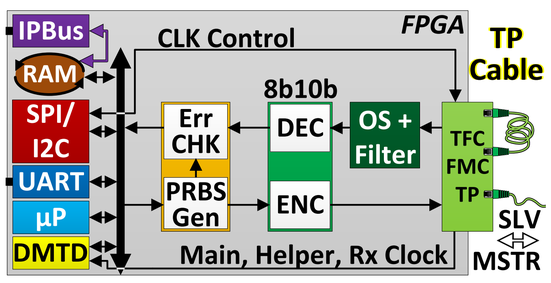
5. Block Diagram of the TFC FMC TP PCB

- **ANSI/VITA 57.1 FMC HPC Connector**
- **4-Port RJ45+XFMR** → Twisted-Pair IF
- **MLVDS ICs, Half-Duplex support**
  ⇒ Large Voltage-Swing
  ⇒ BIDI Transmission
- **Dedicated flexible Clocking IC**
- **Clk Buffer:** High Qual. Clk for TP TRx
- **Voltage Controlled Oscillators**
- **Main Clk:** VCO → CLK IC → CLK_{Main}
- **Helper Clk:** VCO/progr. Osc → CLK_{Help}
- **FMC BIDI Clks:** Tx/Rx of Main Clk
  ⇒ System Clk, Sharing of Clk in Crate
- **RJ45 Port0:** With TFC Slave Funct.



Block Diagram of the TFC FMC TP PCB

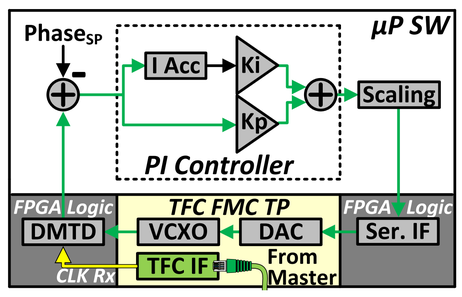
6. Evaluation system with TFC FMC TP PCB



µP System for Transmission Tests and Slave OSC Sync. (PLL)

Loopback TRx with 25m CAT7 cable:

- **8b10b encoded PRBS sequences**
- **Bit error ratio testing**
  Rx data ⟷ Ref. sequence
- **TRx: 3x240 Mbit/s Data, 120 MHz CLK**

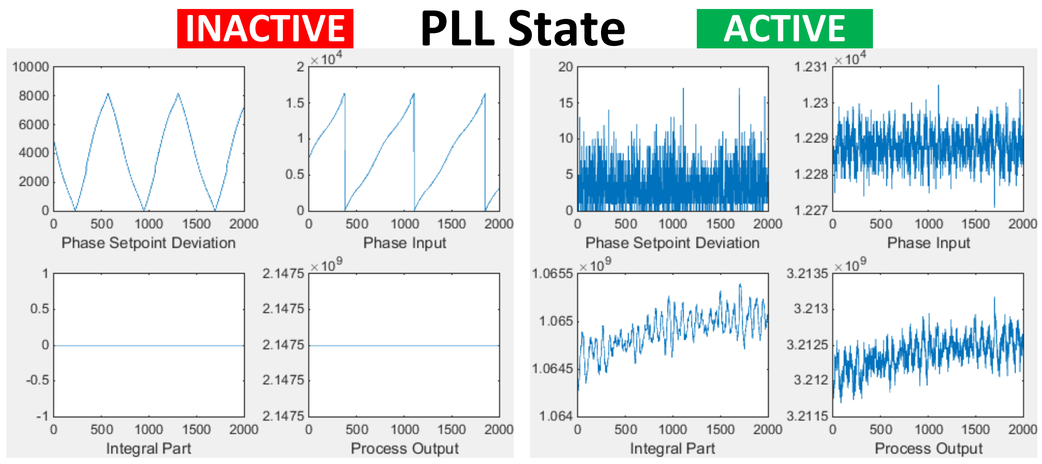


PLL Control Loop with TFC FMC TP Board

TFC Master-Slave System: PLL Control

- **μP computes control loop parameters**
- SPI/I2C for OSC and CLK IC CTRL
- **Rx CLK from TP IF:** PLL Ref. Frequency
- **Phase Detector: DMTD** (FPGA Logic)

7. Measured PLL Control Loop Behavior



Recorded PI Controller Parameters (Circular RAM) of a) ***INACTIVE*** *and* b) ***ACTIVE****, Locked Control Loop*

8. Summary

- **Versatile TP-based TFC FMC**
- **Dimensions for being mounted onto AMCs for mTCA.4 Crates**
- **Sharing of Clocks inside Crate**
- **BIDI MLVDS Transmission Concept** → Determine Master-Slave Phase Offset
- **Test System** proves the **Capability** to:
  - **TRx at 240 Mbit/s/120 MHz, 25 m CAT7**, all lines used, different direct.
  - **Perform PLL-based SYNC using VCOs and DMTD Approach** → High Quality copy of Master CLK