Readout Channel with Majority Logic Timestamp and Digital Peak Detector for Muon Chambers of the CBM Experiment

E. Atkin[1], I. Bulbakov[1], V. Ivanov[1,3], P. Ivanov[1], E. Malankin[1], D. Normanov[1], I. Sagdiev[1], V. Samsonov[1,3], V. Shumikhin[1], O. Shumkin[1], S. Vinogradov[1], A. Voronin[1,2]

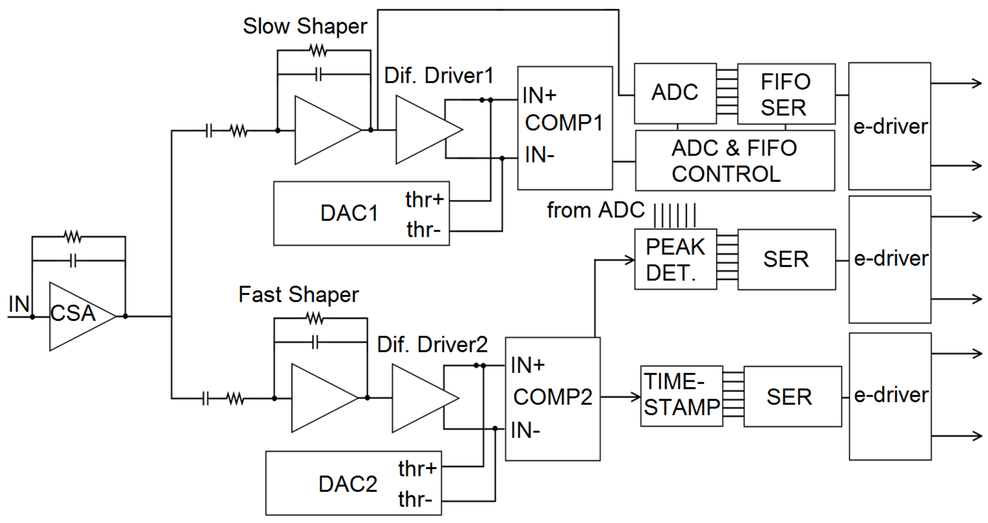
[1]National Research Nuclear University MEPhI, Moscow, Russia
[2]Skobel'tsyn Institute of Nuclear Physics, Moscow State University, Russia
[3]Petersburg Nuclear Physics Institute, NRC Kurchatov Institute, Gatchina, Russia

Abstract

A prototype readout channel was manufactured in UMC CMOS 180 nm for the purpose of the CBM experiment at the FAIR accelerator. The channel includes a preamplifier with fast and slow CR-RC shapers, discriminator with a differential threshold setup circuit, 6 bit SAR ADC (40 MSps, 1.5 mW power consumption), digital peak detector and block of the time stamp registration. The control data, clock and output data are supplied through a SLVS transmitter and receiver. The slow and fast channels have an 1500 e^- and 2000 e^- ENC accordingly at a 50 pF detector capacitance. Power consumption is 10 mW/channel.

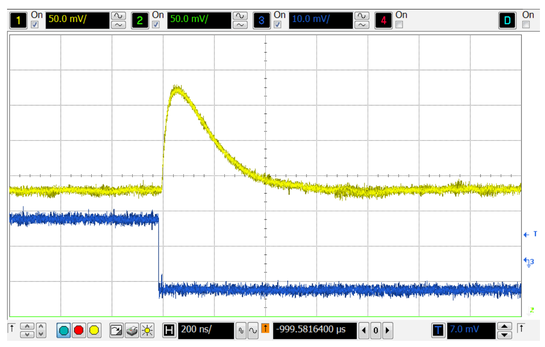
ASIC Structure

The MUCH detector is built with GEMs. Since the sensors will have different granularity, the requirements to the front-end electronics are also different for the central and peripheral parts. Thus, the preamplifier is followed by two circuits: a slow channel, optimized for S/N ratio in order to use it in the periphery, and a fast one, adapted to the hit rate of the inner detector part, where the occupancy is the highest. The fast channel is also supposed to be used for the timestamp determination. Both channels are realized with CR-RC shapers with different peaking times, 60 ns and 260 ns accordingly. The channel is optimized to operate with the negative charge polarity. The preamplifier dynamic range is 100 fC. The channel occupancy is up to 1 MHz. The signal from either the slow or fast shaper (depends on occupancy) is processed by a 6 bit SAR ADC. The ADC is followed by a digital peak detector. The chip has fast and slow discriminators. The fast discriminator output is connected to a timestamp block. Both fast and slow discriminators can be used by the logic for hit overlap detection. In the current version the data from ADC, peak detector and timestamp are serialized and sent out via an SLVS transmitter.

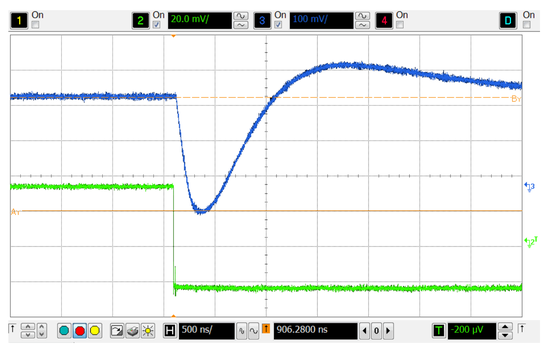


Analog Channel

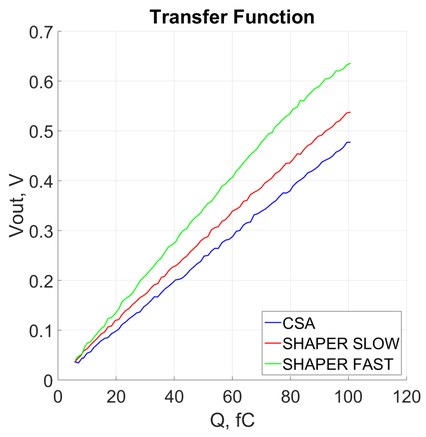
Generator tests of the prototype ASIC functionality were provided. The test pulse from generator was supplied through the serial capacitance 1.2 pF. Functionalities of the CSA, Shapers, Comparators and DAC were checked.

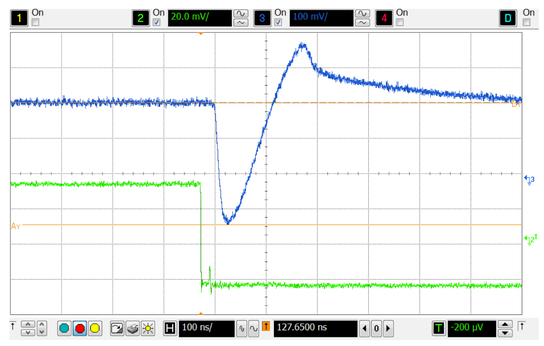


CSA



SHAPER SLOW

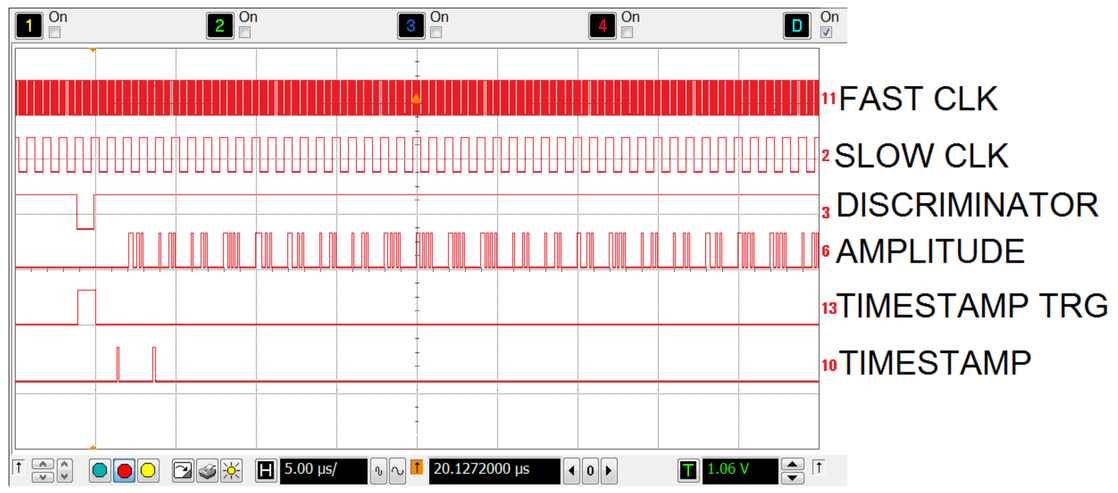




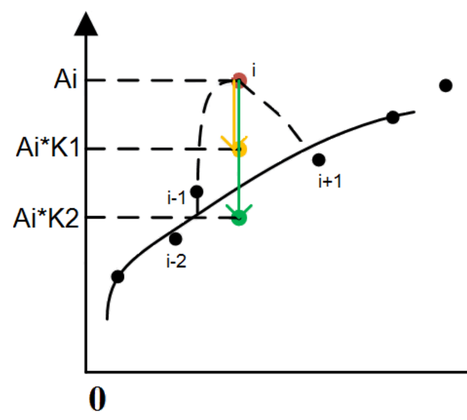
SHAPER FAST

Majority Logic Timestamp

The timestamp block contains three Gray code counters which specify the global chip time. The signal from the fast discriminator starts the timestamp block. Value from counters is recorded to the local channel time registers. After that, the majority logic block compares data from registers and sends them to the timestamp output.

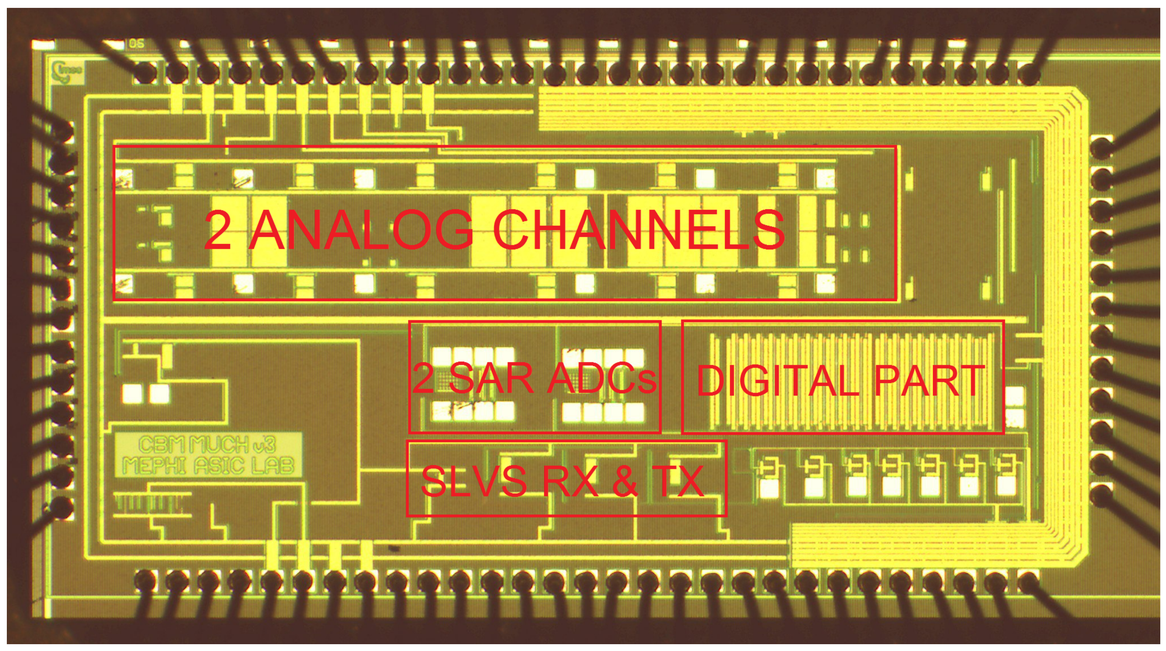


Digital Peak Detector



The digital peak detector finds the peak in the ADC data. The peak detector has a function of preventing false peak finding due to the presence of noise spikes. The average sum of the previous three ADC samples is compared with the current sample multiplied by reduction factor. If the average sum is less than the current sample, it means that the found peak is false.

ASIC Layout



The MUCH ASIC v3 was designed and prototyped via Europractice by means of the 0.18 μm CMOS MMRF process of UMC. The die size is 3240 x 1525 μm^2.

References

- E. Atkin et al. 2015 JINST **10** C04006
- E. Malankin et al. 2016 JINST **11** C01084

Contacts

E. Malankin, ASIC lab and the Department of Electronics,
National Research Nuclear University "MEPhI", Kashirskoe shosse 31, Moscow, 115409, Russia.

E-mail: ezmalankin@mephi.ru, tel. +7 499 3242597