SLVS Transmitter and Receiver for Readout ASIC

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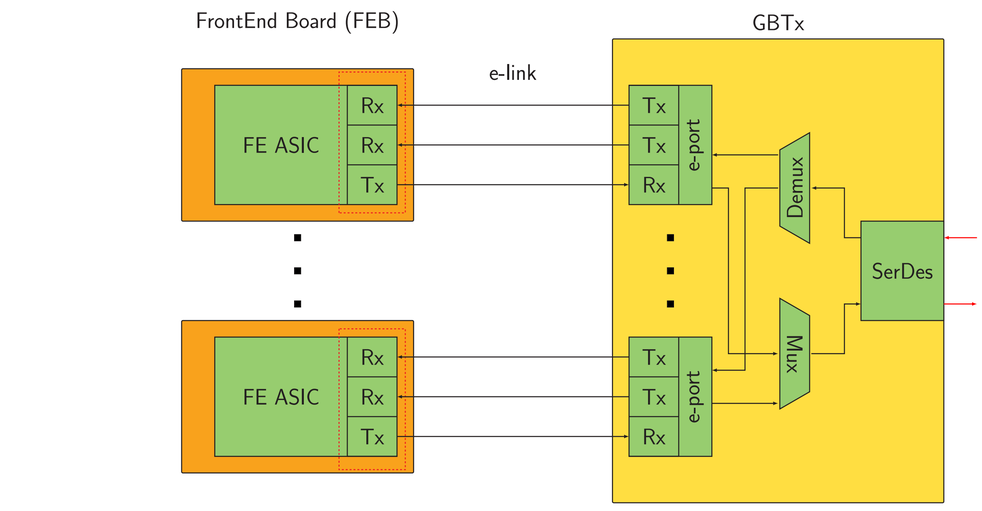
Abstract

The Scalable Low Voltage Signaling (SLVS) Transmitter (Tx) and Receiver (Rx) IP blocks are designed in the UMC 180 nm CMOS technology as component of the readout ASIC for the muon chambers (MUCH) of the CBM experiment. Tx and Rx are the prototype of the physical layer of the e-link interface that is used for ASIC-GBTx connection. The experimental results at 320 Mbit/s are presented.

Introduction

The Gigabit Transceiver (GBTx) chip is designed in CERN for providing interface between readout ASICs and the off-detector data processing system. Up to 57 FE ASICs are connected to the GBTx. Connection between ASICs and GBTx is implemented by an e-link interface. Data from FE ASIC are sent to GBTx (transfer speed up to 320 Mbit/s per link), then serialized and sent to an off-detector processing system via an optical link (speed up to 4.8 Gbit/s). The physical layer of the e-link interface is implemented in accordance with the SLVS (or LVDS) standard. In particular, it is planned to use the structure described above in the Silicon Tracking System (STS) and MUCH of the CBM experiment (FAIR, Darmstadt). However, Tx and Rx are also needed for other experiments (e.g. NICA at Dubna). Therefore, the SLVS transmitter and receiver pair is a universal block for providing compatibility with the e-link interface.



SLVS Standard

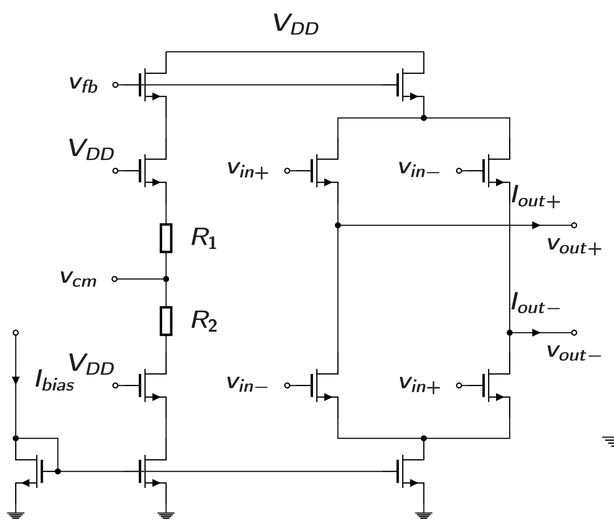
SLVS parameters related to the e-link requirements:

Parameter	Value
Common Mode Voltage	0.2 V
Differential Voltage Swing	±200 mV
Output Current	2 mA
Load Resistance	100 Ω
Clock Frequency	up to 320 MHz
Data Rate	up to 320 Mbps

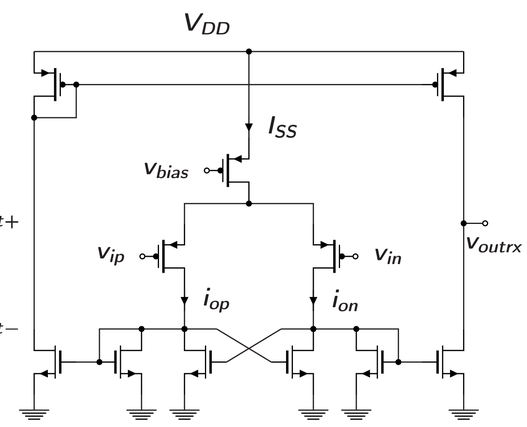
Schematic

The SLVS transmitter is implemented by a switched polarity current source based on an H-bridge of N-channel MOS transistors, replica bias controls the output common mode voltage via common mode feedback. E-link standard allows a few of different transmitter output current values for different transmission speeds (up to 2 mA), but in for this chip only the maximum current value is provided.

The SLVS receiver is implemented by a P-MOS input transistors comparator with output buffer. Because of low common mode voltage, the provision of rail-to-rail input for this comparator is not necessary.

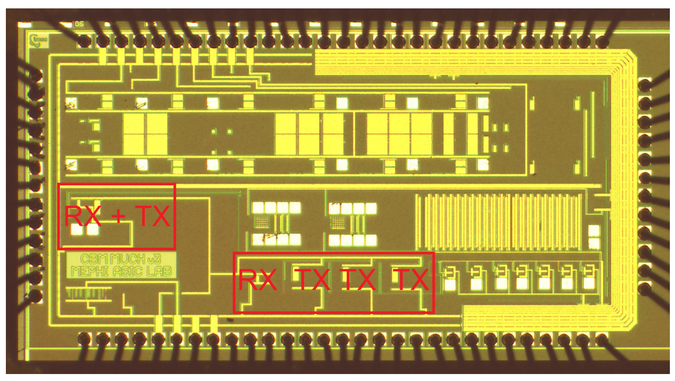


Transmitter output stage



Receiver input stage

ASIC Layout

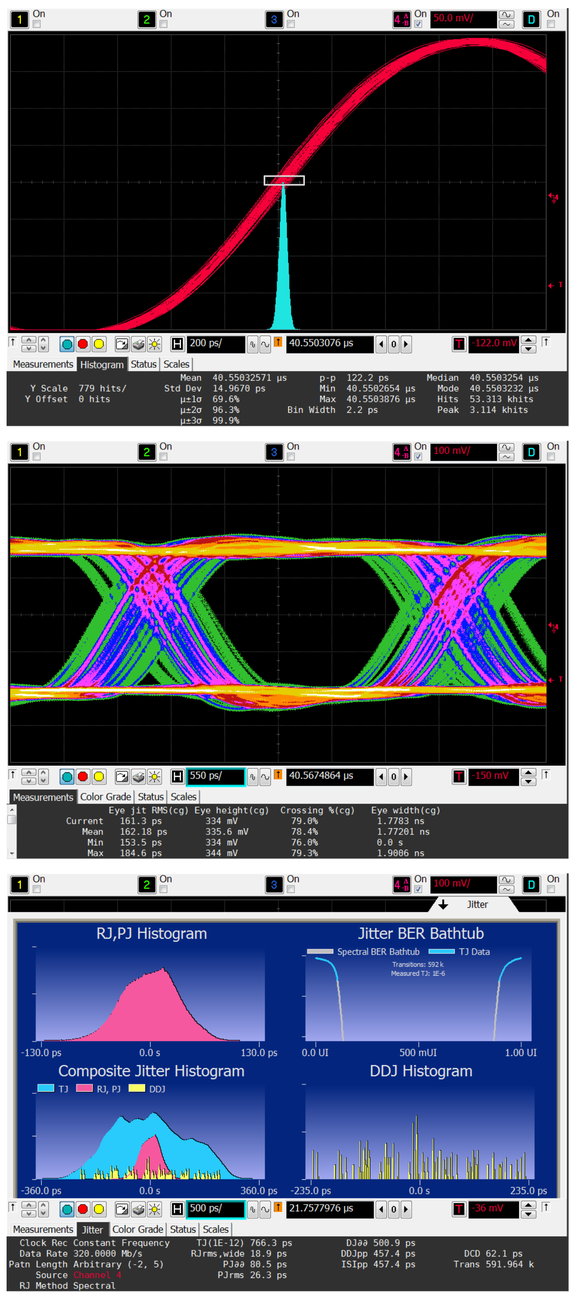


- Europractice run of September 2015
- UMC 180 CMOS MMRF
- Area: 3240 x 1525 μm^2
- Contains 3 Tx and 1 Rx blocks
- Also contains test block (Rx to Tx link with internal pad at Rx output)

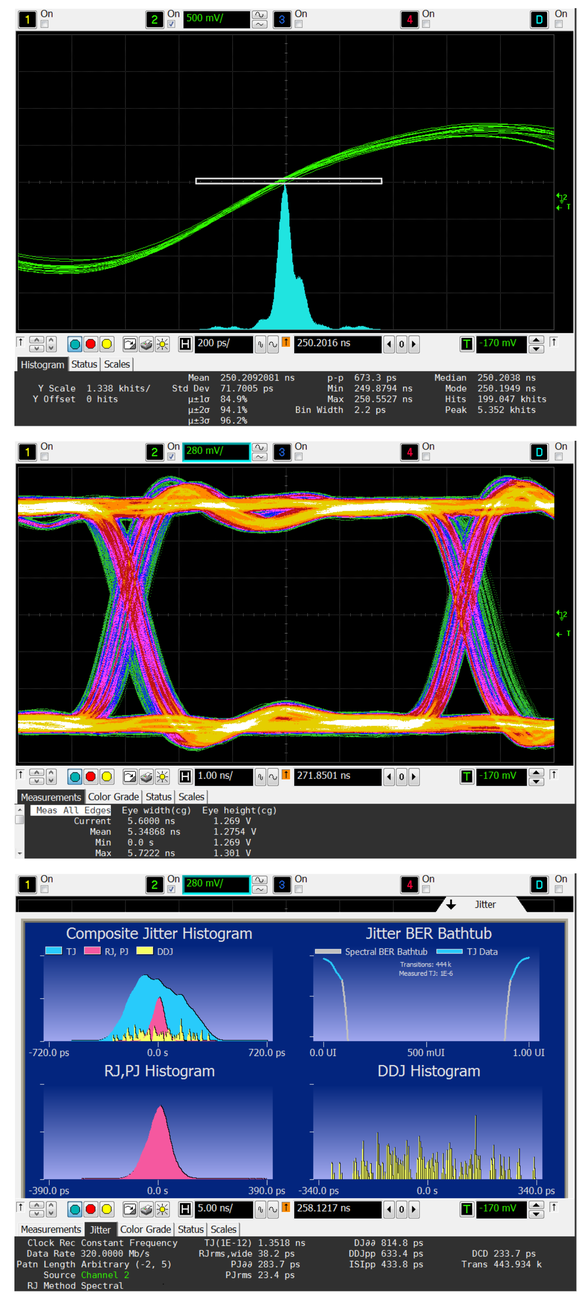
Measurements

- Two sets of the measurements for Tx and Rx:
  - Clock signal (40/80/160/320 MHz)
  - PRBS data stream (40/80/160/320 Mbps)
- Transmitter output signal via Agilent Differential Probe
- Receiver output signal from the internal pad via Picoprobe

Transmitter



Receiver



Parameter	Transmitter	Receiver
Supply voltage, V	1.8	1.8
Power consumption (at 320 MHz), mW	6.6	1.2
Clock jitter std. deviation (at 320 MHz), ps	15	70
Eye height (320 MBps), V	0.35	1.4
Silicon area, μm^2	180x125	150x55

References

- S Bonacini et al. *e-link: A radiation-hard low-power electrical link for chip-to-chip communication*
- A Boni et al. *LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS*

Acknowledgements

This work was supported by the Ministry of Education and Science of the Russian Federation (grant no.14.A12.31.0002) in accordance with the RF government order no. 220.

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