MVD SPD

Sezione di Torino

Status report of the pixel detector readout electronics

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Performances - 1

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Parameter	Current value	Other proposal	Status
Pixel size	100 μm × 100 μm		Fixed
Chip active area	10 mm × 10 mm	11.4 mm × 11.6 mm	To be fixed
dE/dx method	Time over Threshold		Fixed
Max input charge	100 fC		Fixed
Clock	50 MHz	100,125,150 MHz	To be fixed
Time resolution	5.77 ns rms @ 50 MHz	2.31 ns rms @ 125 MHz	To be fixed
Max event rate	12.3 MHz/cm^2	Ongoing simulations	To be fixed
Data rate per chip	615 Mb/s	815 Mb/s	To be fixed

Performances - 2

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Parameter	Current value	Other proposal	Status
Analog gain	40 mV/fC		~ Fixed
ToT gain	180 ns/fC	72 ns/fC	To be fixed
Max ToT	18 μs	7.2 μs	To be fixed
Signal polarity	Either n or p		Fixed
Analogue noise	0.032 fC (200 e-)		~ Fixed
Quantization noise	0.032 fC (200 e-)		~ Fixed
Sensor leakage current	< 50 nA/pixel		
Power consumption	< 750 mW/cm^2	< 500 mW/cm^2	To be fixed

Performances - 3

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Parameter	Current value	Other proposal	Status
Total Ionizing Dose (PANDA lifetime)	10 Mrad		To be confirmed
Neutron fluence (PANDA lifetime)	$5 \cdot 10^{14}$ 1MeV n_{EQ}/cm^2		To be confirmed
LET threshold			To be defined
SEU saturation cross section			To be defined

ToPiX pixel cell

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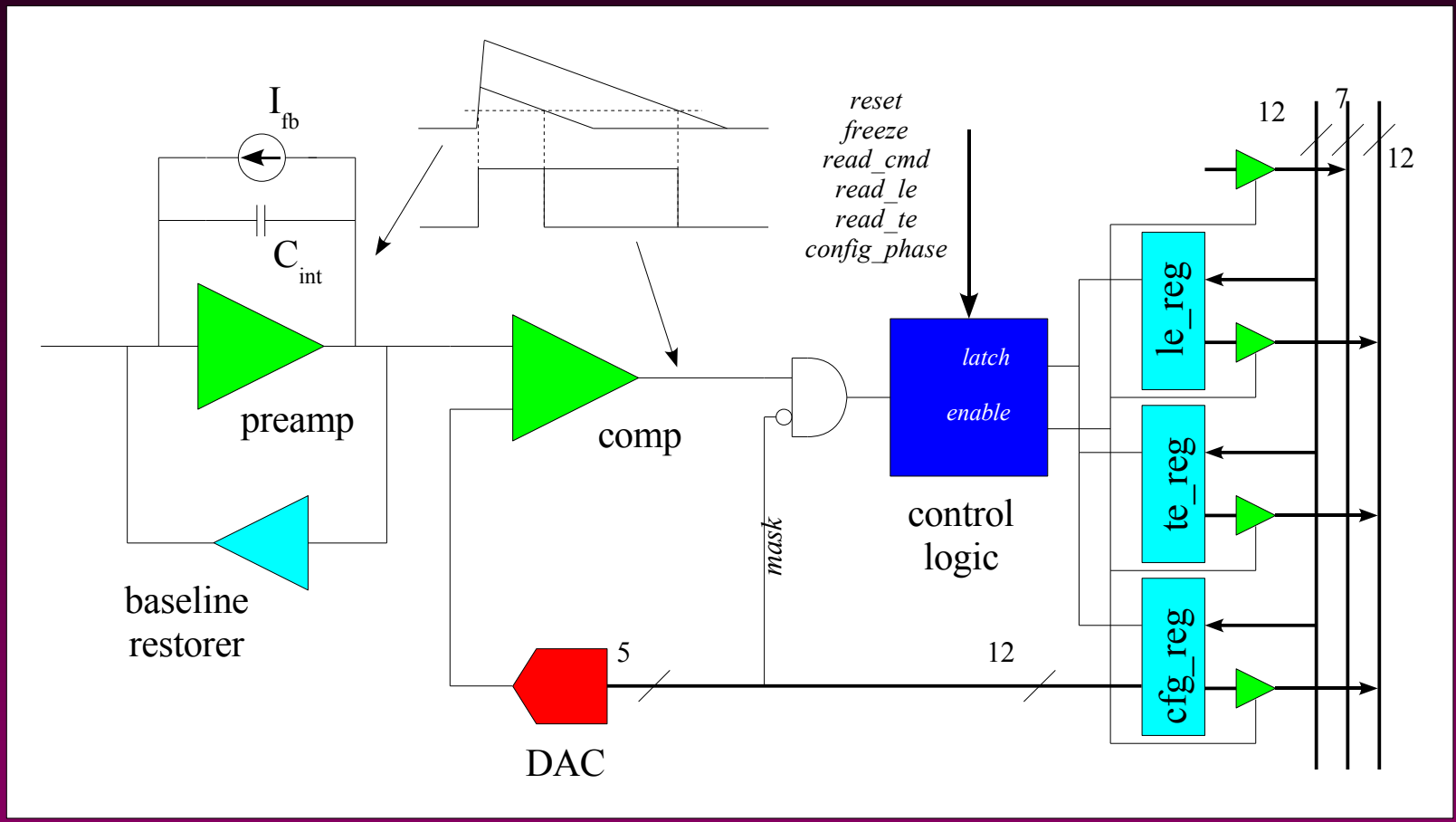

ToPiX prototype

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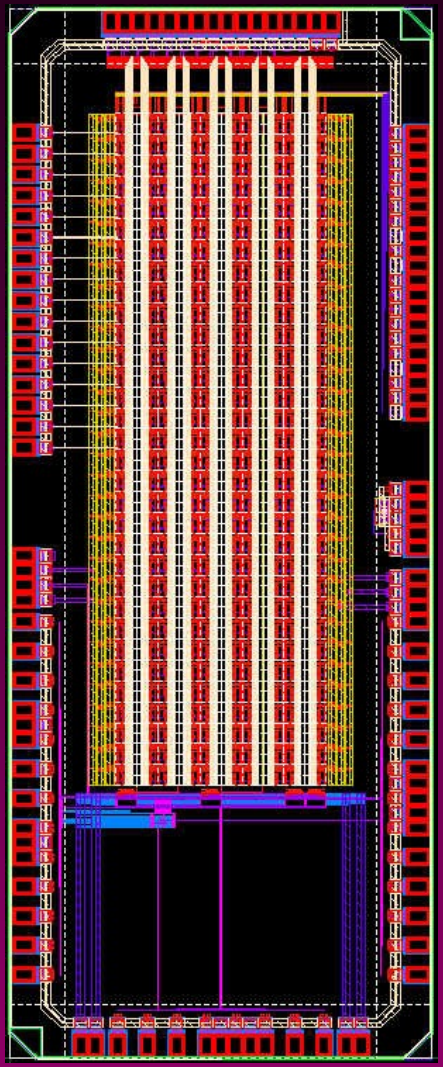
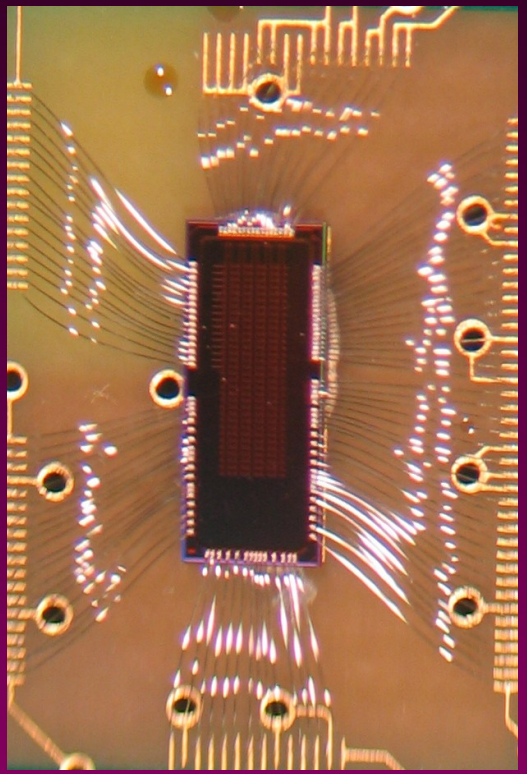


- Full pixel cell (analogue + digital)
- Two folded columns with 128 cells
- Two columns with 32 cells
- 5x2 mm^2 die area
- CMOS 0.13 μm LM technology
- Working frequency : 50 MHz
- Dice-based SEU resistant FFs
- Tests :
  - → test bench
  - → with a sensor and a radiation source
  - → TID and SEU



ToPiX upgrade - 1

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- Technology : LM → DM
  - Reason : DM will become the HEP mainstream
  - LM : 6 (thin) + 2 (thick) metal layers
  - DM : 3 (thin) + 2 (thick) + 3 (RF) metal layers
  - bus width increases by a factor of 3÷4
  - shared bus among adjacent columns
  - better power routing (thicker lines)
  - signal routing is critical

DM – LM bus comparison

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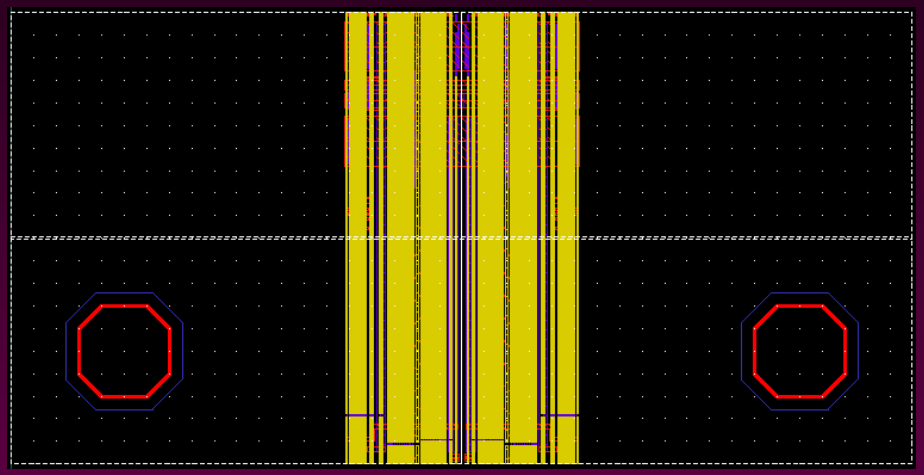
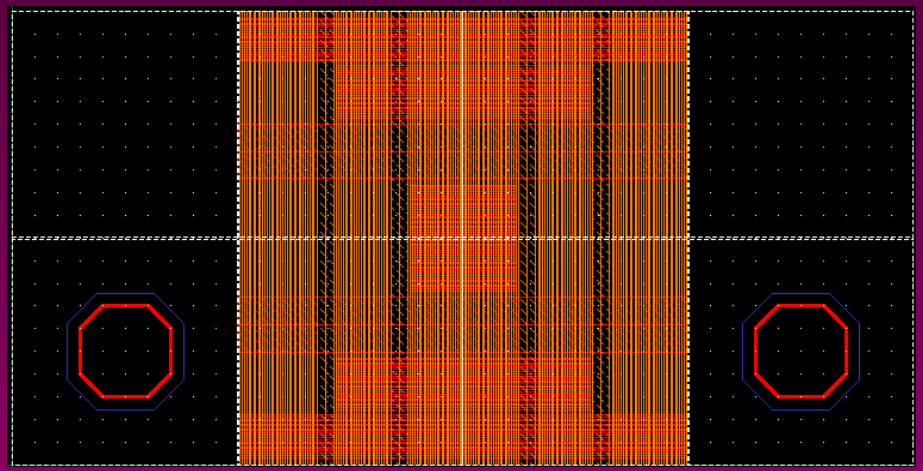


25 μm

LM option : bus routing on M4 and M6

DM option : bus routing on MG only

100 μm



ToPiX upgrade - 2

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- Working frequency : 50 MHz → 125 MHz
  - Time stamp bin : 20 ns → 8 ns
  - Column readout : 40 ns → 32 ns
  - Column drivers and receivers to be redesigned
  - New system simulations required
- SEU protection : DICE cells → triple redundancy
  - Size increase (estimated : × 1.5÷2) in the digital part of the chip → rescaling of the analog part
  - TMR with correction in the configuration register only

Module

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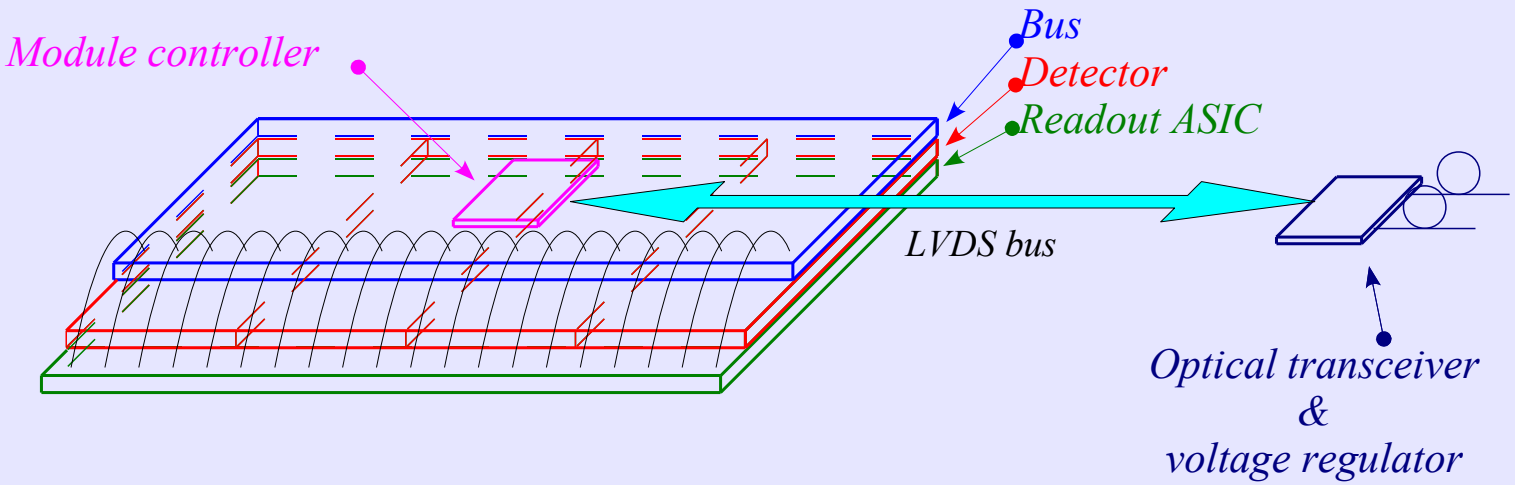

Module concept - 1

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- Modules with different size required (2,4,5 and 6 F/E chips)
- Up to four 250 Mb/s serial links between ToPiX and module controller.
- 2 or 3 ToPiX chips per module controller
- Module controller to service board : up to 3 × 1 Gb/s electrical links ($f_{CK} \times 8 \rightarrow$ PLL needed)
- Module controllers can be chained
- Up to 6 F/E ASICs per service board
- Service board to counting room : 3.2 Gb/s optical link

Module concept - 2

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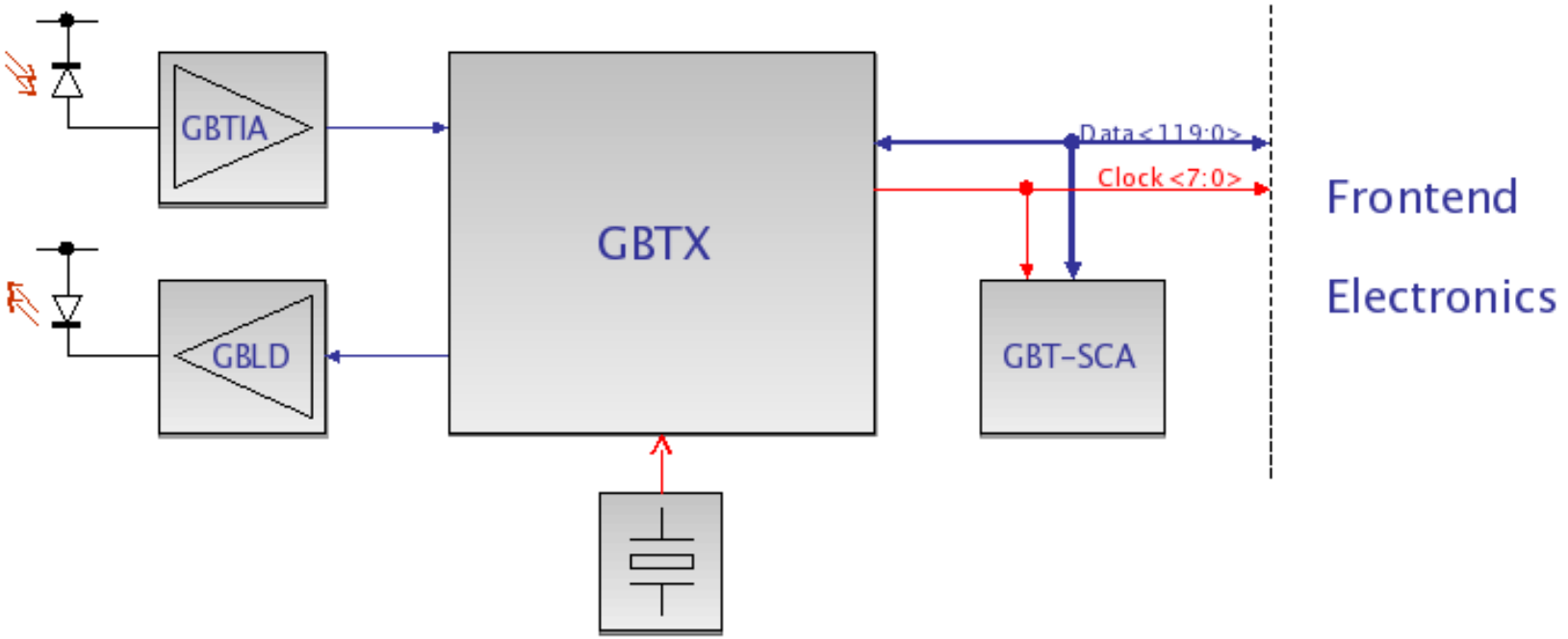
- The module controller functions :
  - → Data concentrator
  - → Cable reduction
  - → Interface between ToPiX and the non-custom circuits
- Service board size and position to be fixed
  - → influences on power and signal traces
- Connector position

Worst nightmare : cable routing

GBT Chipset

- *Radiation tolerant chipset:*
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and timing and transceiver
  - GBT-SCA: Slow control ASIC
- *Supports:*
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s
- *The target applications are:*
  - Data readout
  - TTC
  - Slow control and monitoring links.
- *Radiation tolerance:*
  - Total dose
  - Single Event Upsets



GBT frame

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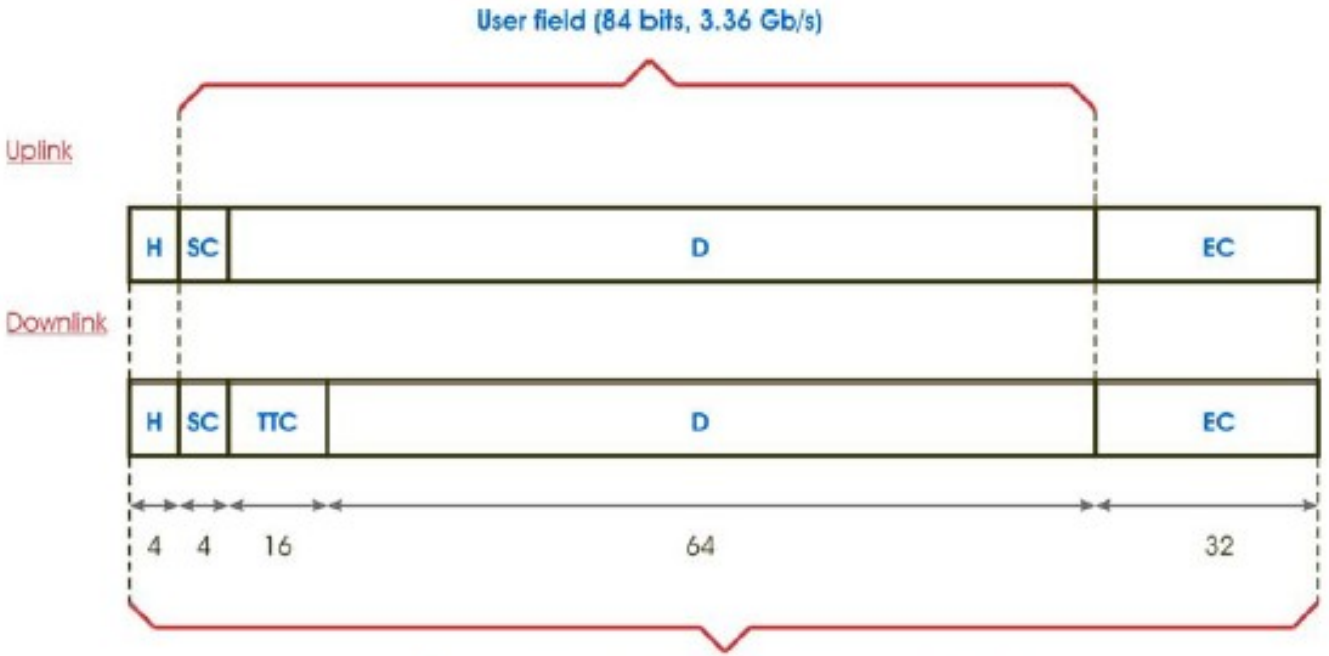
2.1 Frame structure



Frame: 1 SLHC Clock Cycle (120 bits, 4.8 Gb/s)

H - Header

SC - Slow Control (160 Mb/s)

TTC - Timing Trigger and Control (640 Mb/s)

D - Data (2.56 Gb/s)

EC - Error correction

Conclusions

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- A ToPiX v2 prototype has been designed and tested with good results, *but...*
- *...due to the clock and technology flavour change a major upgrade is required*
- The module controller will require relatively high speed serial links → custom design, contacts with sLHC groups with similar developments for building blocks sharing
- Position of the service board to be fixed – ideally as close as possible to the module
- Existing (GOL) or under development (GBT) rad-hard transceiver for the electrical – optical connection