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Electronic simulation

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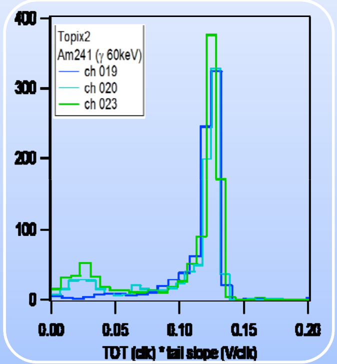
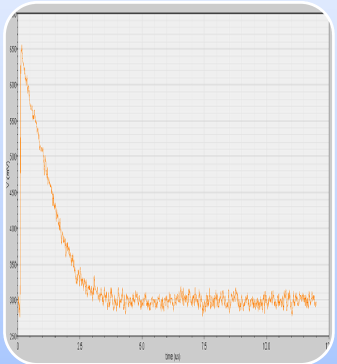
Outline

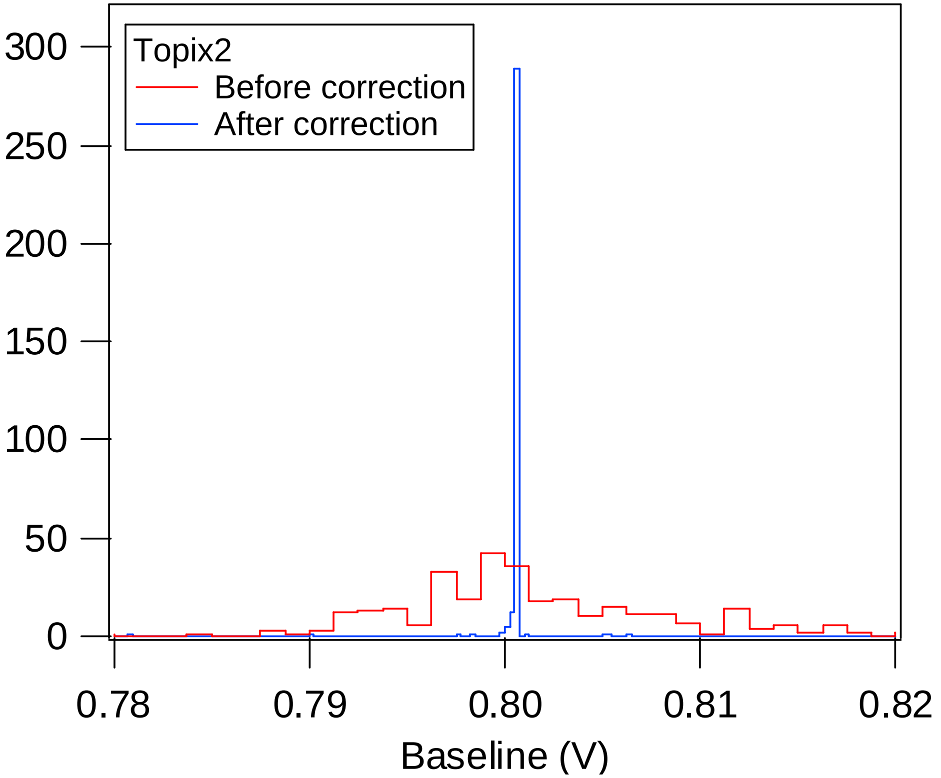


Update on the last ToPix measurements.

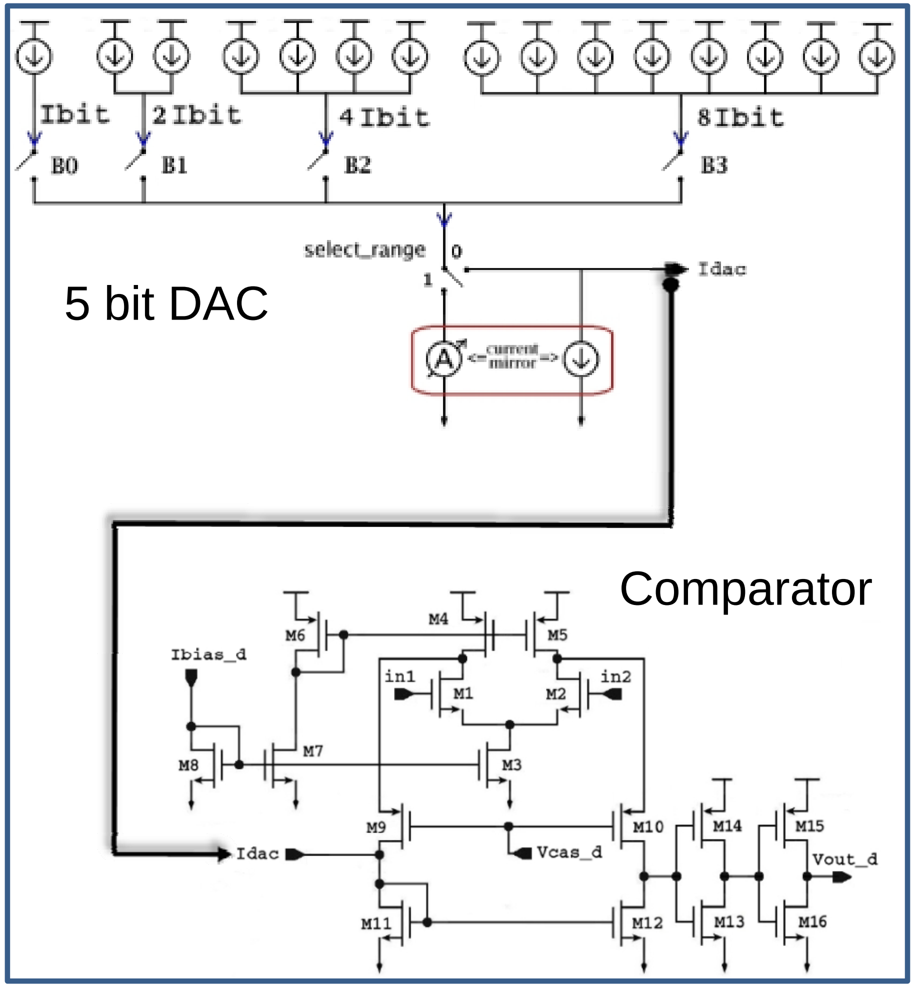


First simulations of a "strip adapted" ToT Front-End

Measure: threshold dispersion



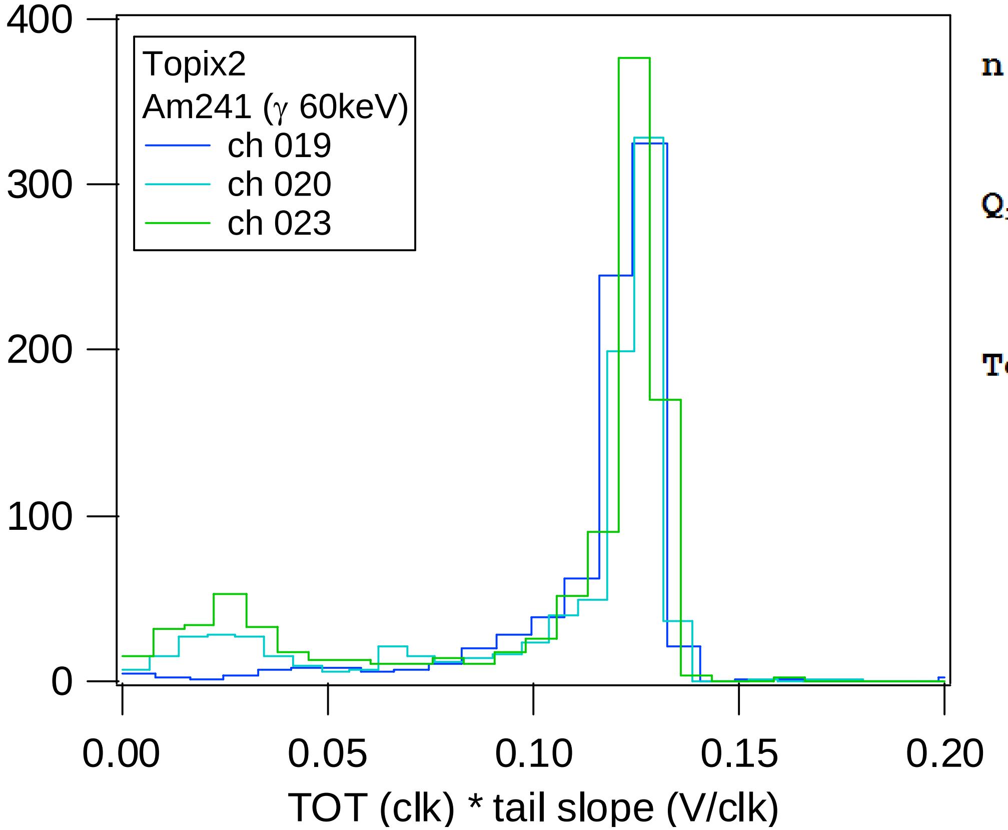
To mitigate the threshold dispersion a local 5 bit DAC is added in each pixel, to allow a fine tuning of the threshold on a pixel by pixel basis.



Compensation system in each pixel

Measure: Calibration with Am source

Calibration with 60 KeV γ (Americium source)
Standard Floating Zone p-type sensor 300 μm thick,
size: 50μm x 425 μm



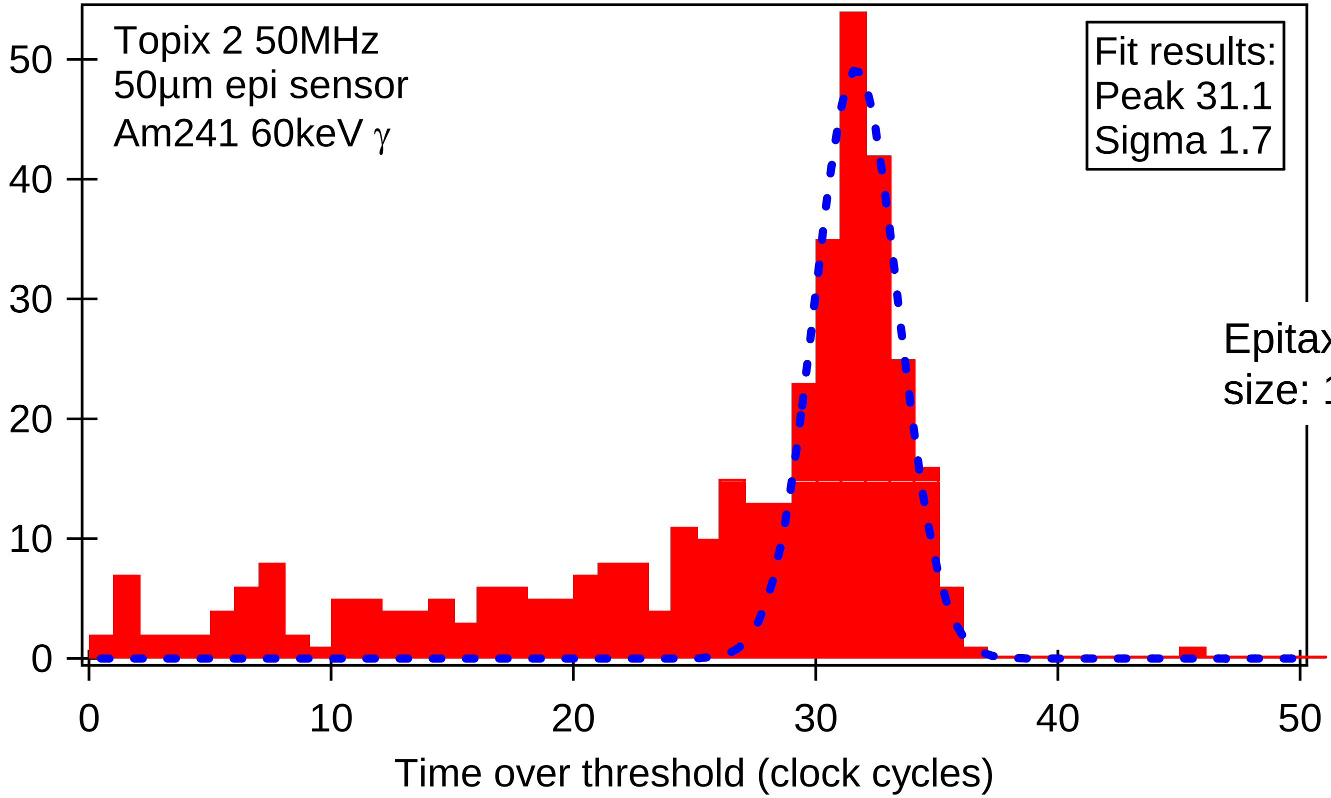
$$n^\circ \text{ of } e^- h \text{ pairs} = \frac{E_\gamma}{E_{ion}} = \frac{60 \text{ keV}}{3.6 \text{ eV}} = 1.67\ 10^4$$

$$Q_{in} = n^\circ \text{ of } e^- h \text{ pairs} * e = 1.67\ 10^4 * 1.6 * 10^{-19} \text{ C} = 2.67 \text{ fC}$$

$$\text{ToT (clk)} * \text{tail slope (V / clk)} = Q_{in} * \text{Preamp\_Gain} = 11.1 \text{ mV}$$

Expected value: 11.1 mV
Good response

First spectra with an epi-sensor



Epitaxial sensor 50 µm thick, size: 125µm x 325 µm

- Signal to noise ratio is limited by parasitics capacitance due the external connections
- Bonding pad+wirebonding+protection diodes

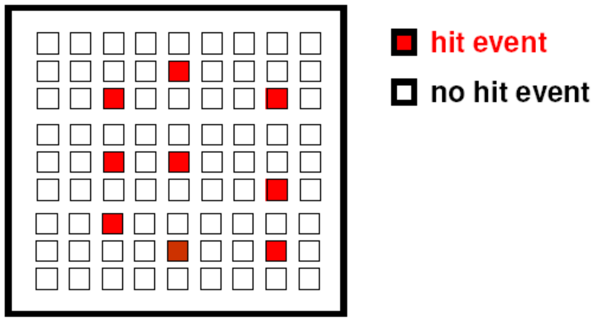
ToT for strips

- Could the ToT architecture of ToPix be suited for the read-out of the strip detector?
- Advantages:
  - Possible sharing of digital read-out and DAQ
  - Digitization with low power consumption
  - Since we have more area available (100u x 400u) we can improve the performances of the ToT stage

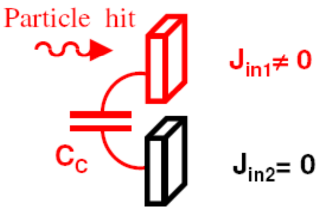
Why we can't use ToPix for the strip readout

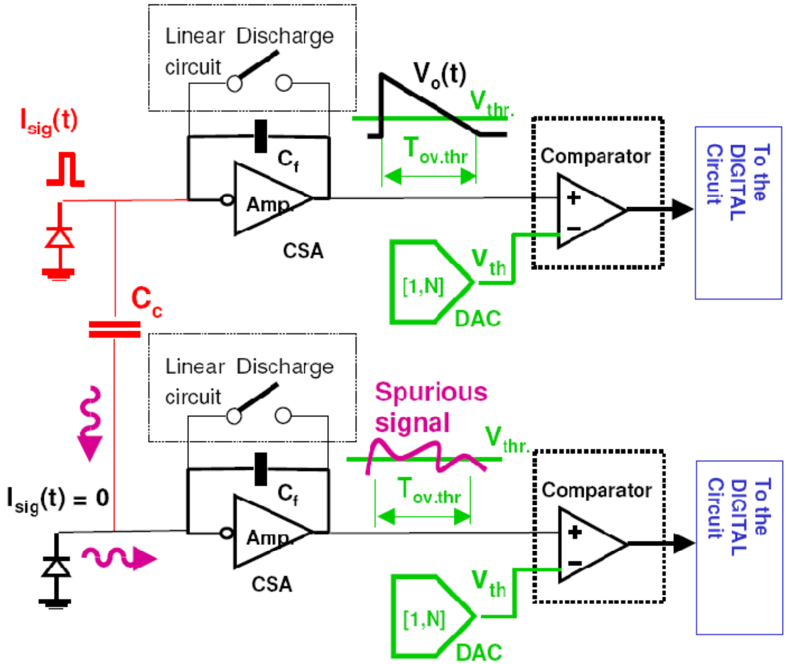
- The strip sensor has a large capacitance (Cd=20pF) -> Cross Talk

Pixel Matrix



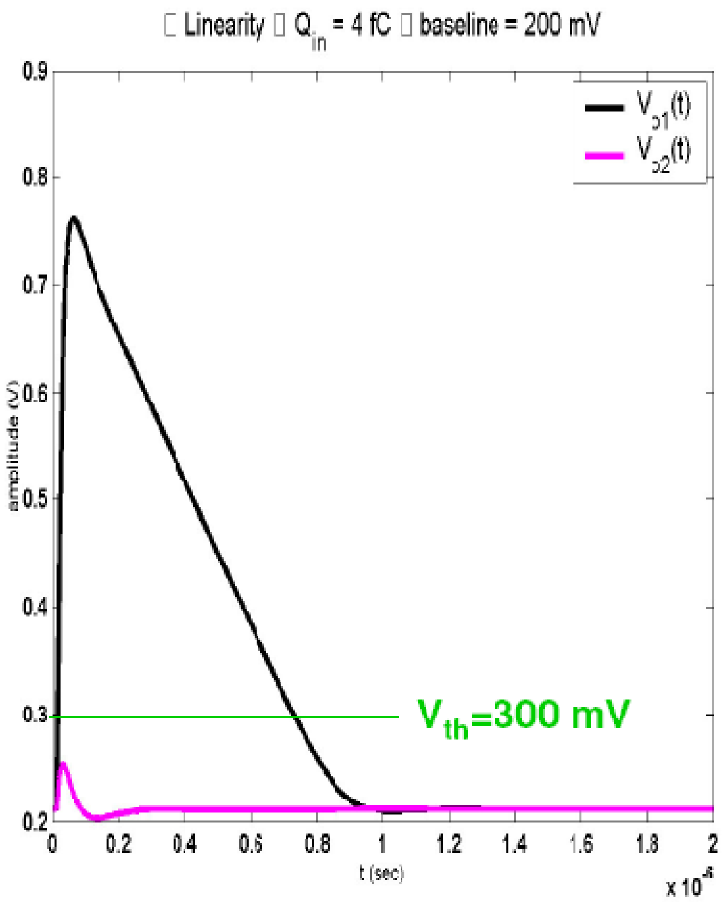
Adjacent Coupled Detectors

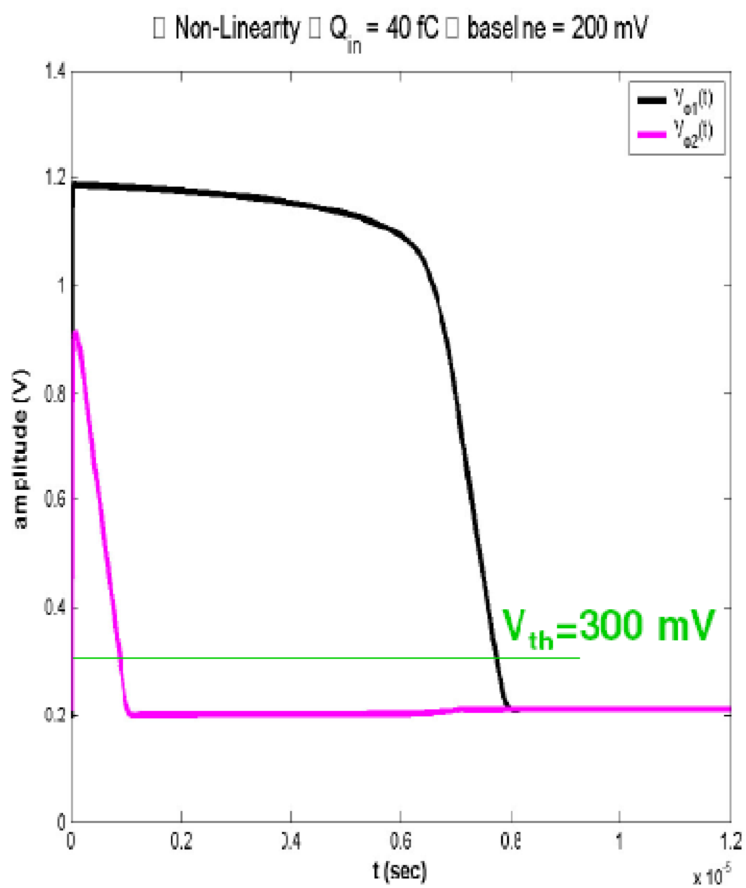




Saturation and cross-talk

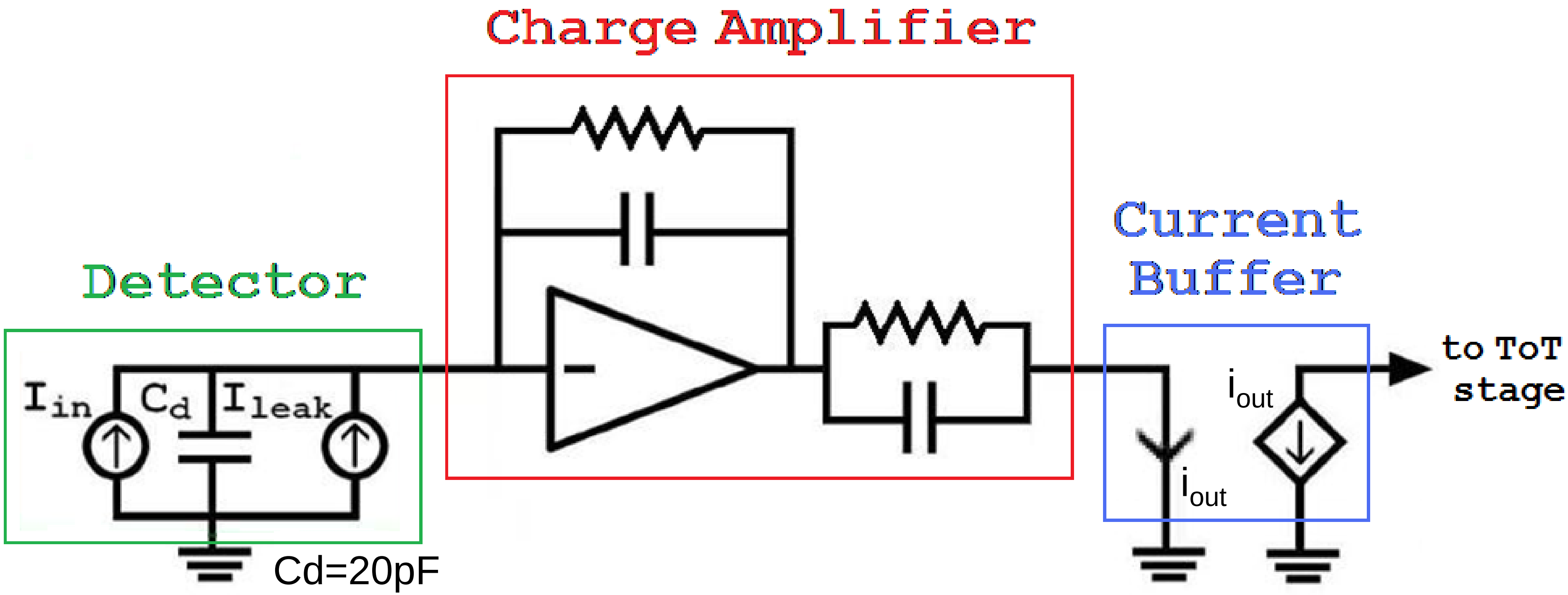
- Effect of the input capacitance on the cross talk





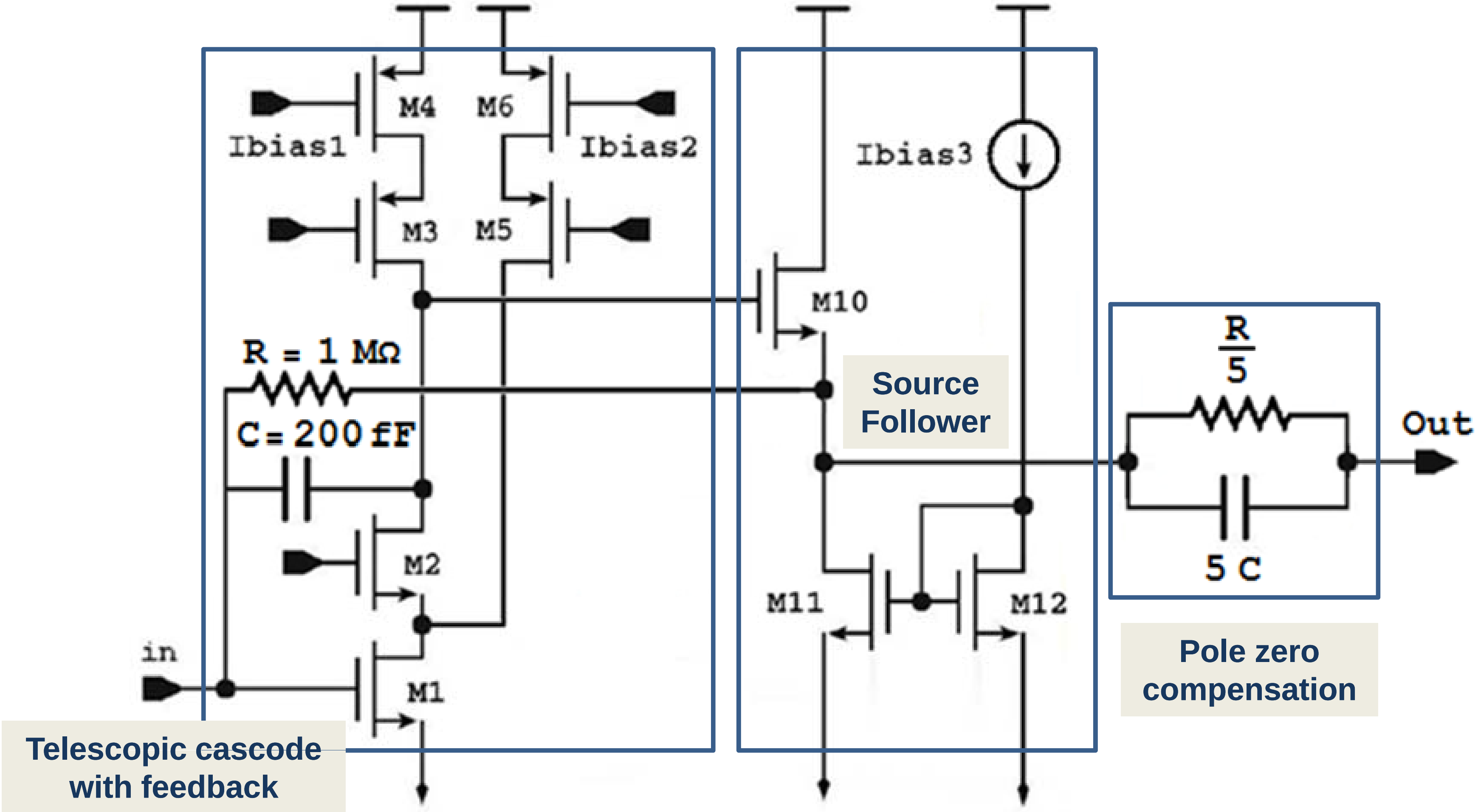
Read-Out Architecture

- Current amplifier to decouple the detector from the ToT stage input node
- Current buffer
- Improved ToT stage

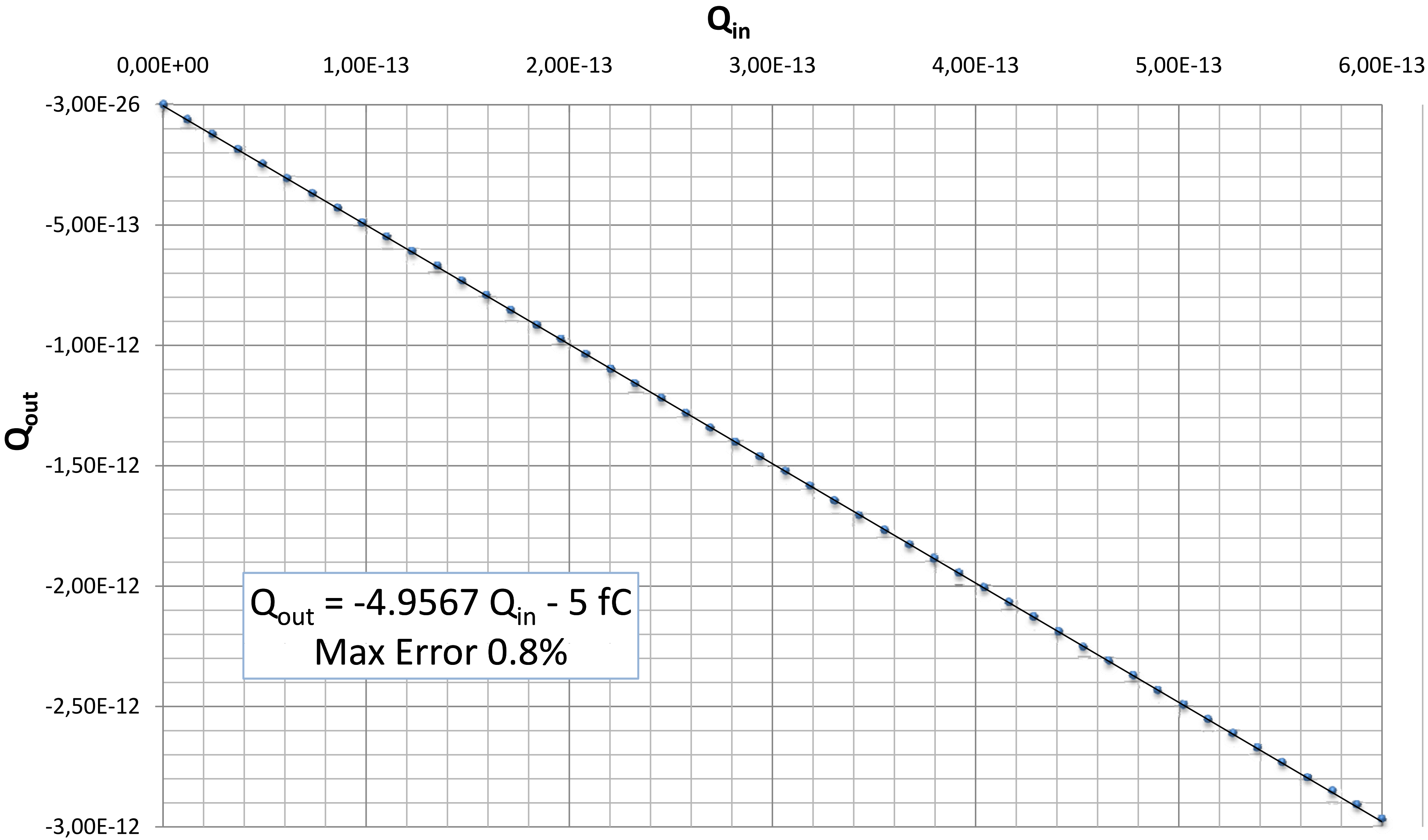


Charge Amplifier

- Charge amplifier: standard configuration with pole-zero compensation.
- 30MHz bandwidth, charge gain of 5 and power consumption of 300uW.

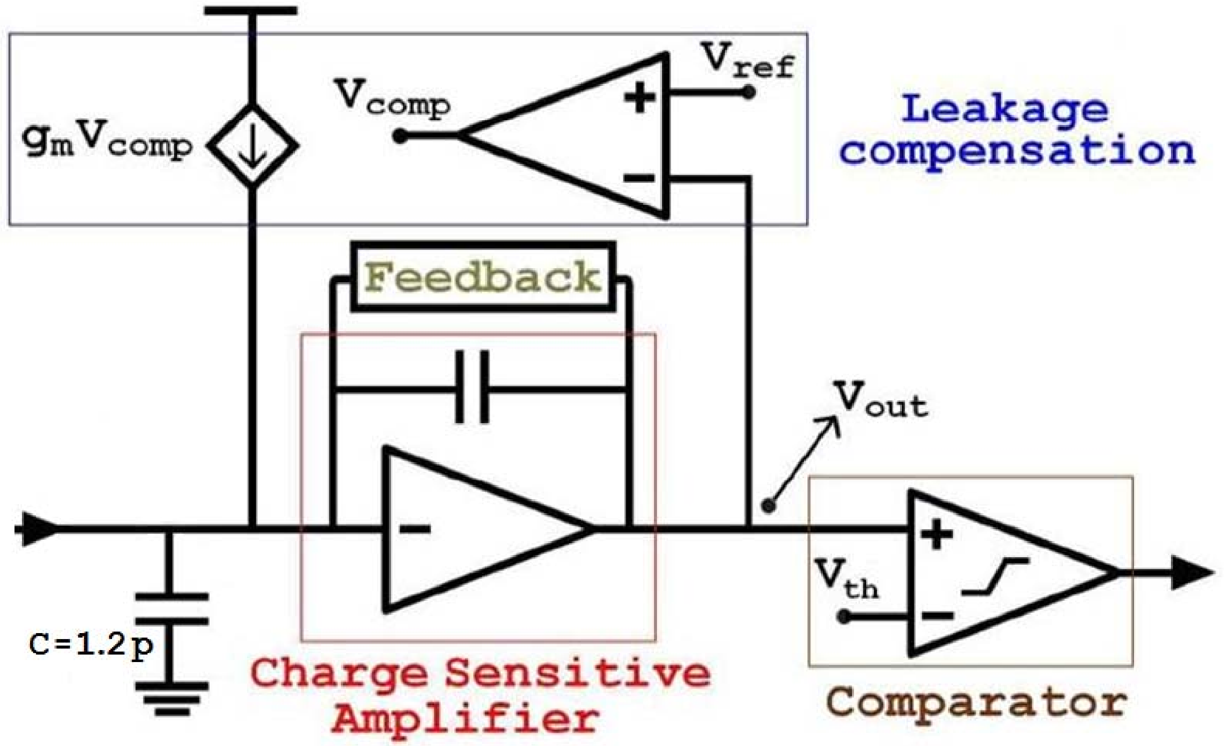


Charge Amplifier - Linearity

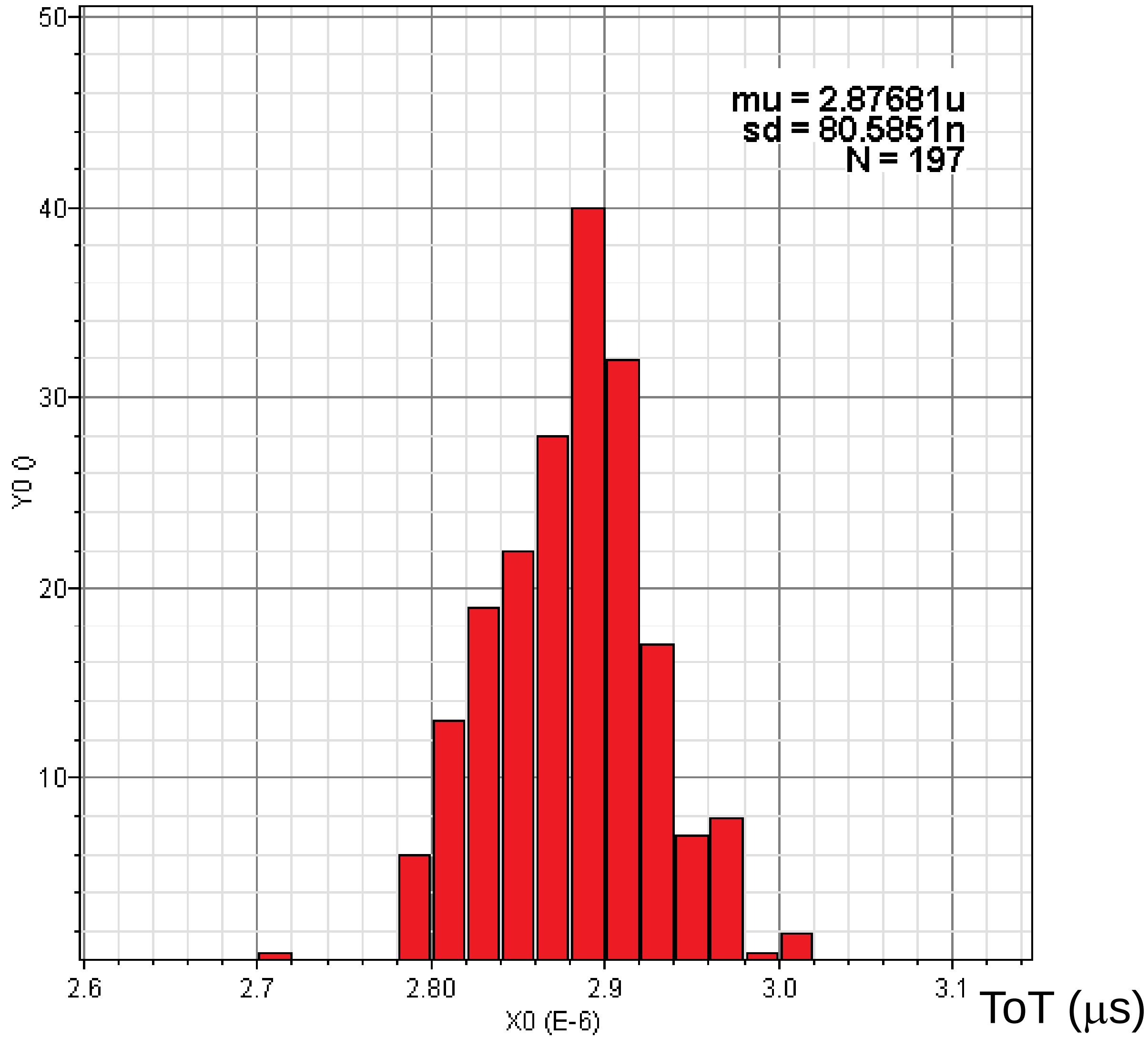


ToT stage

- Same architecture of Topix 2.0
- Improvements:
  - 25 nA discharging current
  - Larger transistors to reduce the channel to channel ToT variation due to mismatch effects.



ToT dispersion



Q_{in} = 43.15 fC

I_{dis} = 160 nA

ToT dispersion: 2.8%

Why we need a current buffer?

$$i_r = \frac{\Delta v}{R_{out}} \qquad \text{If } R_{out} = \infty \rightarrow i_r = 0$$

If $R_{out} \neq \infty$

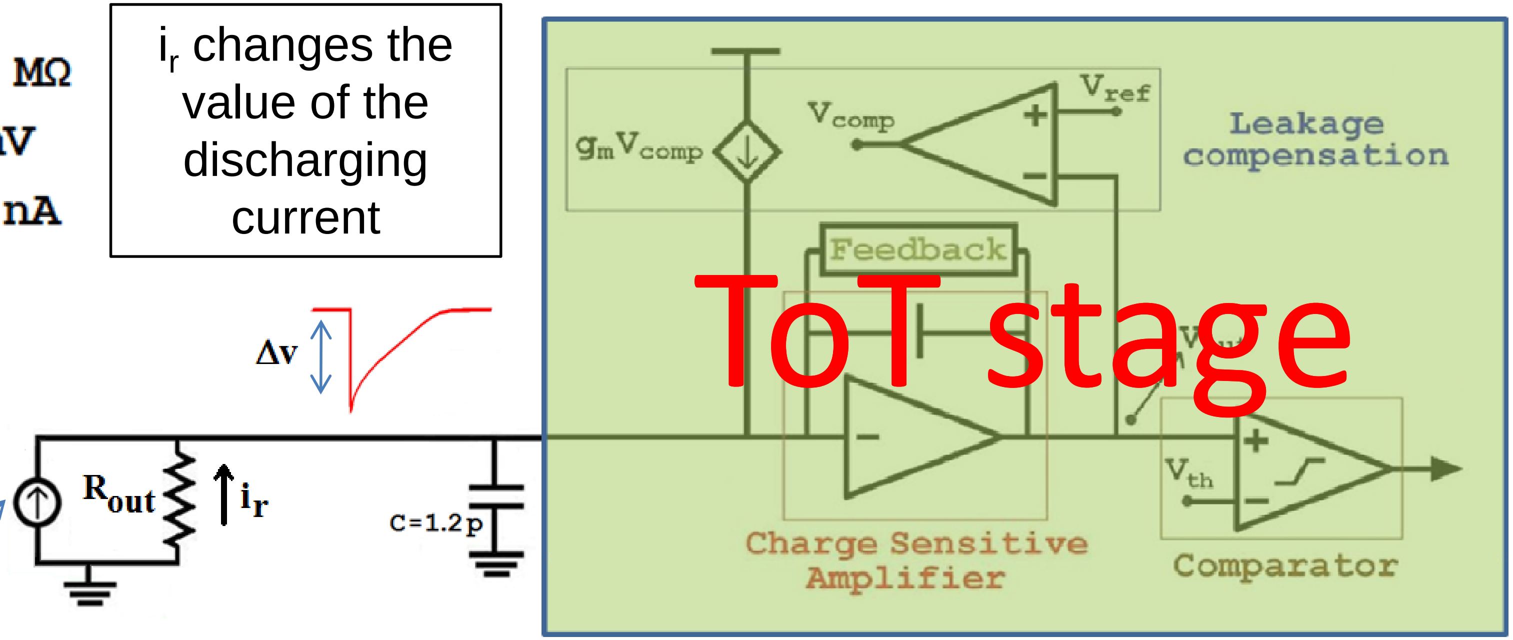
$R_{out} = 10\ M\Omega$

$\Delta v = 50\ mV$

$\rightarrow i_r = 5\ nA$

i_r changes the value of the discharging current

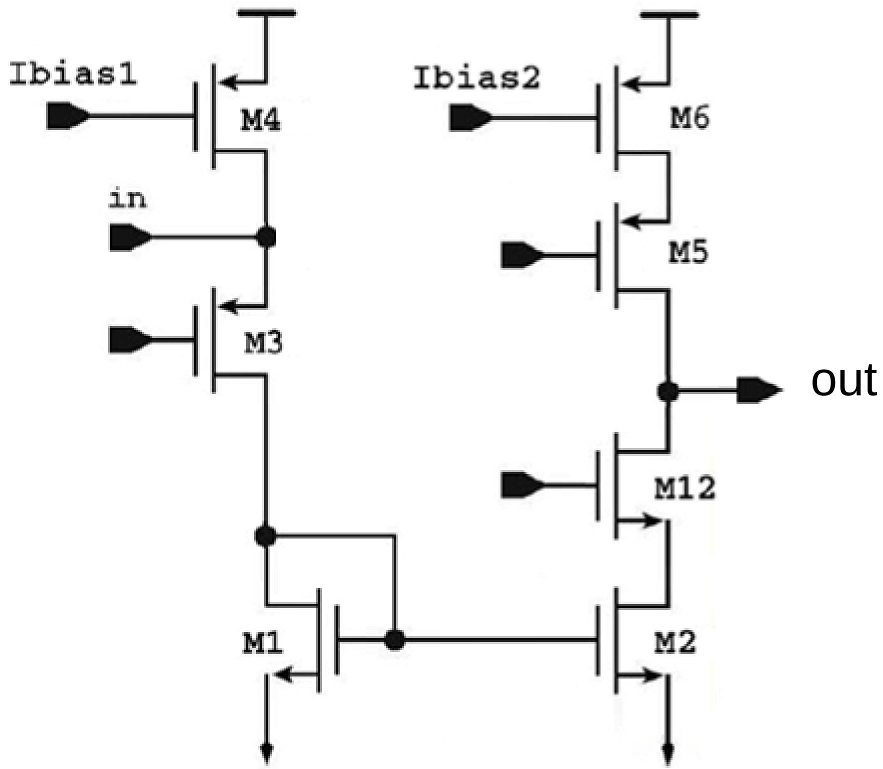
Current from the charge amplifier



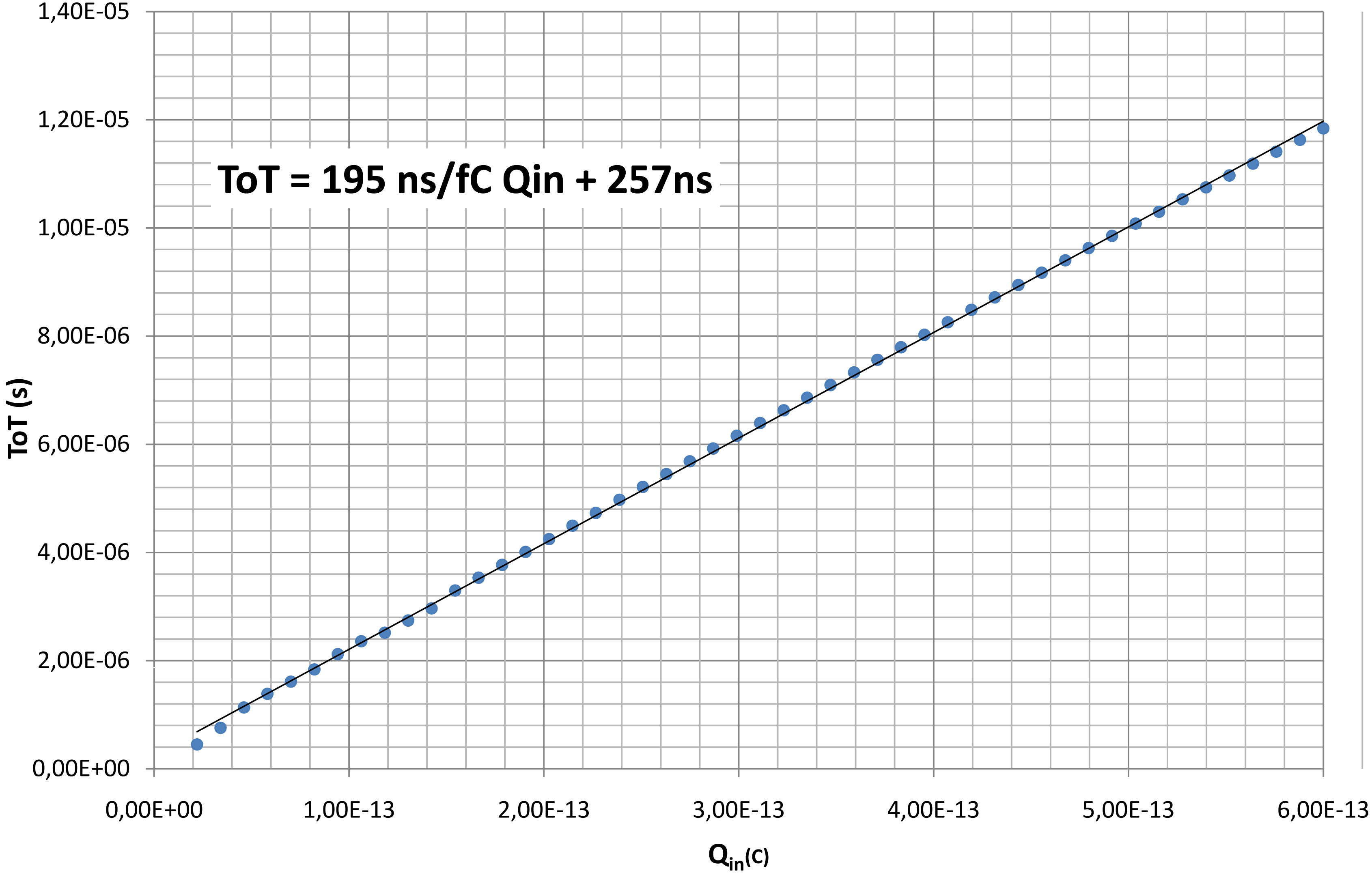
Since the charge amplifier output resistance is low, the ToT stage has to be connected with a current buffer with a high output resistance

Current Buffer: first design

- The current buffer is employed to connect the current amplifier to the ToT stage with a high output resistance



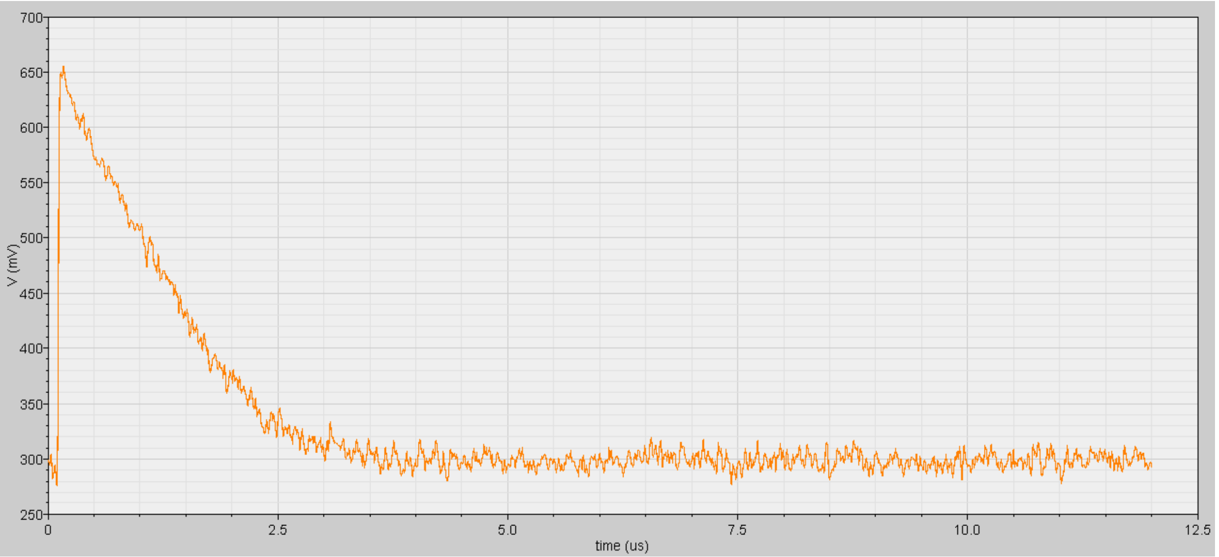
Full chain simulation: ToT linearity



Full chain simulation: Transient noise

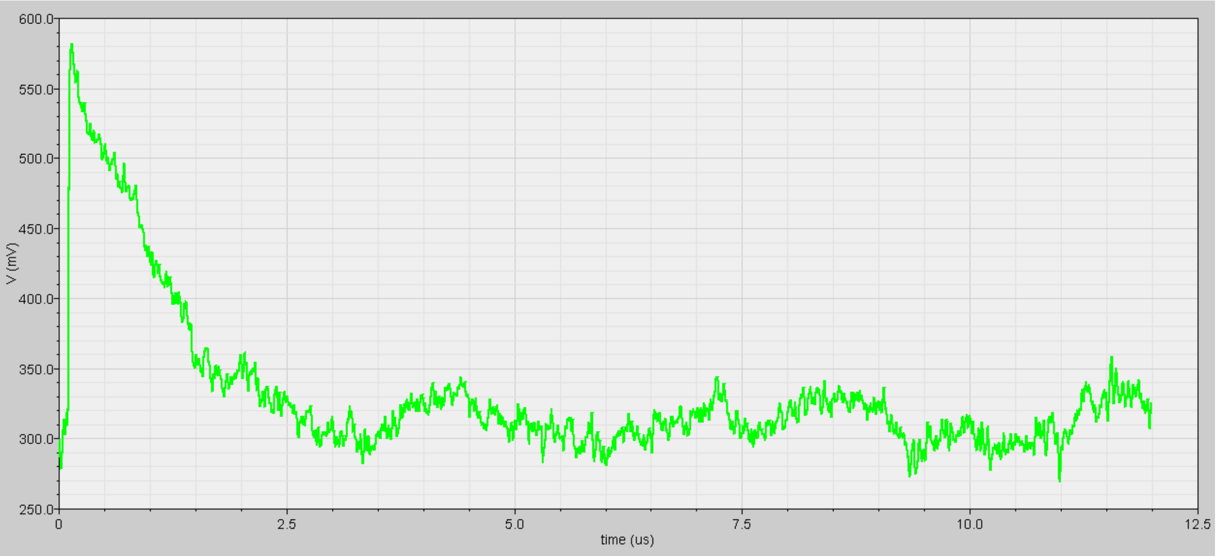
Ideal Current Buffer

Qin = 10fC
Noise = 8.7mV rms
Charge noise 0.25fC (1300 e^-)
Power: 350uW



Actual Current Buffer

Qin = 10fC
Noise = 18 mV rms
Charge noise 0.51fC (2678 e^-)
Power: 370uW



Conclusions and Outlook

From first simulations no major show stoppers.

Critical issue: coupling between preamplifier and ToT stage (impact on noise and linearity).

Next step: design of an improved current buffer.