MVD pixel layout proposal

- Philosophy
  - design pixel sensor modules to optimise forward coverage, then adjust barrel design as a result
  - only one variable: chip size
  - small production so sensors must fit on 4” wafers

Small disks (1,2)

Inner diameter
22 mm

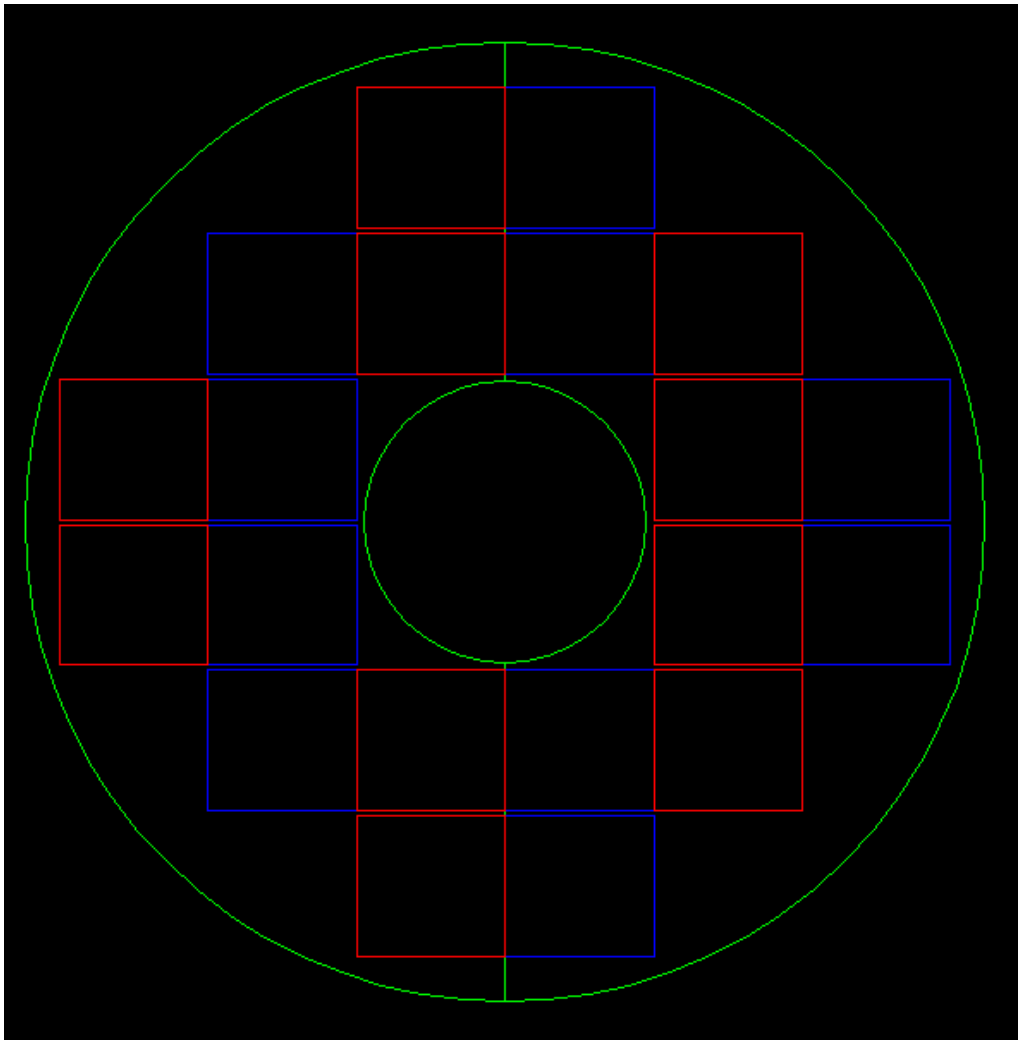
Outer diameter
75 mm

Alternate front and back

Zero overlap

Horizontal zero gap

Vertical gaps bridged with longer pixels



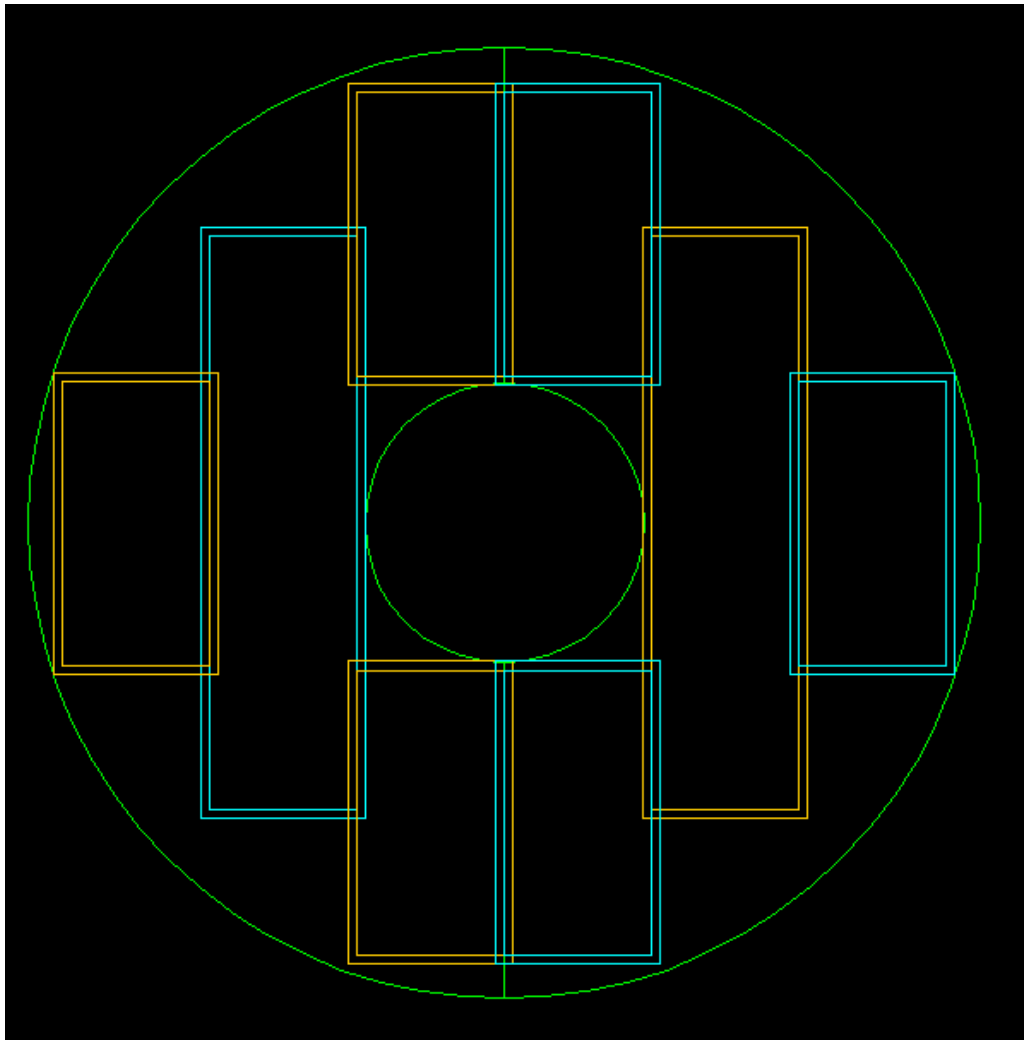
Pixel active area
11.6 x 11.0 mm

Red rectangles: pixel active area on front of disk

Blue rectangles: pixel active area on back of disk

Small disks (1,2)

Some sensor overlap due to dead space (conventional guard design)



Total coverage 65%

Services must in any case stay within the outer diameter limit

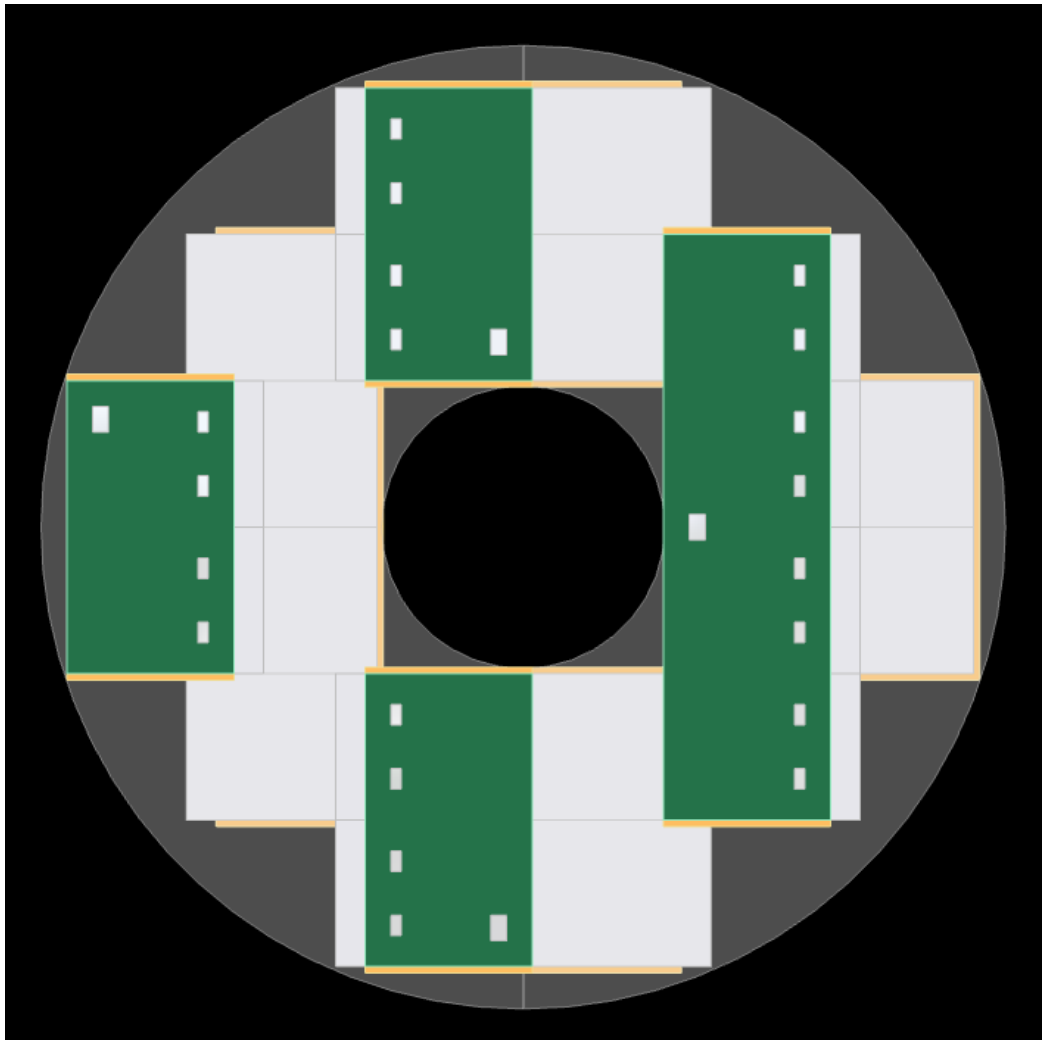
Small disks (1,2)

Schematic sensor modules with full chip size and minimal SMD components

Two module designs:

2-chip x 6

4-chip x 2



Nominal pixel chip size

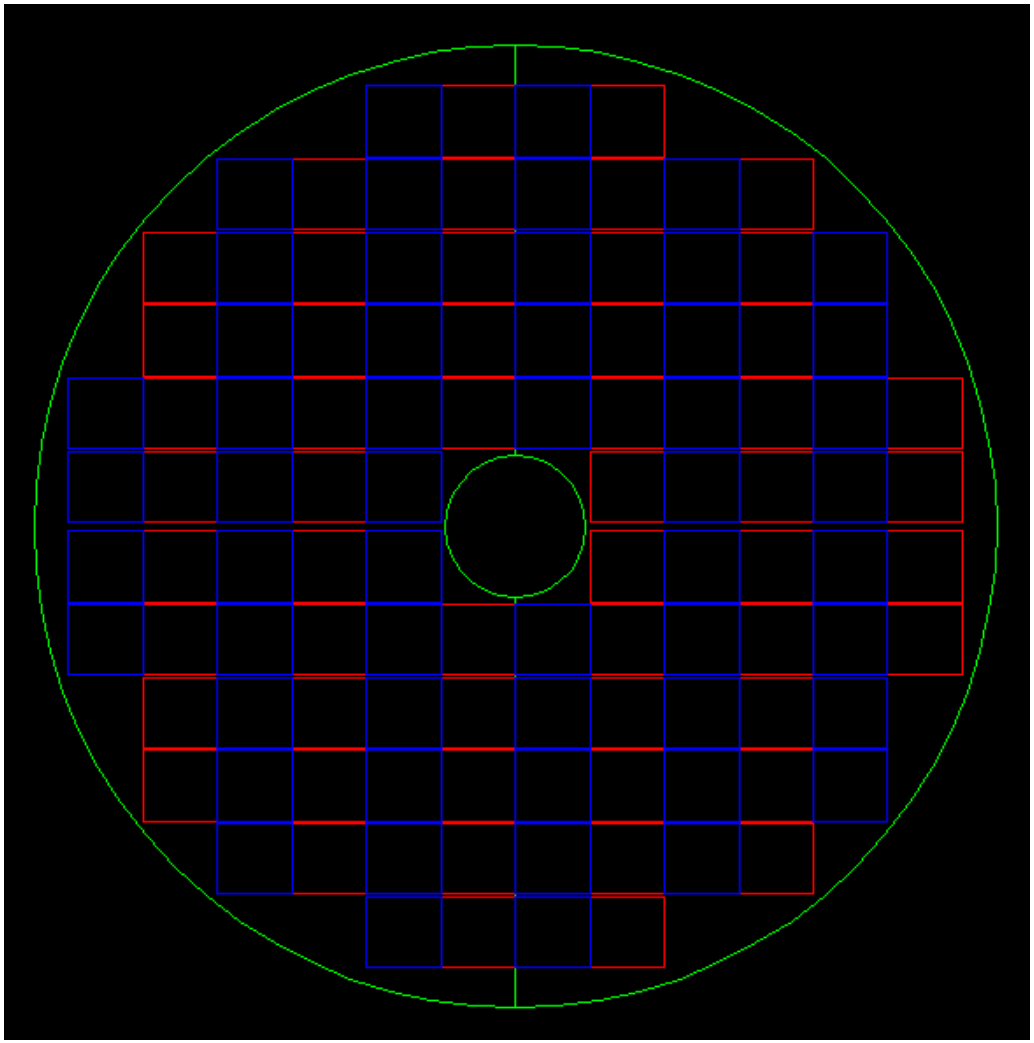
14.8 x 11.4 mm

(in reality slightly less to include dicing tolerances)

Large disks (3-6)

Inner diameter
22 mm

Outer diameter
150 mm

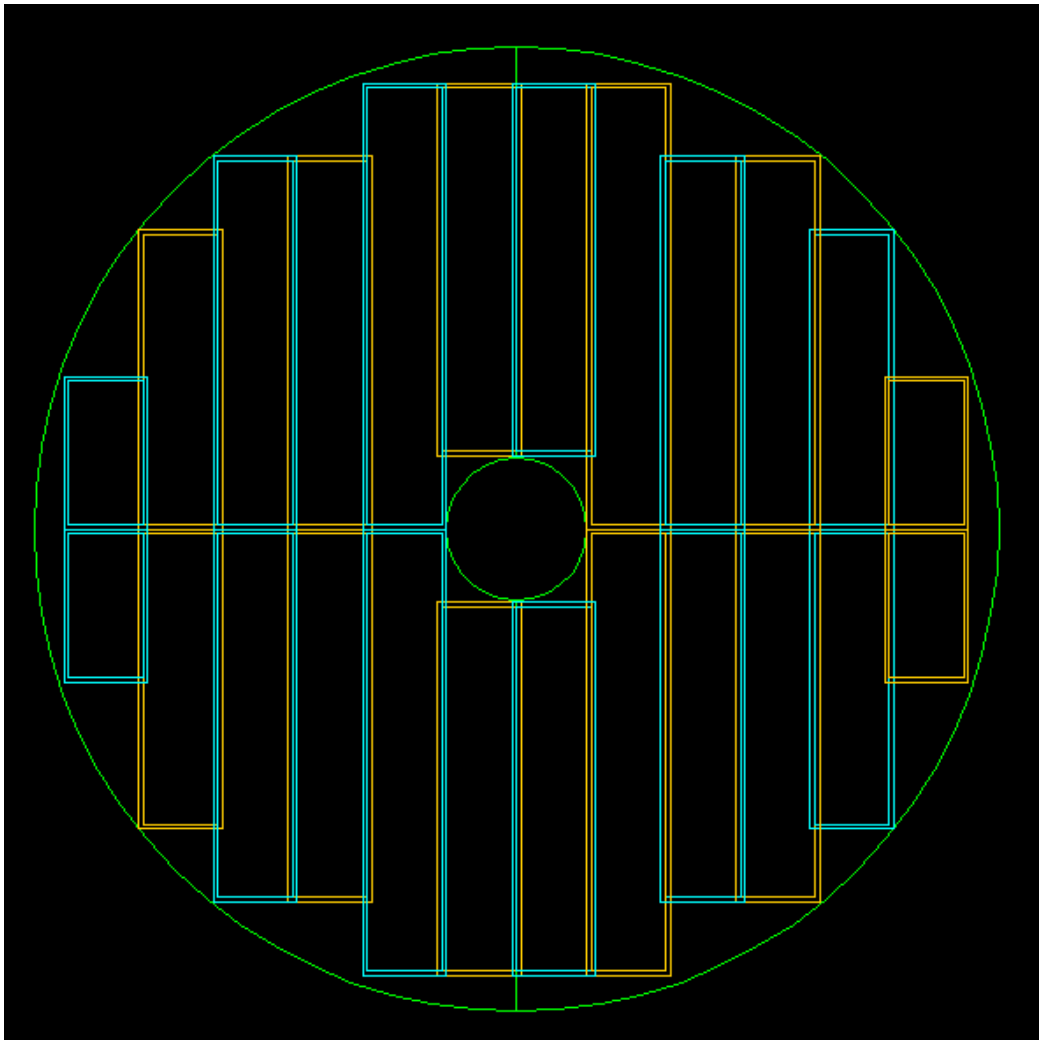


Red rectangles:
pixel active area
on front of disk

Blue rectangles:
pixel active area
on back of disk

Large disks (3-6)

Small dead zone (1.4 mm) where two sensors meet



Total coverage 82%

Again services must stay within outer diameter limit

Large disks (3-6)

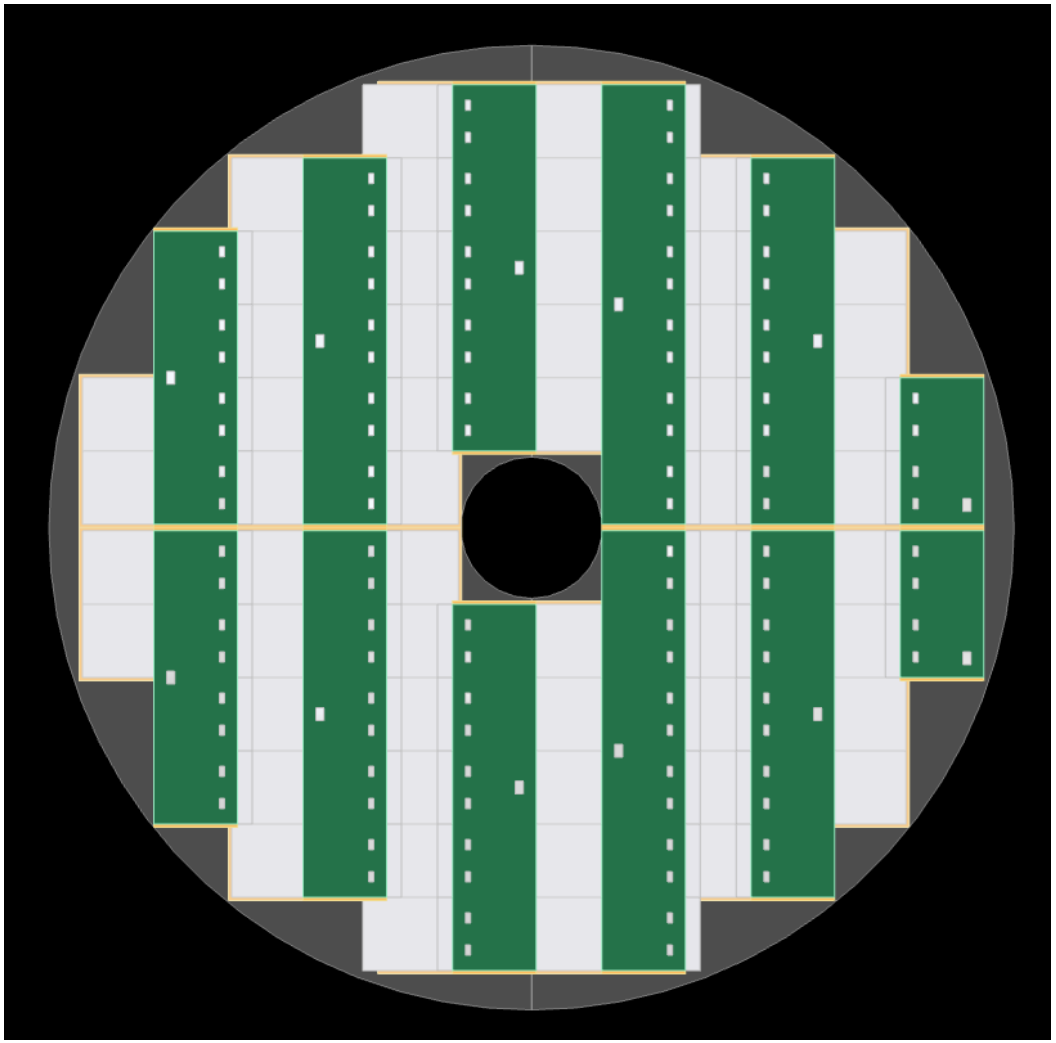
Four module designs:

2-chip x 4

4-chip x 4

5-chip x 12

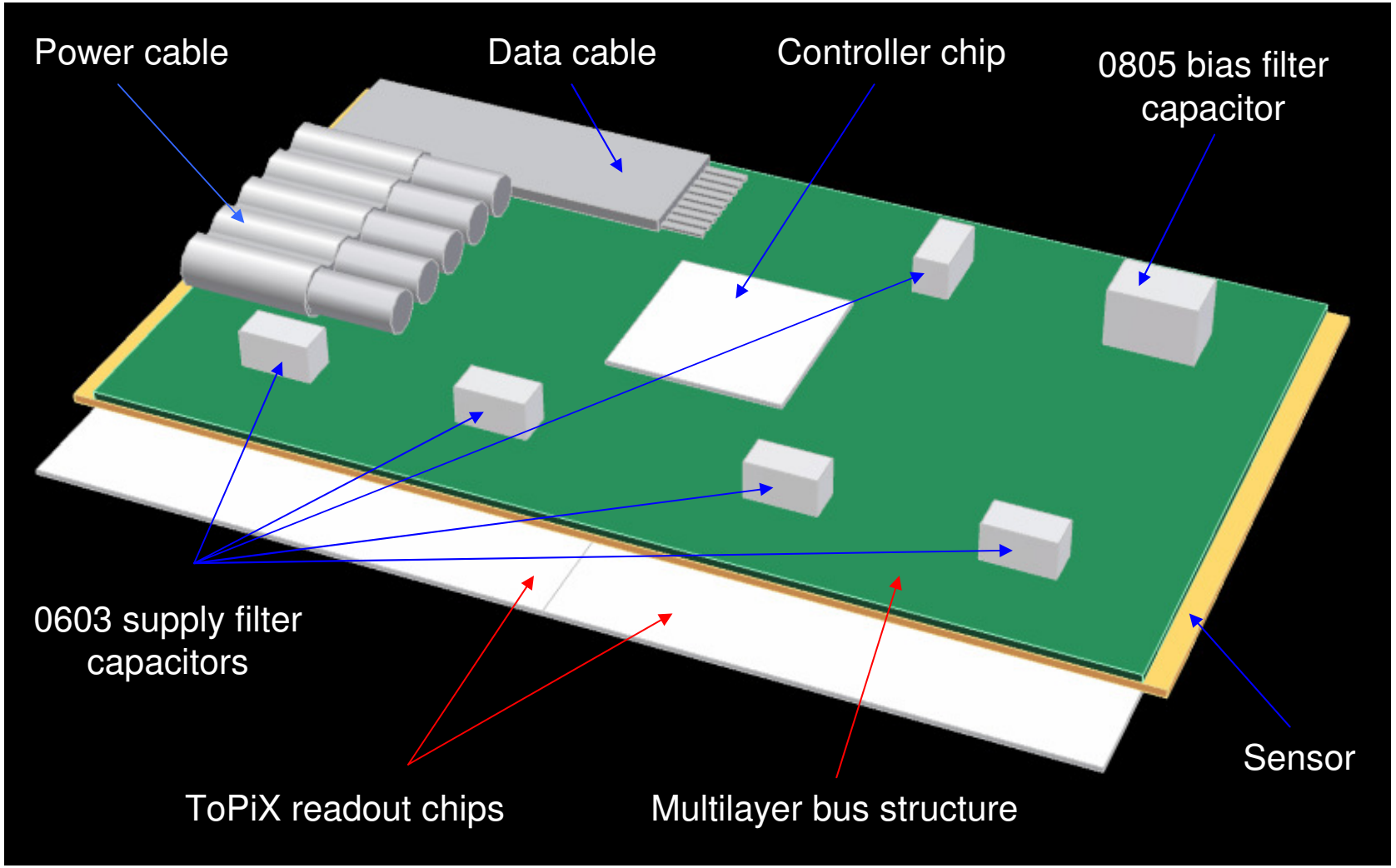
6-chip x 4



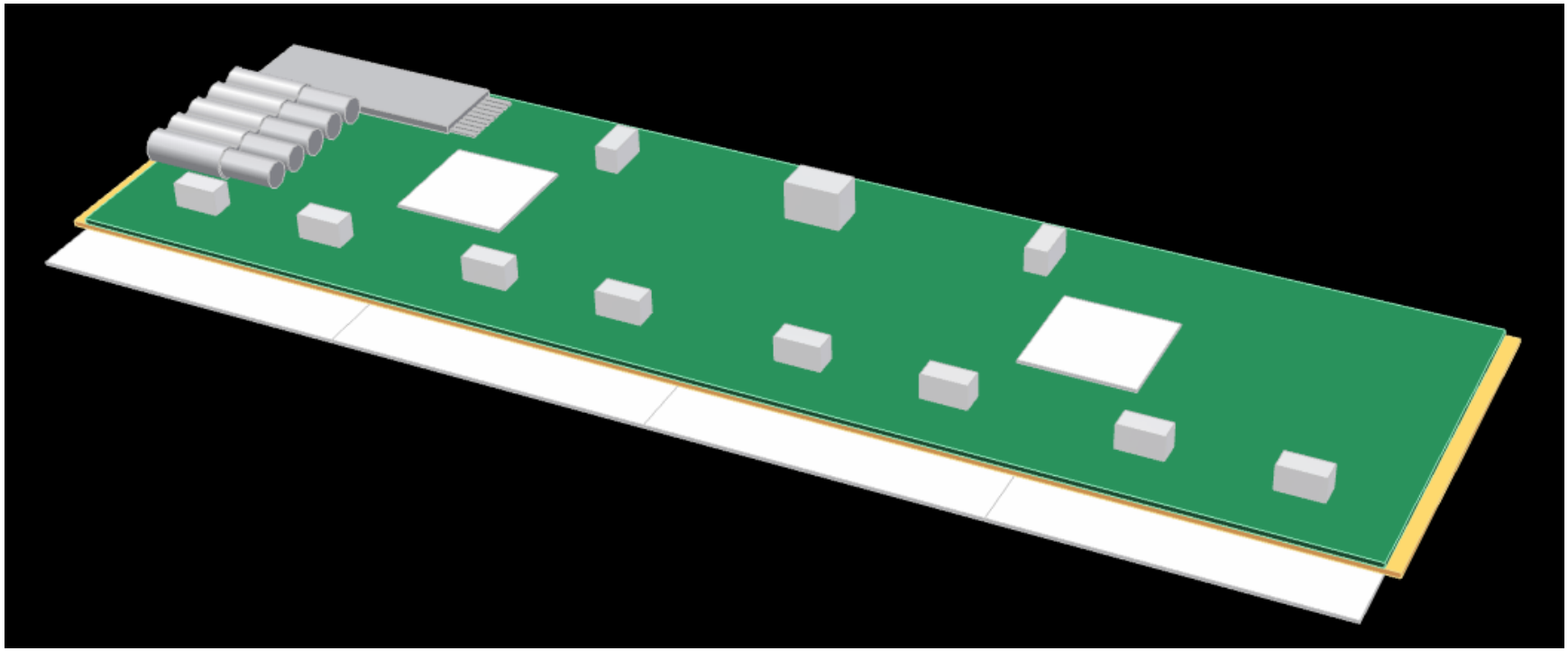
MVD pixel module concept

- Disk service routing limitations rule out ALICE-style bus with electronics and external connections outside the active region
  - choose ATLAS/CMS style
- Pixel modules must transmit Gbit data to outside
  - risky to put directly into pixel chips
    - add piggy-back controller chip to module
- Conversion to optical complex, also likely to require multiple ASIC's
  - at least first part of transmission by cable

2-chip module

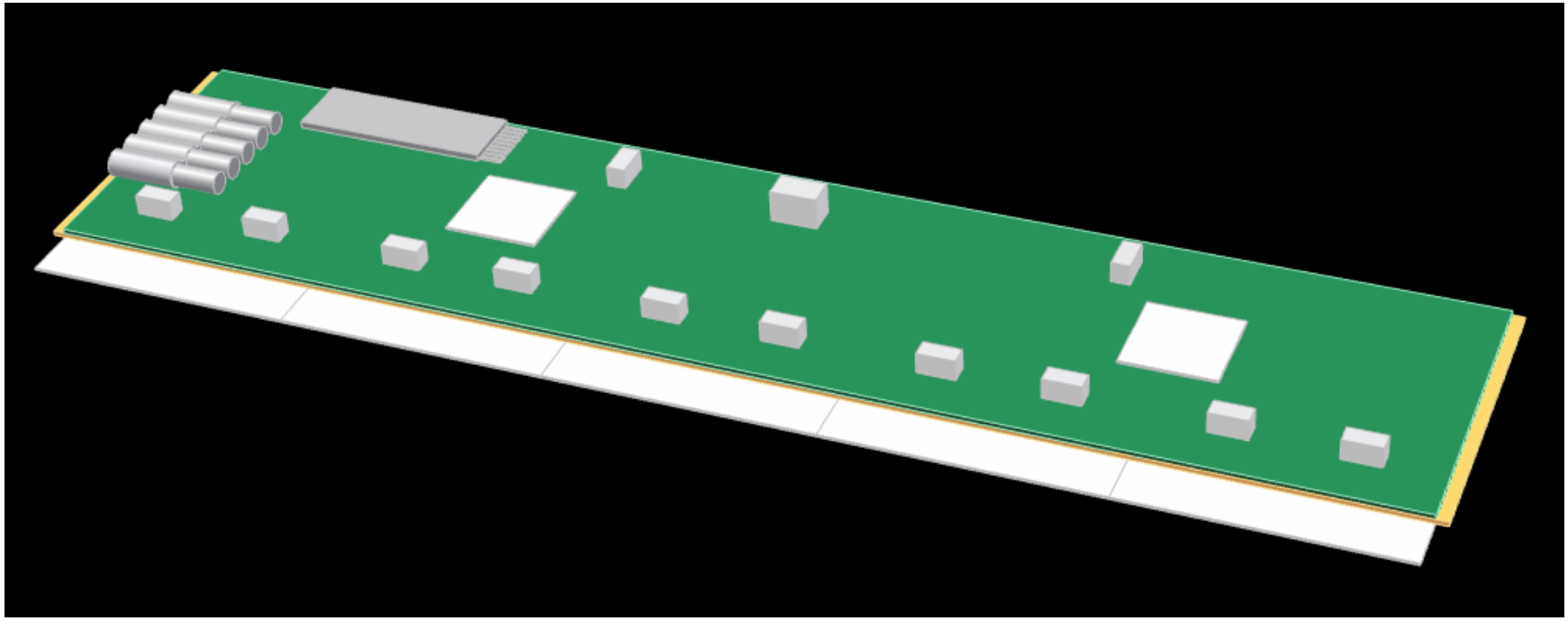


4-chip module



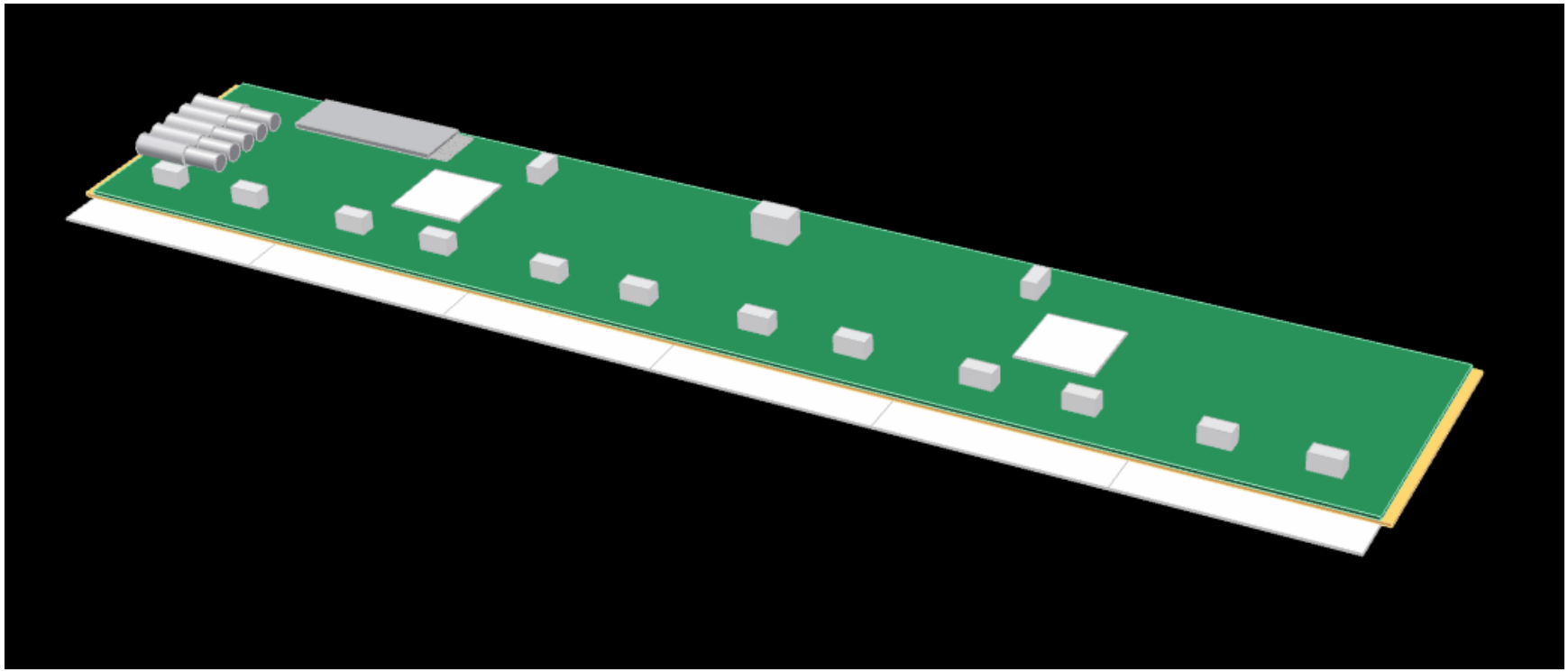
Possibility of daisy-chaining controllers to save on cables (where data rates allow)

5-chip module



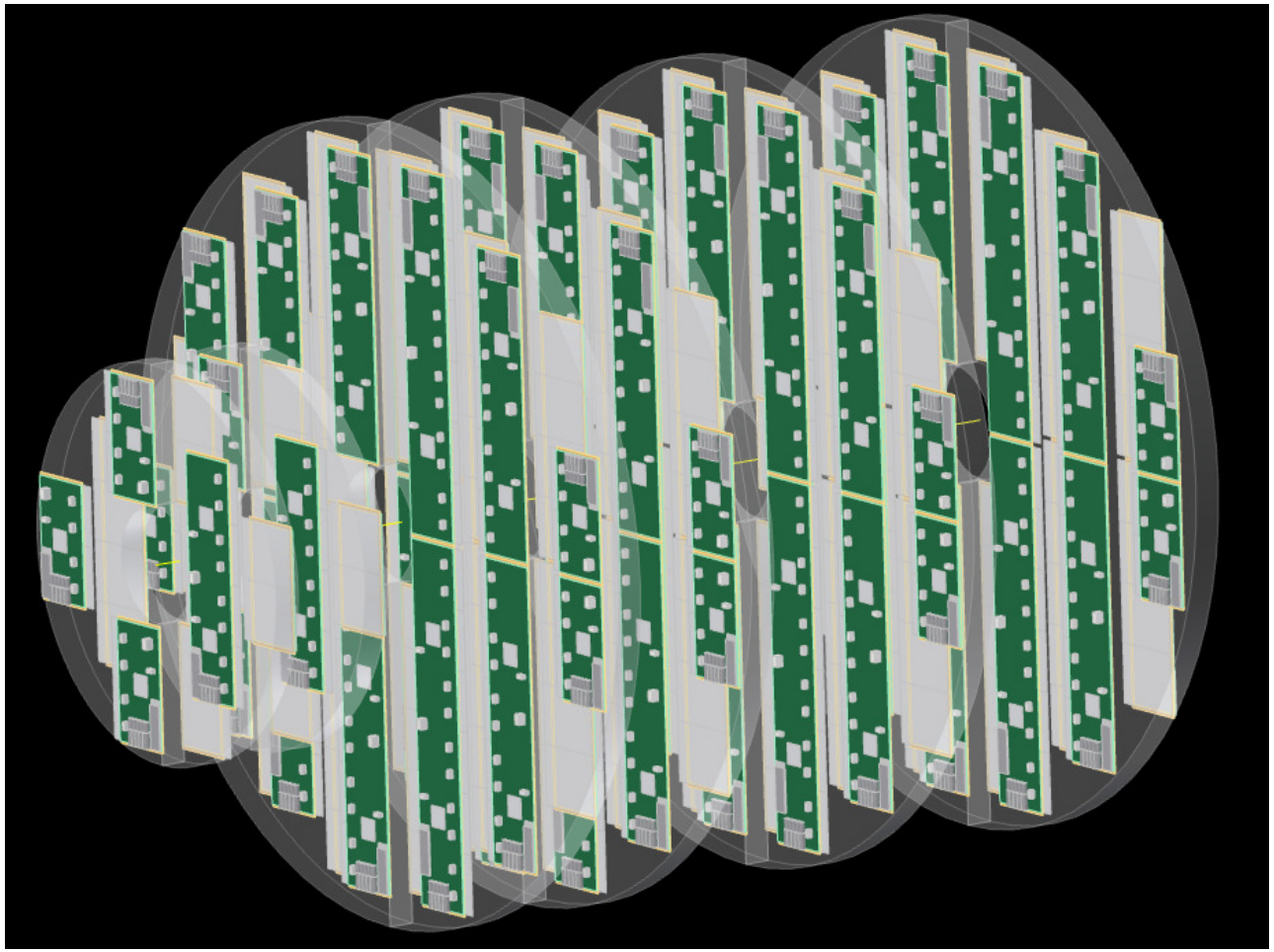
Controller chips serve two or three ToPiX readout chips

6-chip module



For outer layer of barrel would need to daisy-chain two 6-chip modules (power and controller chips) to keep cables out of active region

Complete forward assembly



Keeping cables out of active region means that some modules may require two designs according to which end the cables have to be connected