Update of BWEC Activities

Oliver Noll

$\bar{\text{P}}$ANDA-Collaboration Meeting 17/2

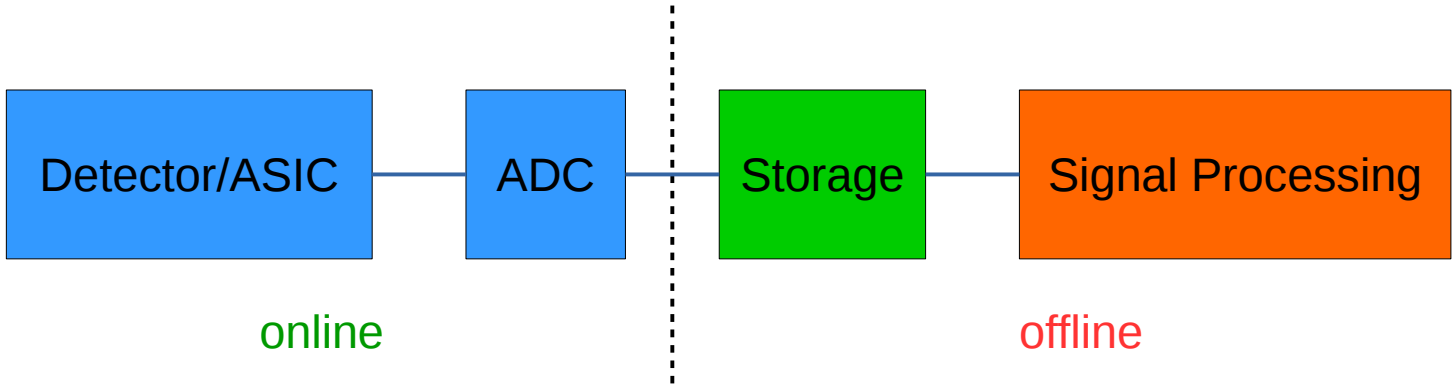
June 2017

APFEL ASIC Feature Extraction

Feature Extraction (FE) for APFEL ASIC Pulses (offline)

Past

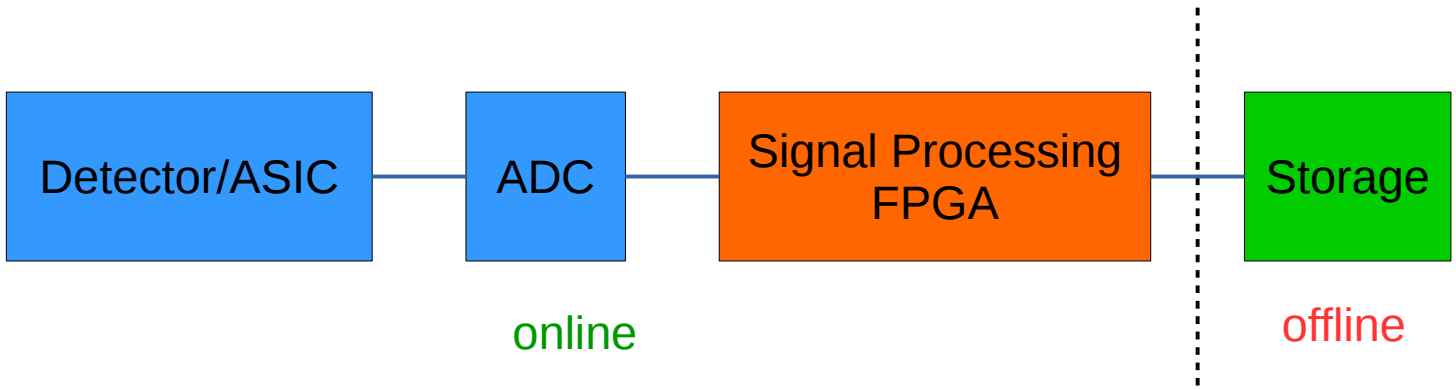
- FE for APFEL ASIC Pulses (Software,C++) ✓
- Parameter optimisation with beam data ✓
- Noise hit studies ✓



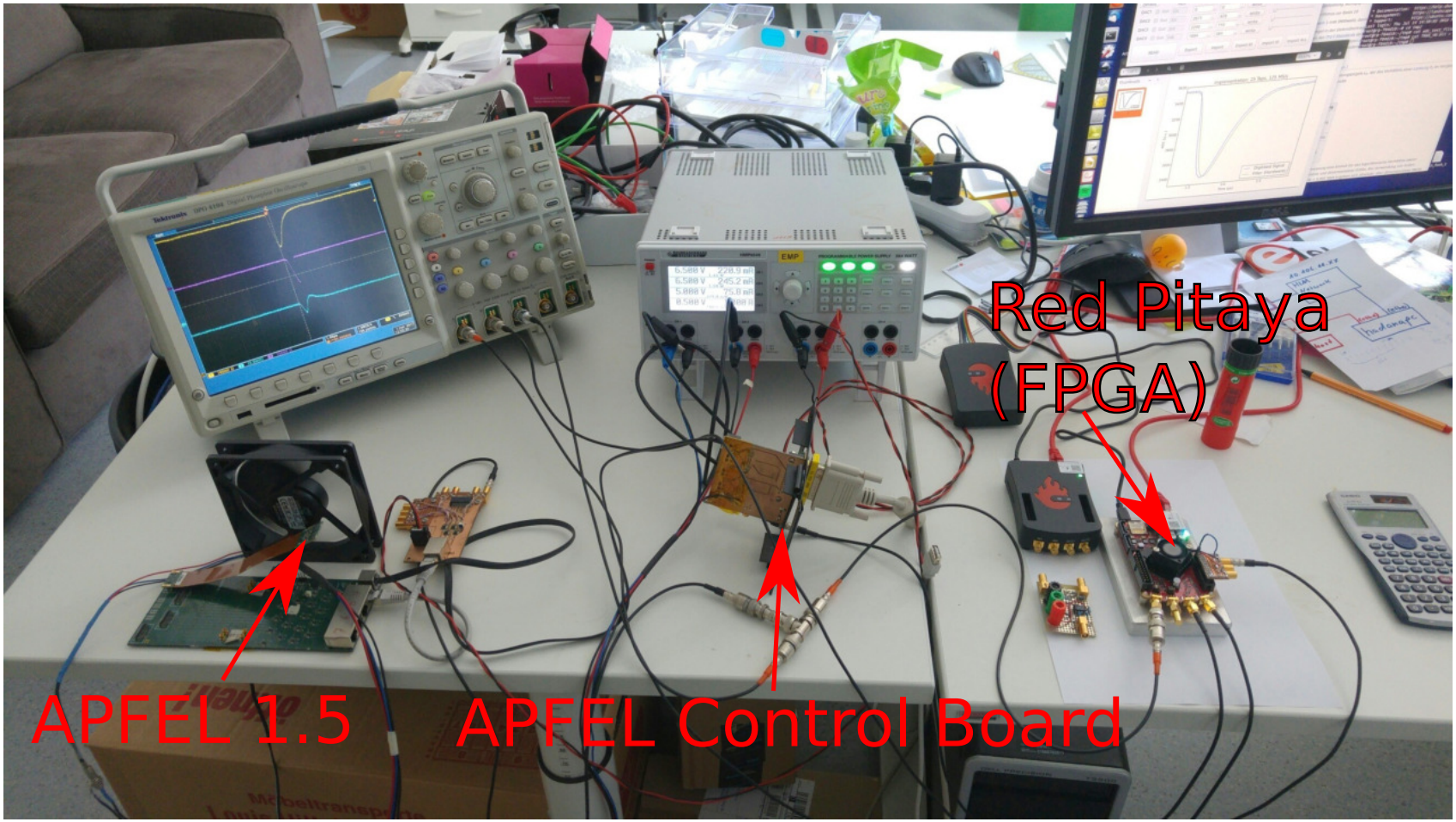
Feature Extraction (FE) for APFEL ASIC Pulses (online)

Now

- First implementation of FE on FPGA (Verilog) ✓
- Optimisation of smoothing procedure ✓
- Running on Zynq FPGA (Red Pitaya) ✓
- Transfer to $\bar{\text{P}}$ANDA ADC/FPGA ongoing



FE - Setup (FPGA)



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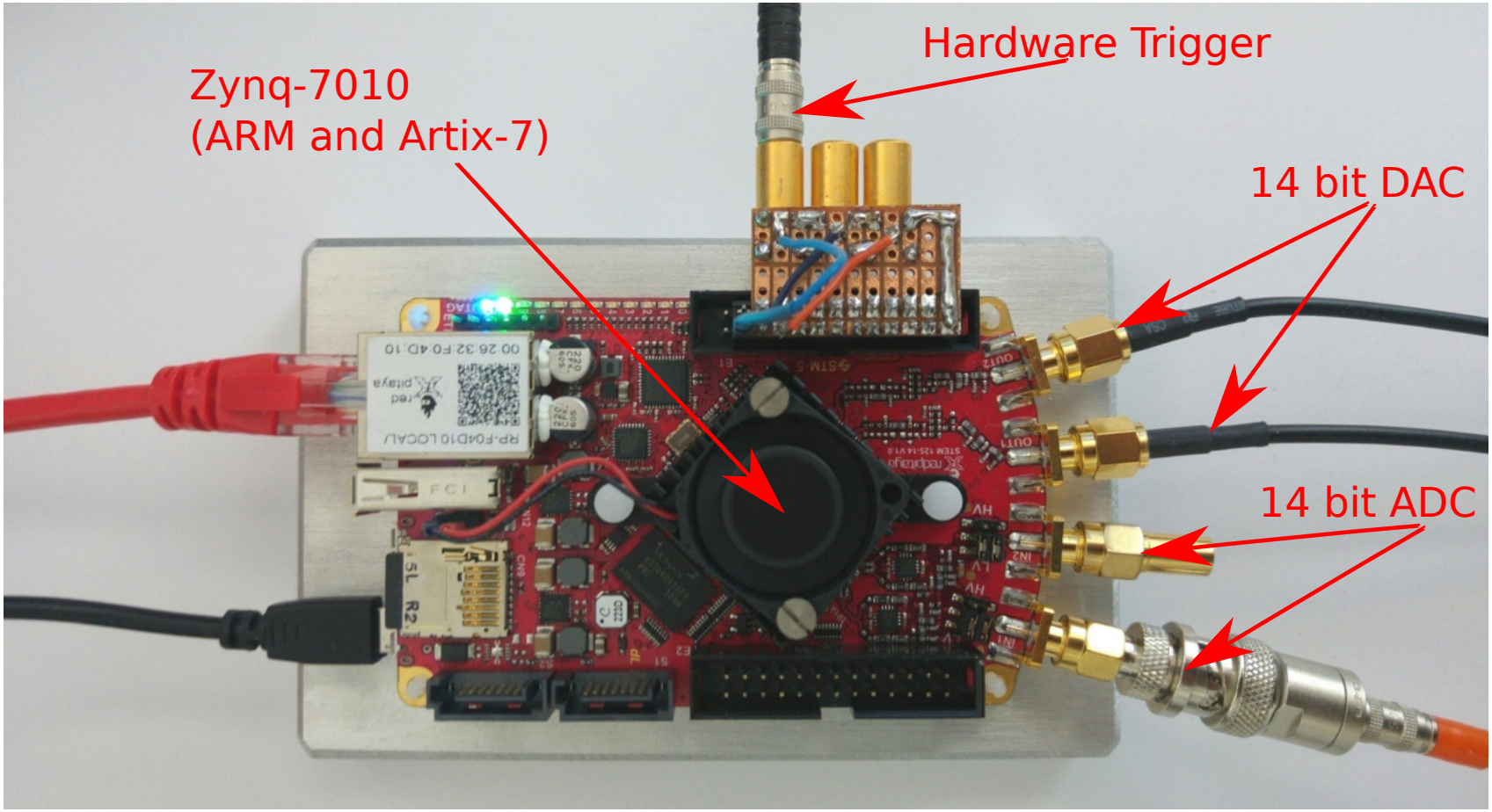
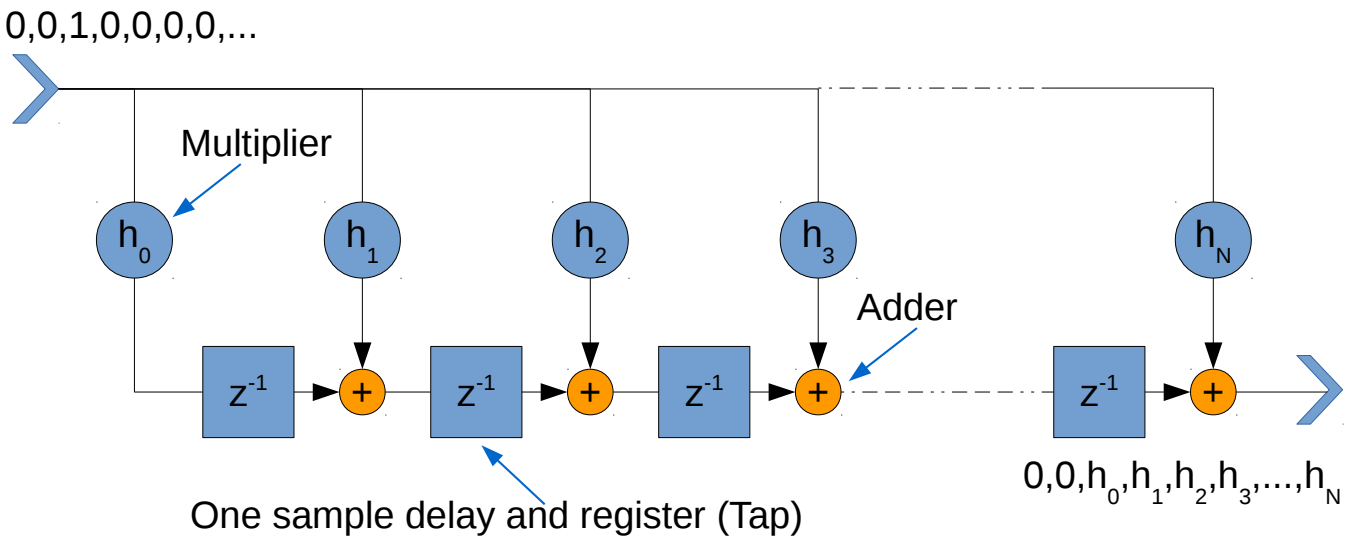


FE - Smoothing via Finite Impulse Response (FIR) Filter

Idea

- Transfer function which suppresses undesired signal frequencies
- $H(z) = \sum_{j=0}^{N} h(j) \cdot z^{-j}$ (Z-transformation of impulse response)
  - $h(j)$: filter coefficients
  - $z = e^{i\omega}$ with $\omega = 2\pi f / f_s$ (f_s : sampling rate)
- Each output value is weighted sum of most recent input values
- $\mathbf{out}[n] = h_0\mathbf{in}[n] + h_1\mathbf{in}[n-1] + \ldots + h_N\mathbf{in}[n-N]$



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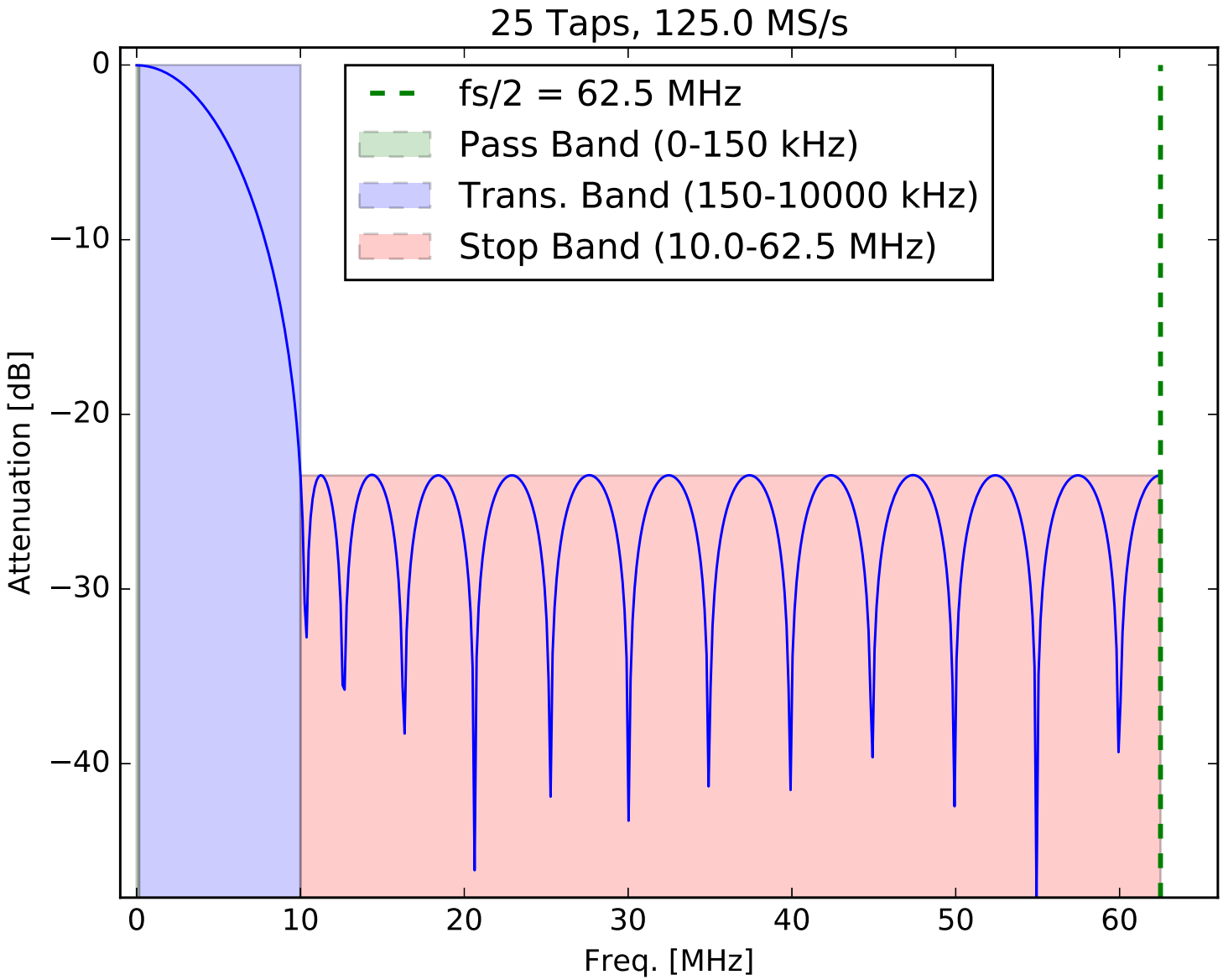

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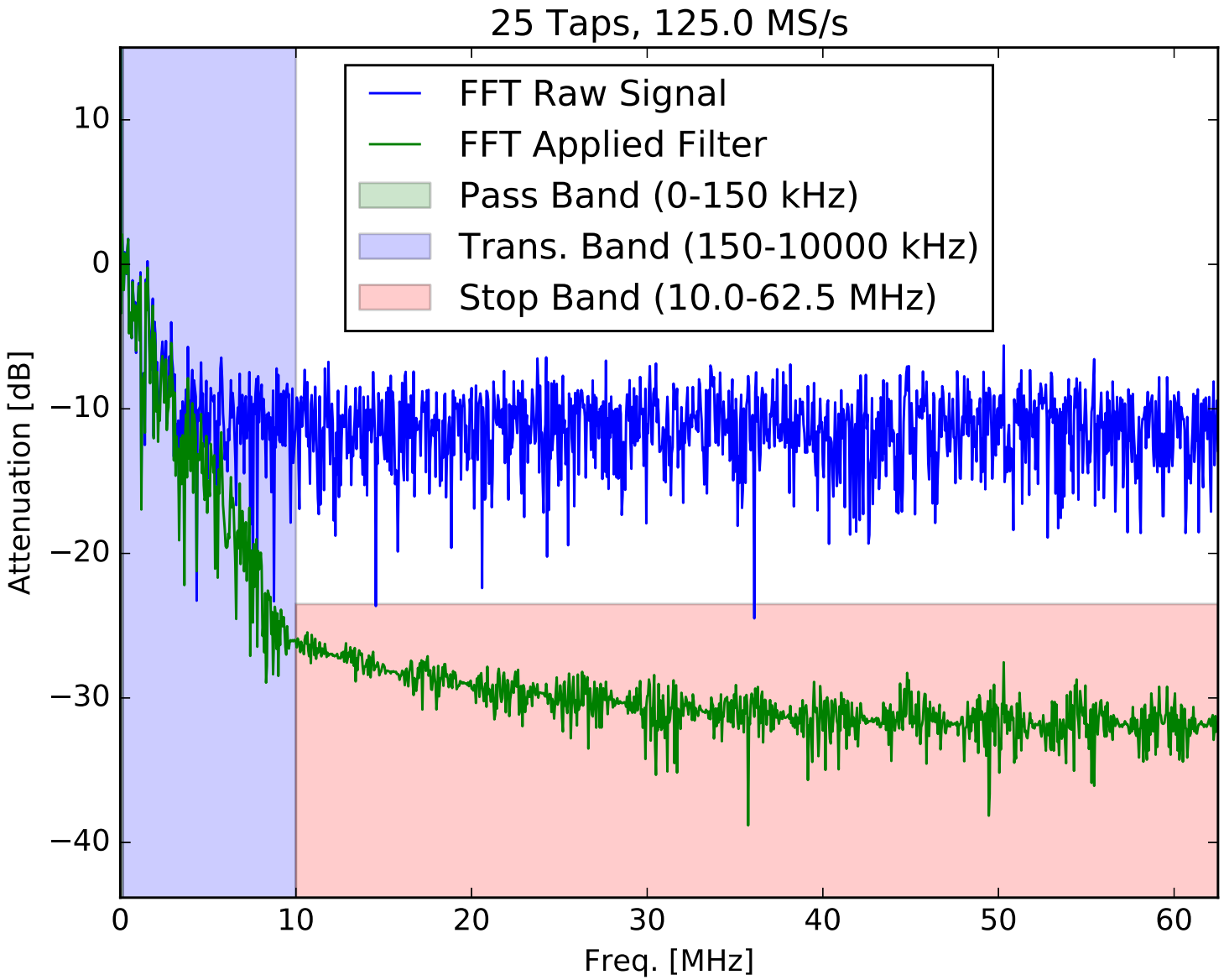

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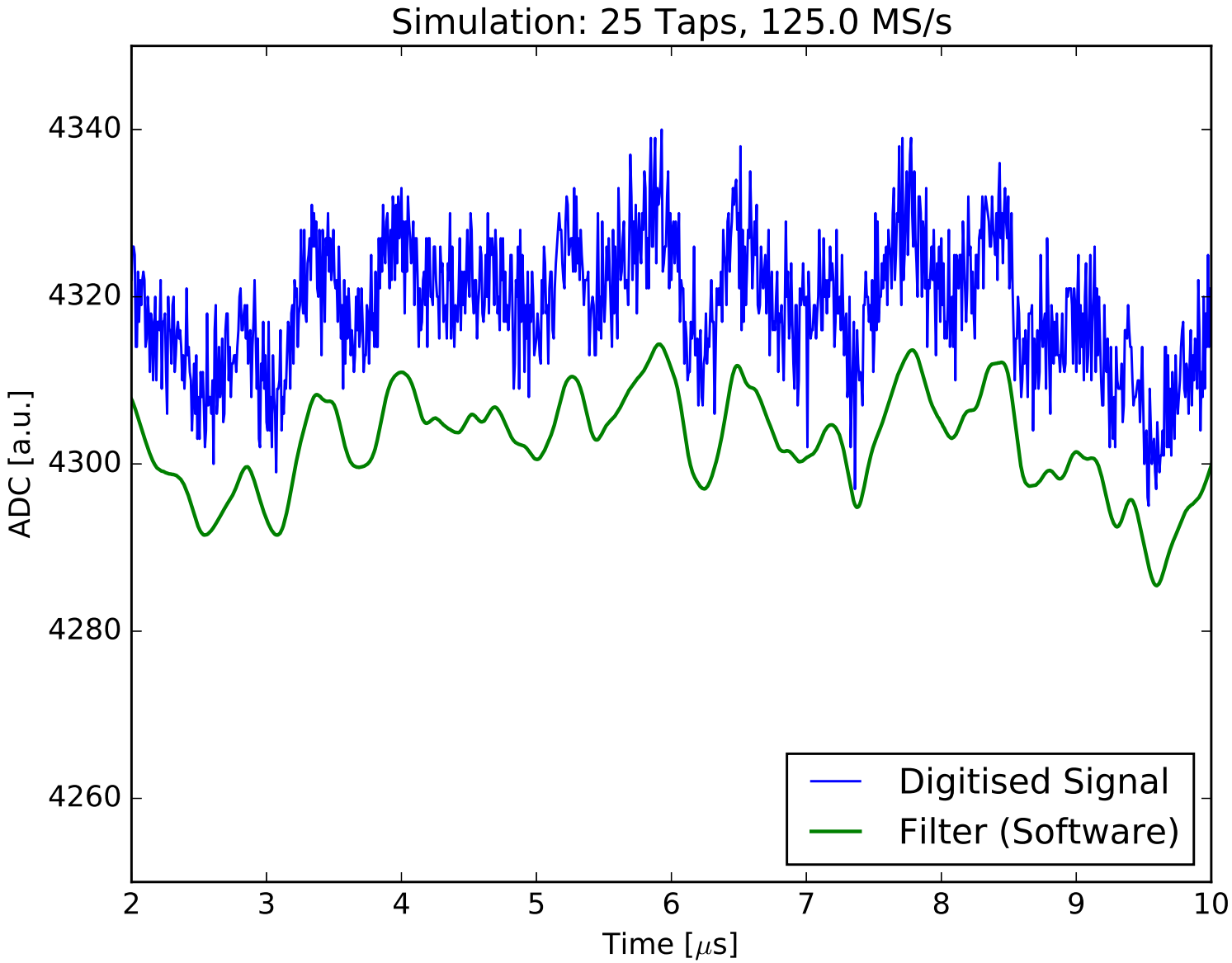
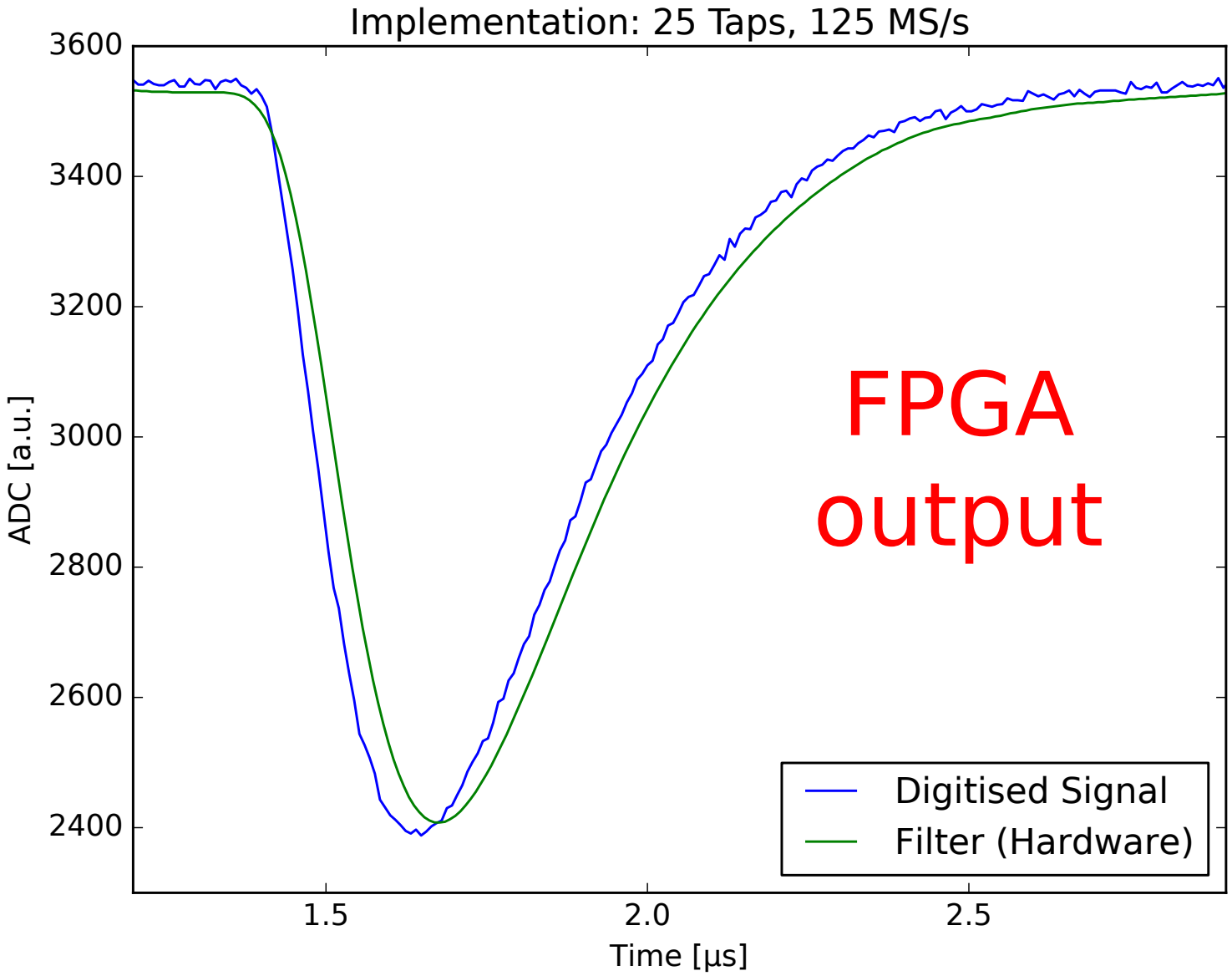


Signal from APFEL Preamplifier - Online Smoothing



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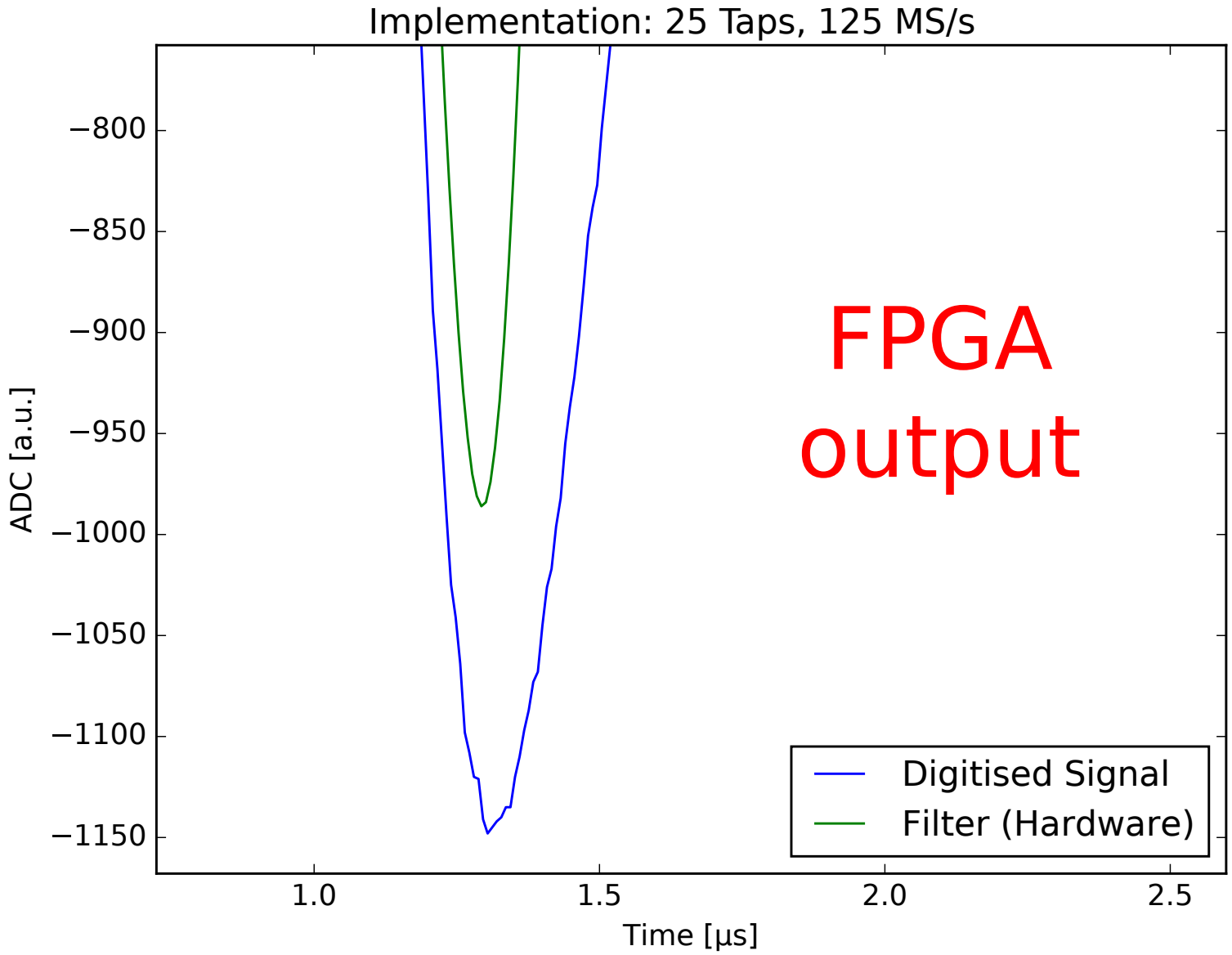
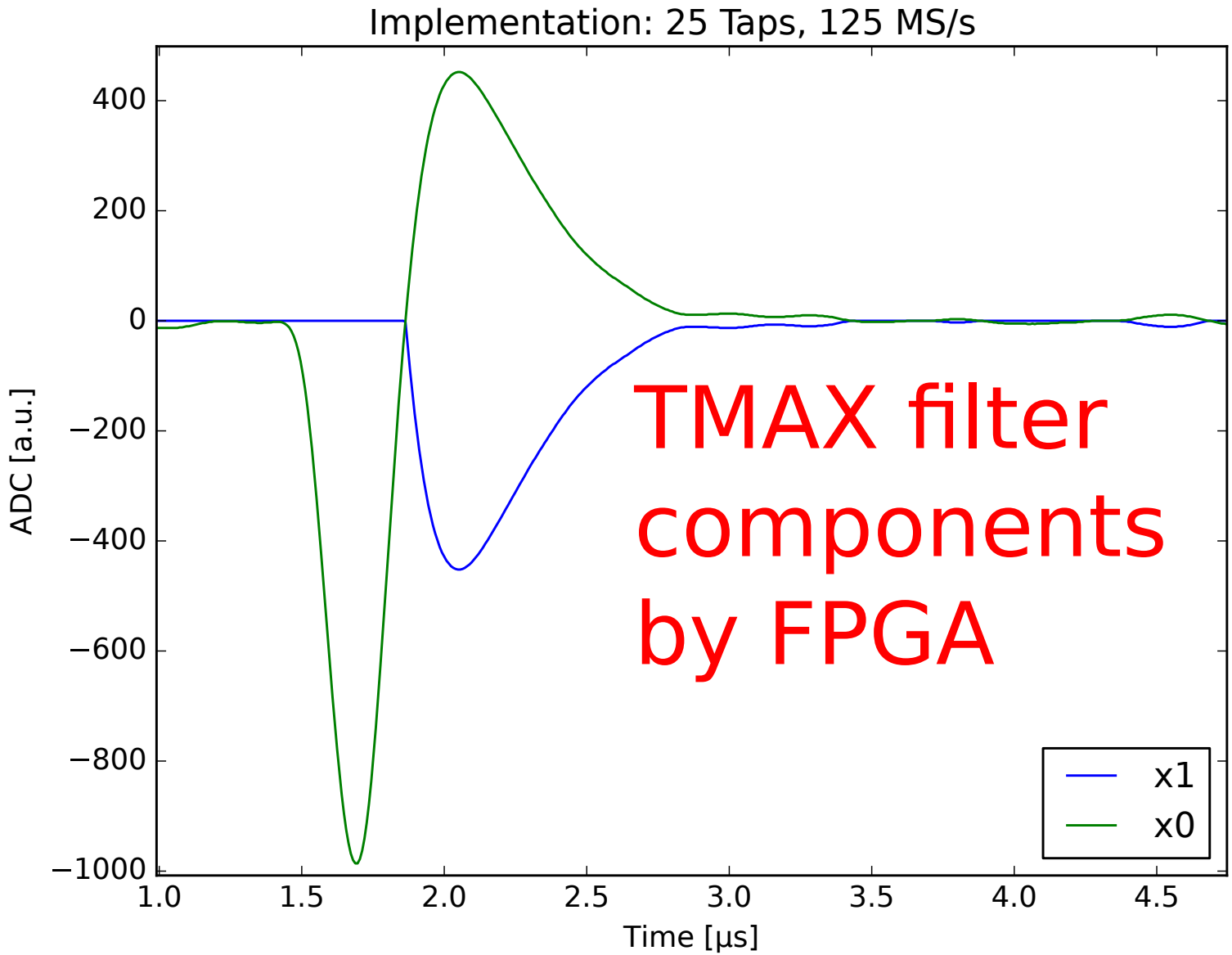


Time Measurement and Amplitude Extraction (TMAX)



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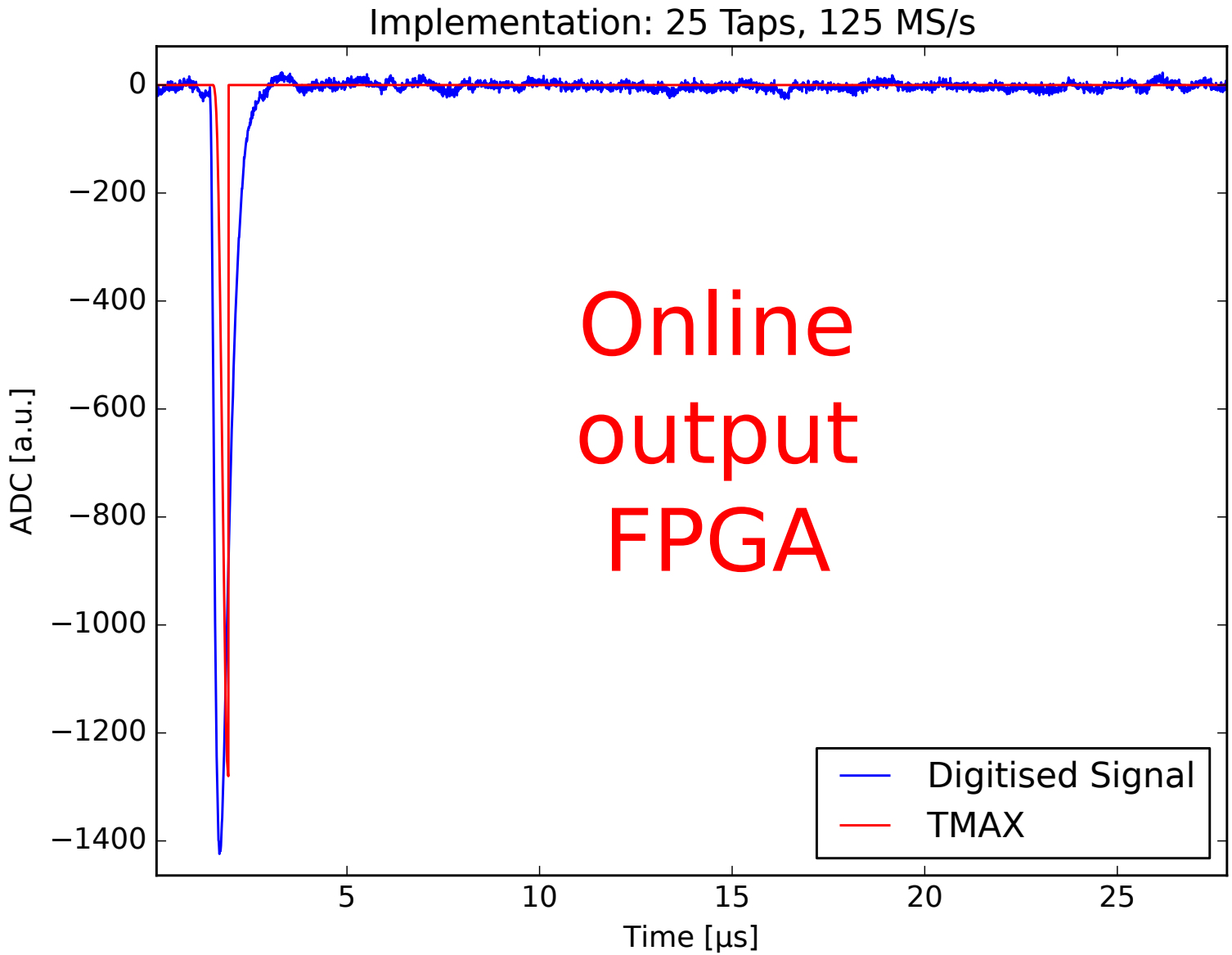

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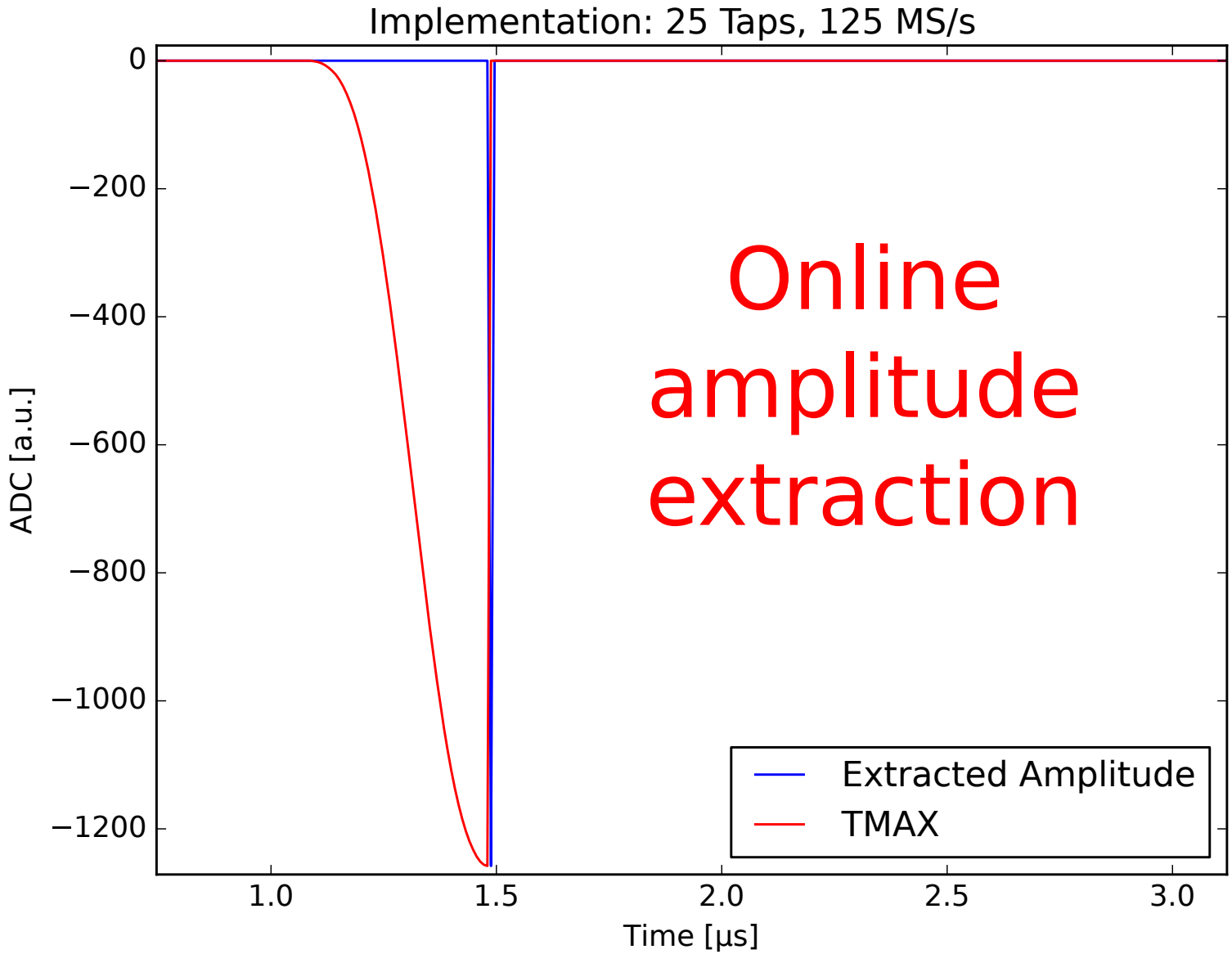

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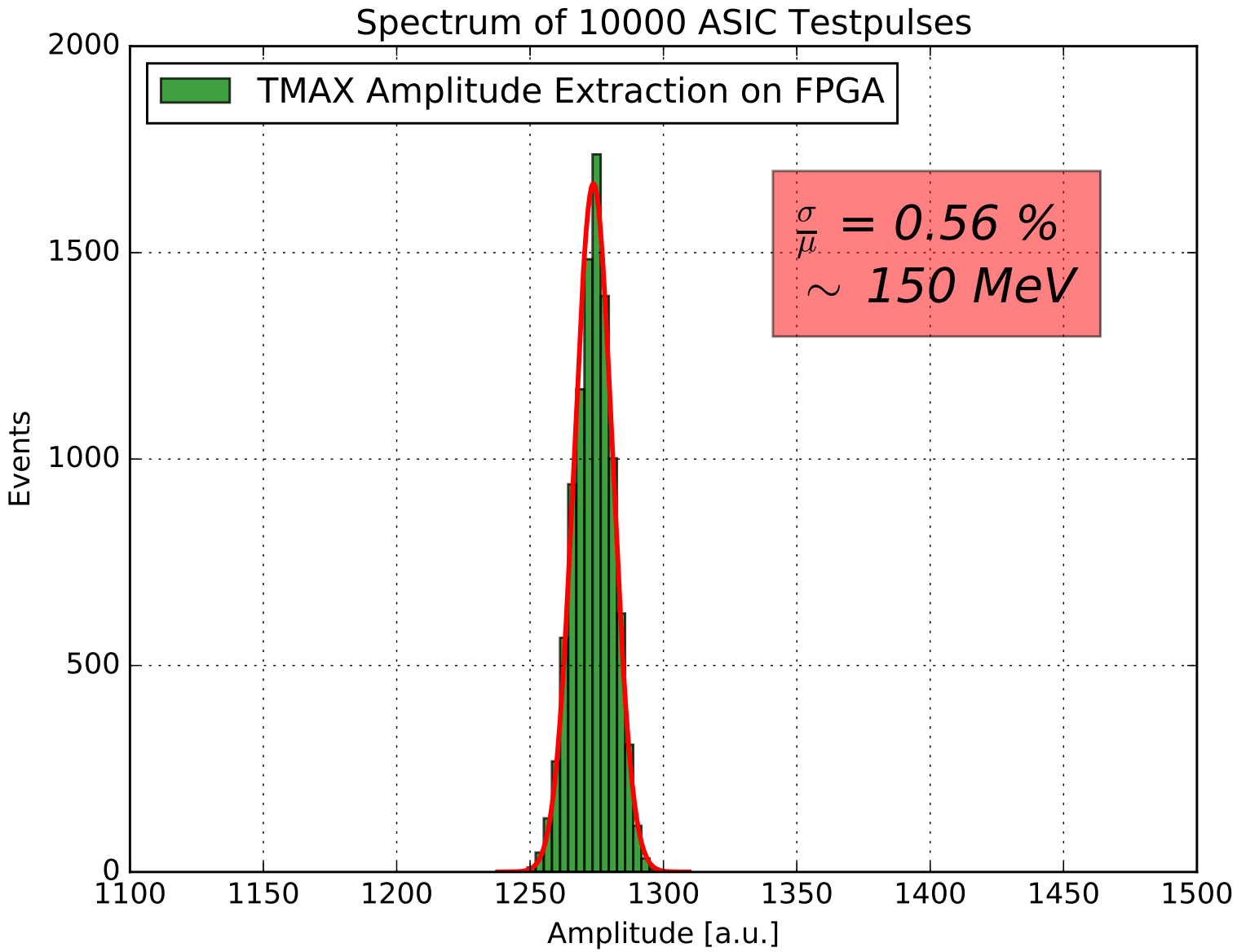
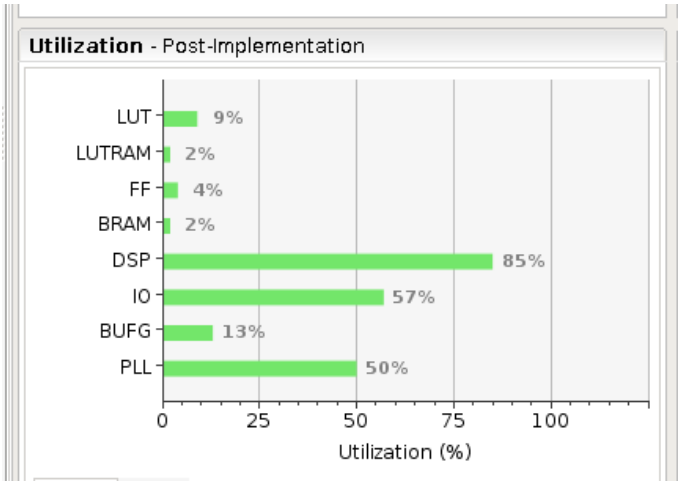


FPGA Utilisation for FIR+TMAX

Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
LUT	1518	17600	8.63
LUTRAM	108	6000	1.80
FF	1555	35200	4.42
BRAM	1	60	1.67
DSP	68	80	85.00
IO	57	100	57.00
BUFG	4	32	12.50
PLL	1	2	50.00



COMPARE	XC7K70T	XC7K160T	XC7K325T
Logic Cells	65,600	162,240	326,080
DSP Slices	240	600	840
Memory	4,860	11,700	16,020
GTX Transceivers	8	8	16
I/O Pins	300	400	500

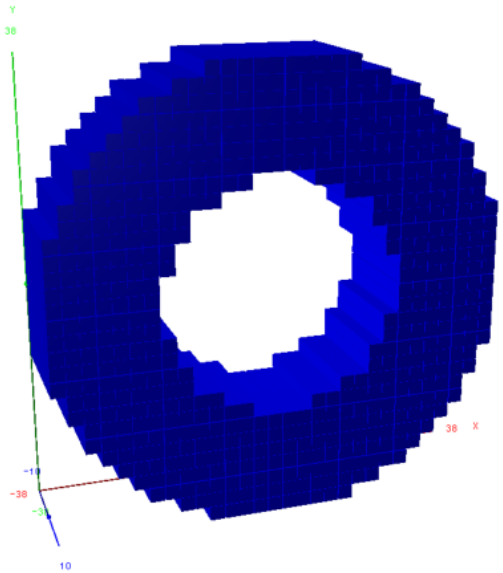
Update of BWEC Implementation in $\bar{\text{P}}$ANDA ROOT

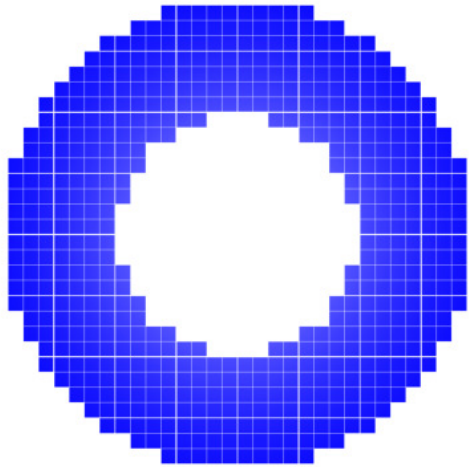
- See also computing session contribution by Luigi

$\bar{P}$ANDA ROOT Implementation

Past (2008)

- Many open questions:
  - Materials
  - Mechanical constraints
  - Number of crystals
- Only simple implementation of crystals $\rightarrow$ no dead material
- Since then, geometry has changed.

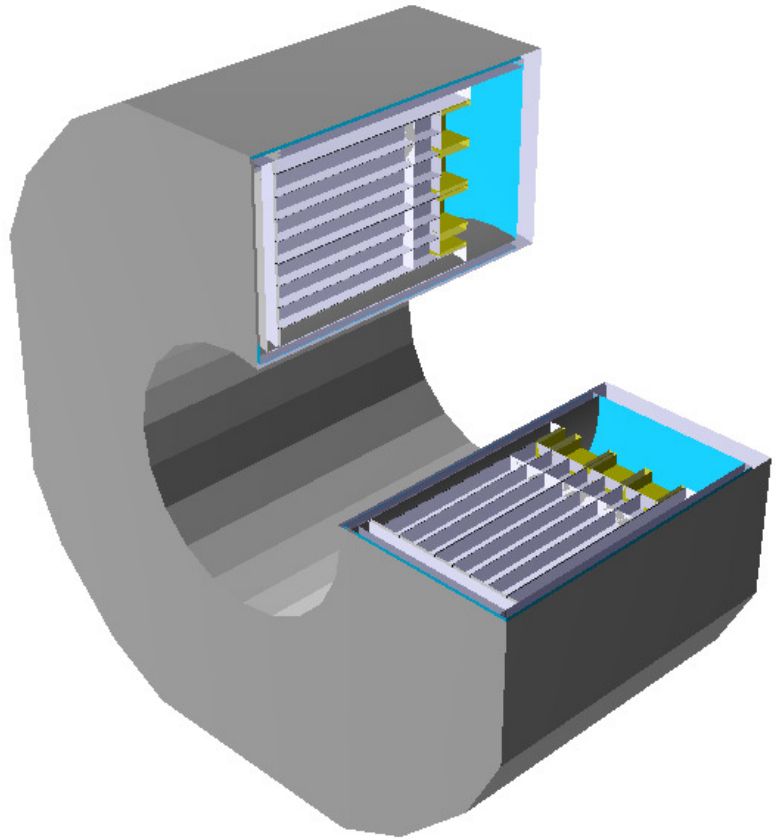




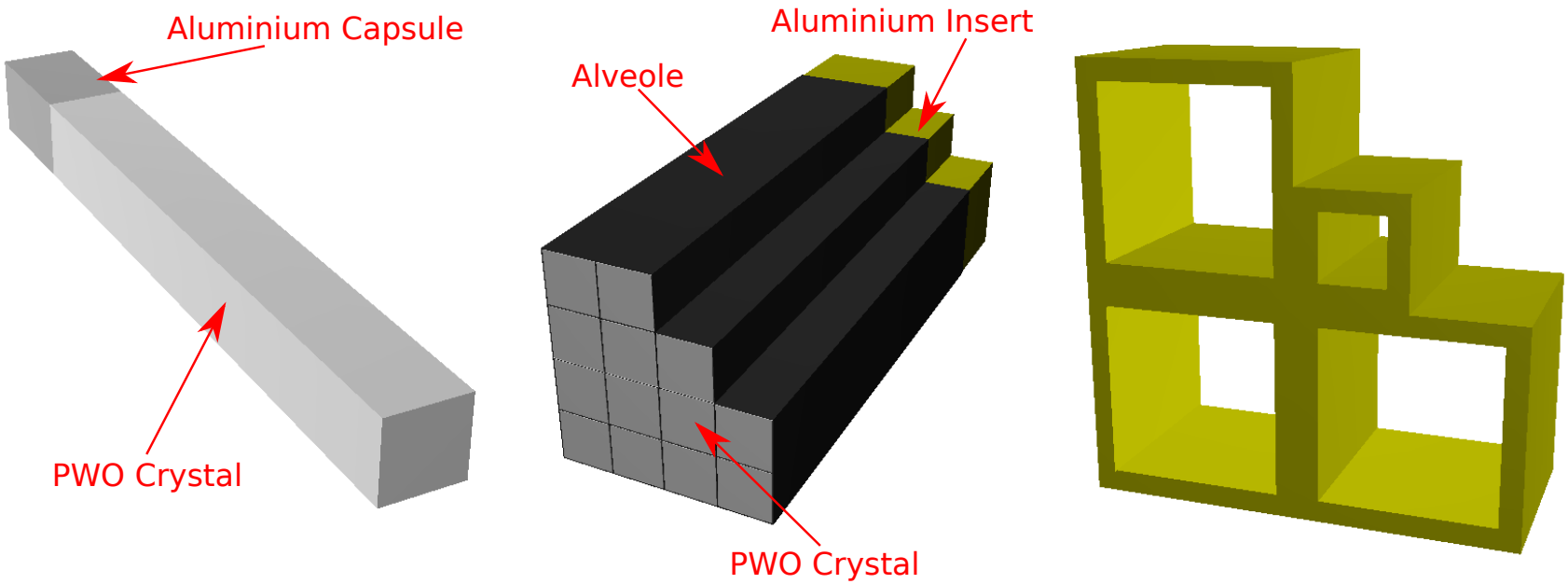
$\bar{P}$ANDA ROOT Implementation

Now

- Present geometry ✓
- More details:
  - Alveoles ✓
  - Inserts ✓
  - Aluminum capsules ✓
  - Radial cooling ✓
  - Front cooling ✓
  - Cooling fluid ✓
  - Insulation (VIP) ✓
  - Gaseous nitrogen ✓
- ROOT geometry ✓



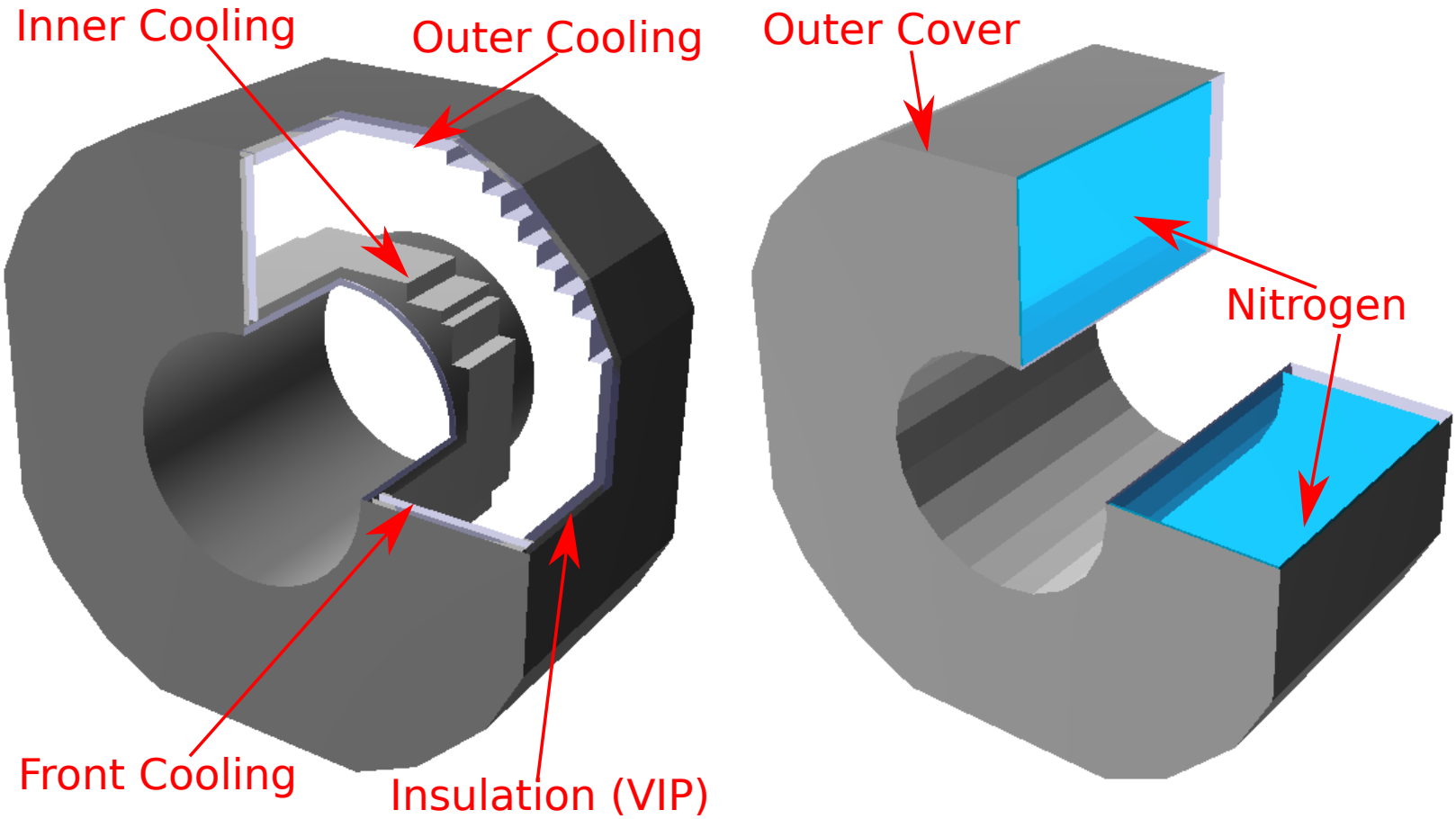
$\bar{P}$ANDA ROOT Implementation



Implementation of material behind crystals?

- Backscattering
- More detailed determination of radiation dose in the hall

$\bar{\text{P}}$ANDA ROOT Implementation



$\bar{P}$ANDA ROOT Implementation

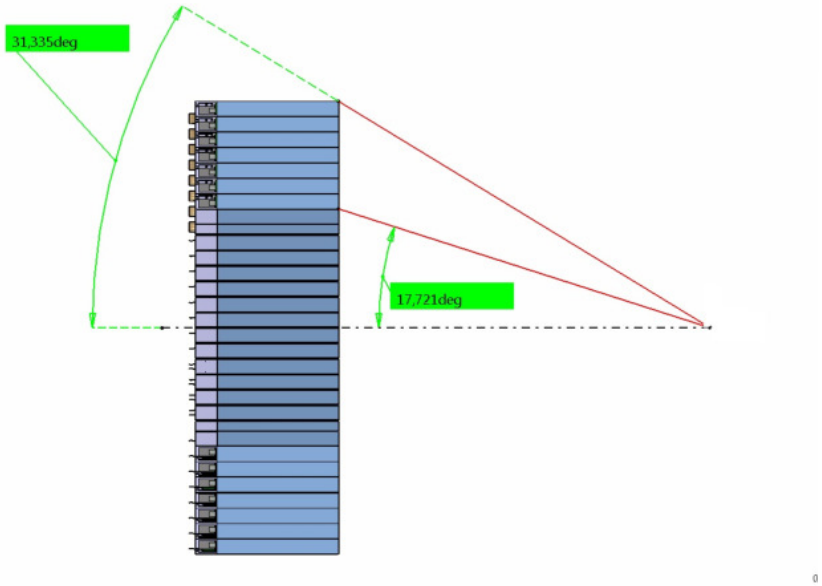
Materials available

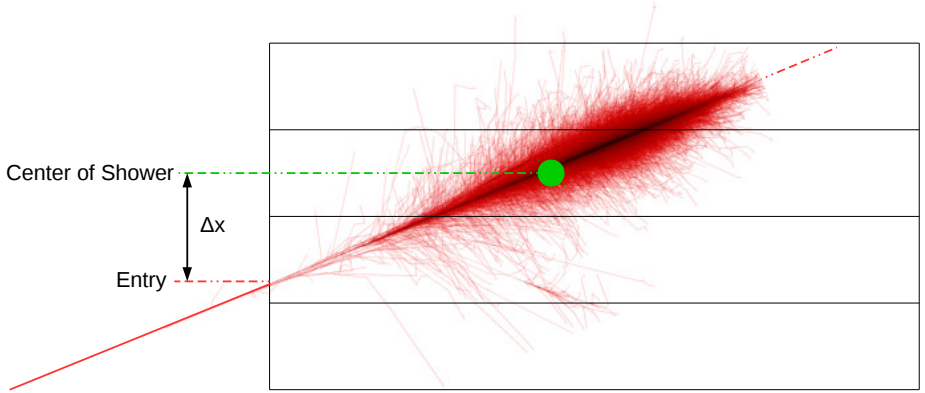
- Cooling fluid (water-methanol mixture)
- Prepreg (Carbon fiber reinforced polymer)
- Gaseous Nitrogen at 1013 hPa and -25°C

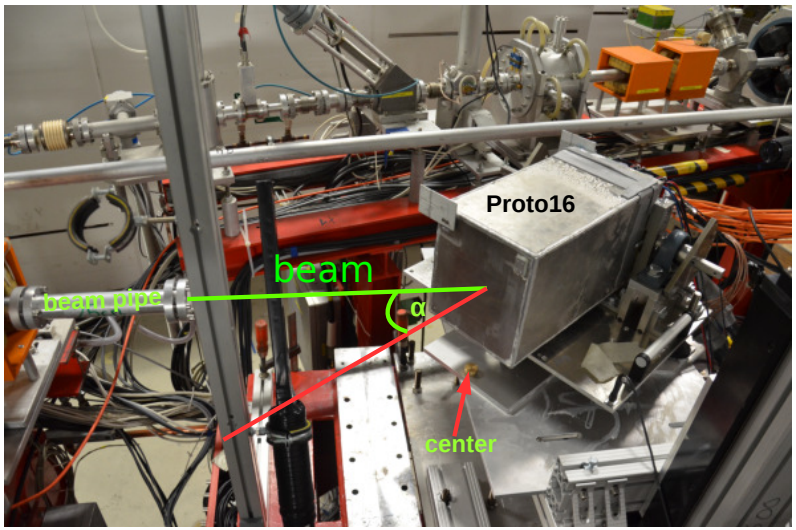
To do

- Event reconstruction
- Crystal mapping modification
- BWEC angle correction

$\bar{P}$ANDA ROOT Implementation

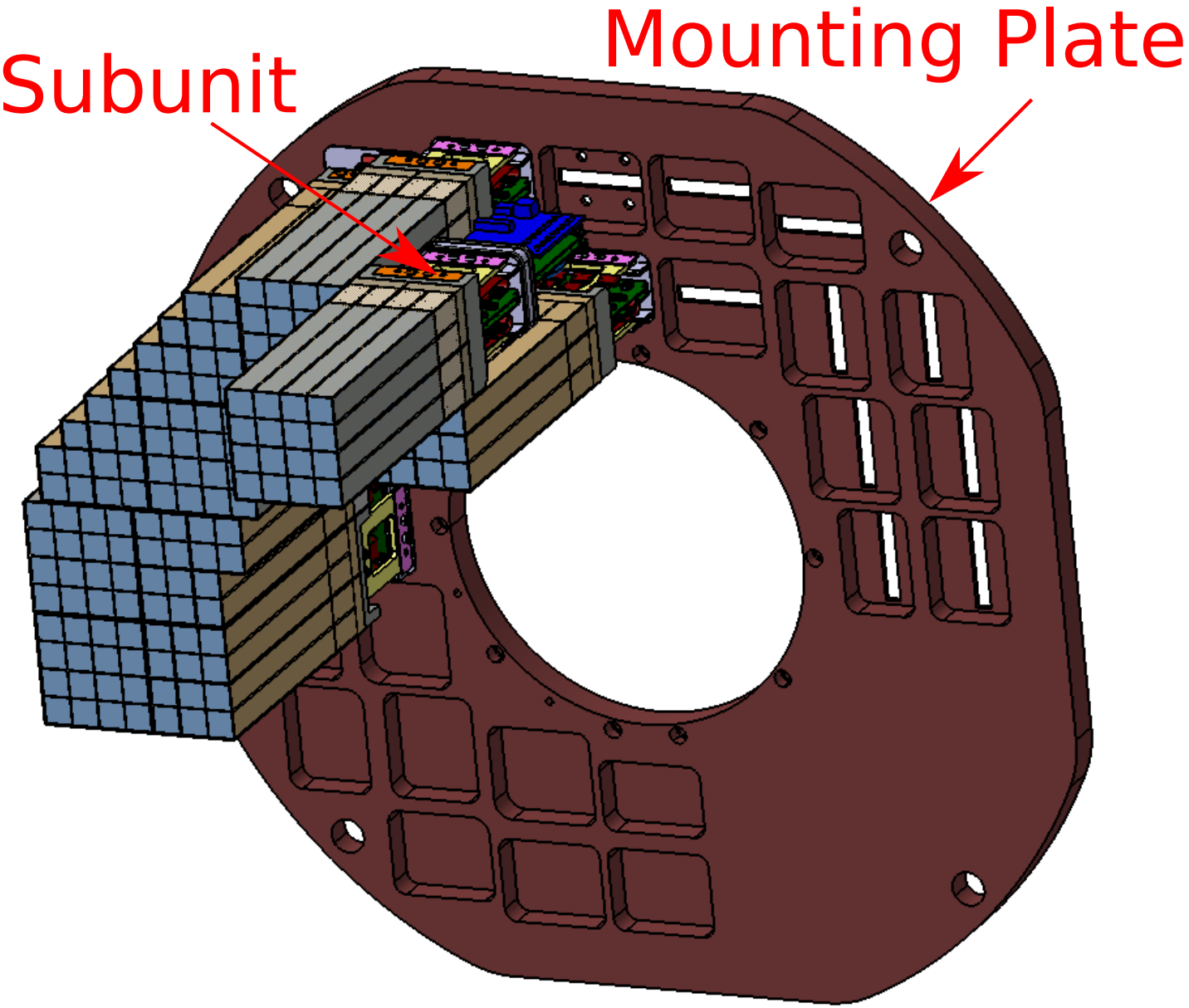






New Analog Line Driver and PROTO16-2

New Analog Line Driver



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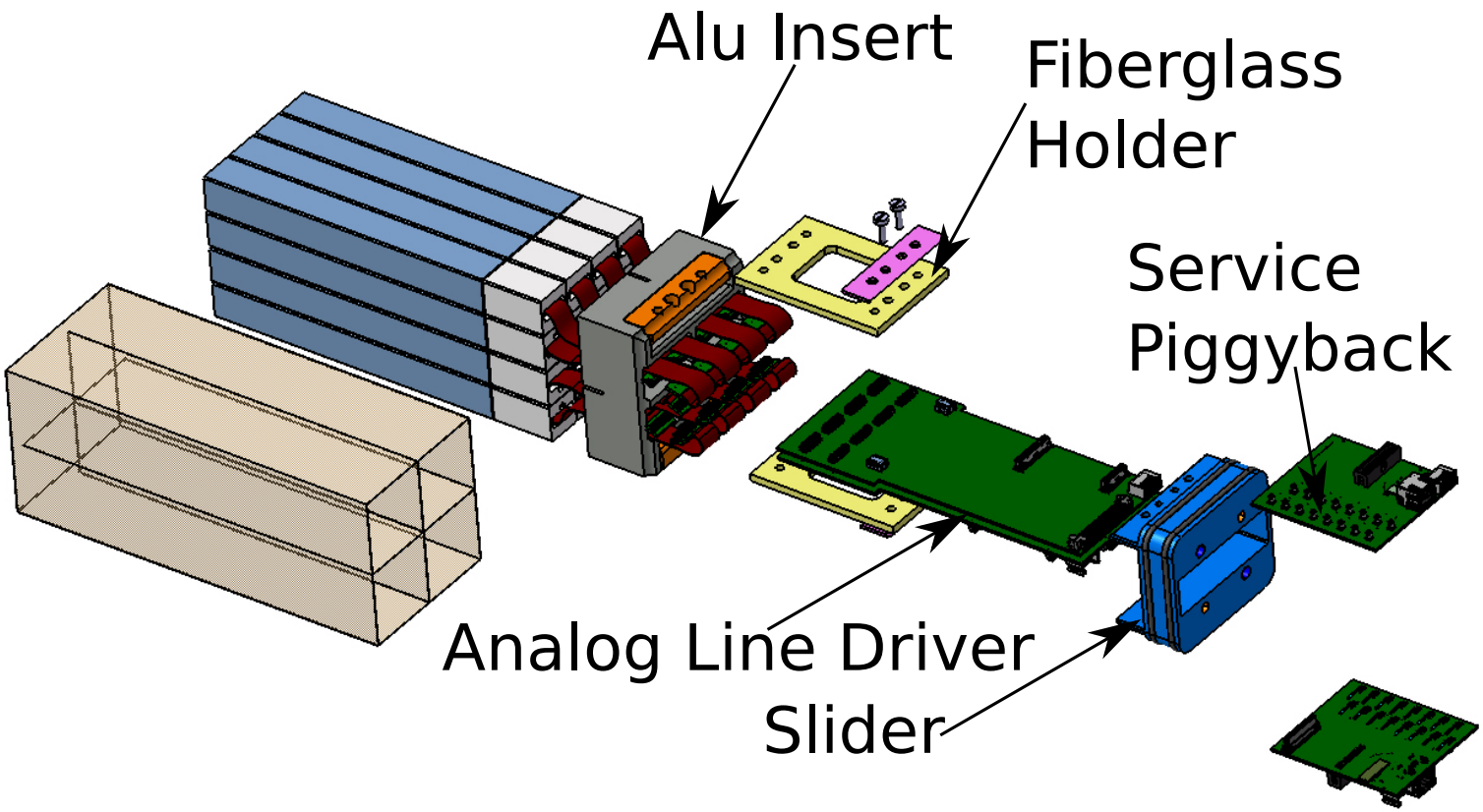

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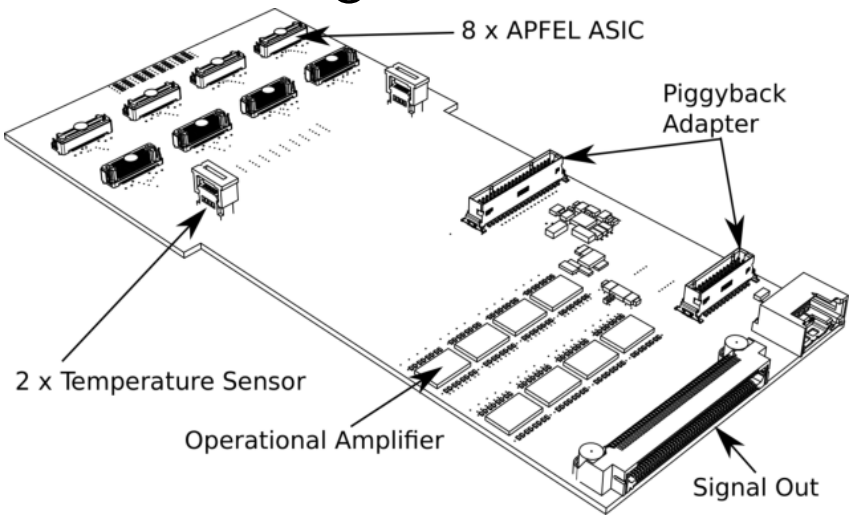
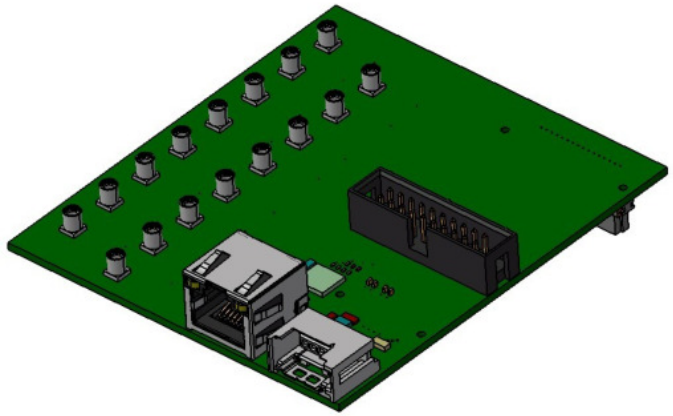
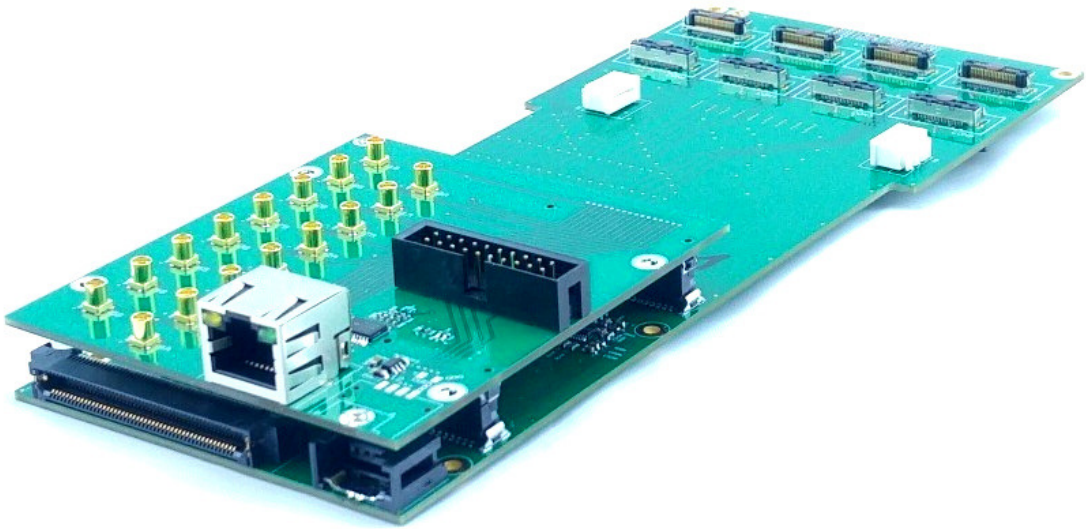


Service Piggyback



- HV input
- HV splitter/trimmer
- THMP connector
- ASIC control connector
- Line driver adapter

New Analog Line Driver



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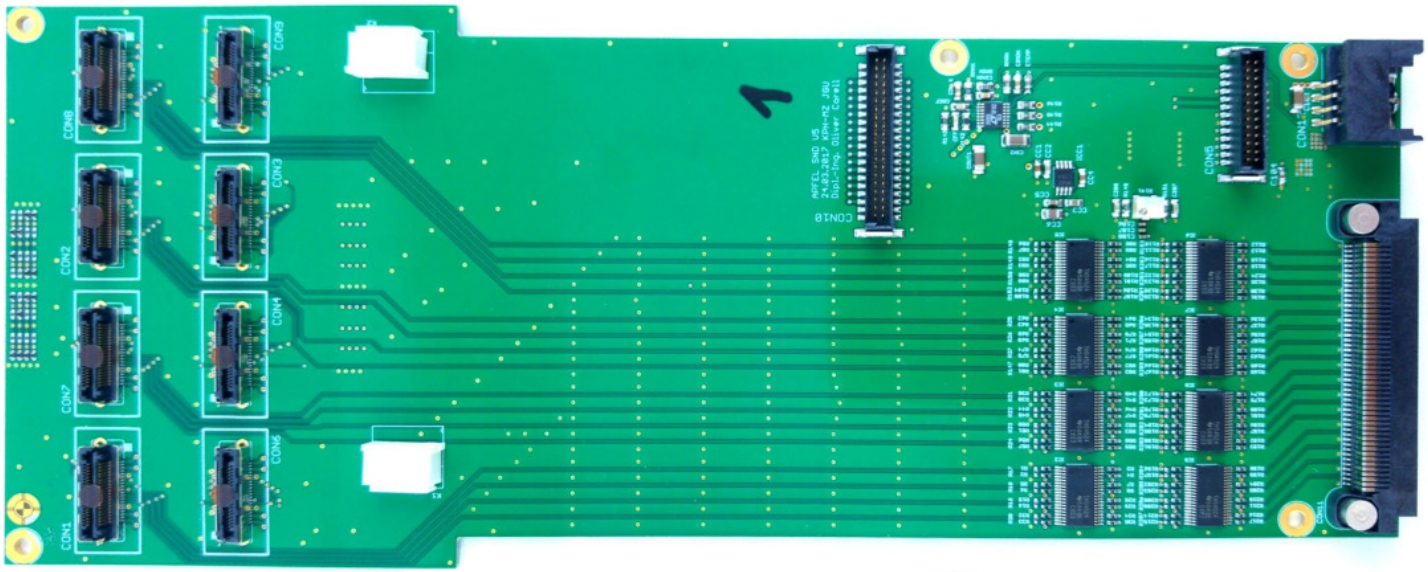
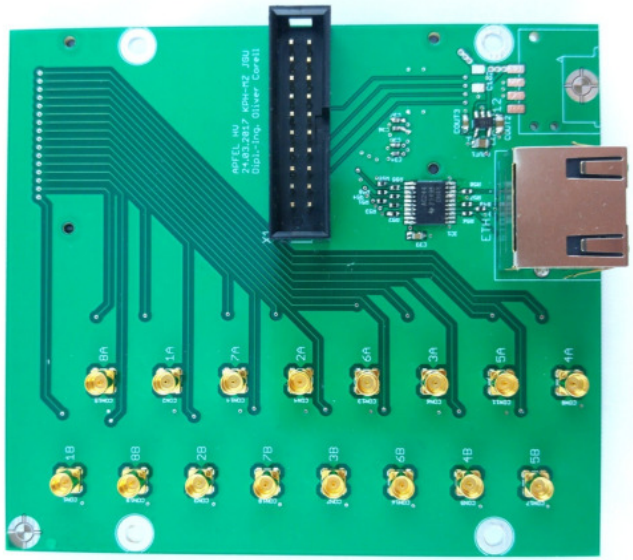
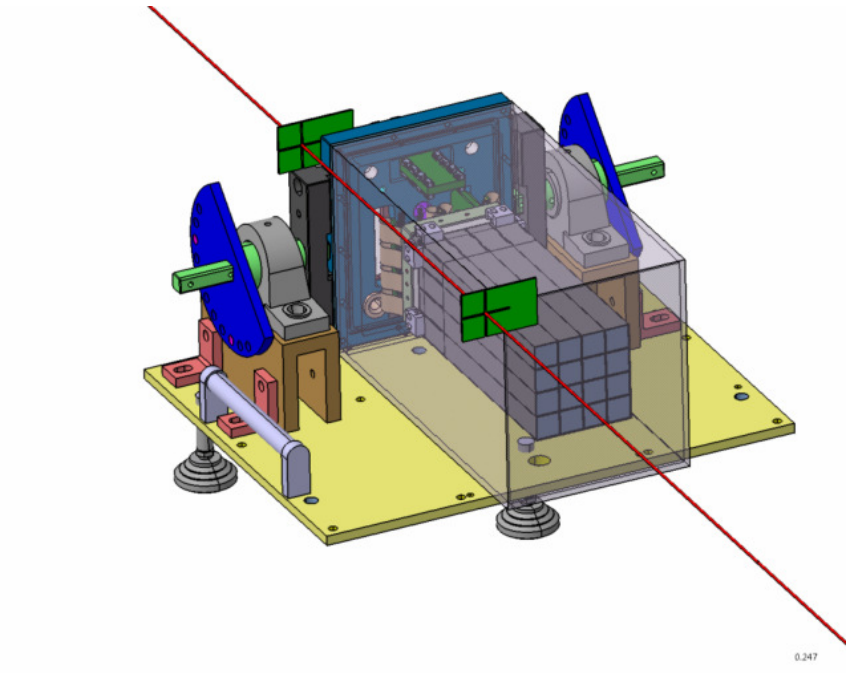




PROTO16-2



PROTO16-2

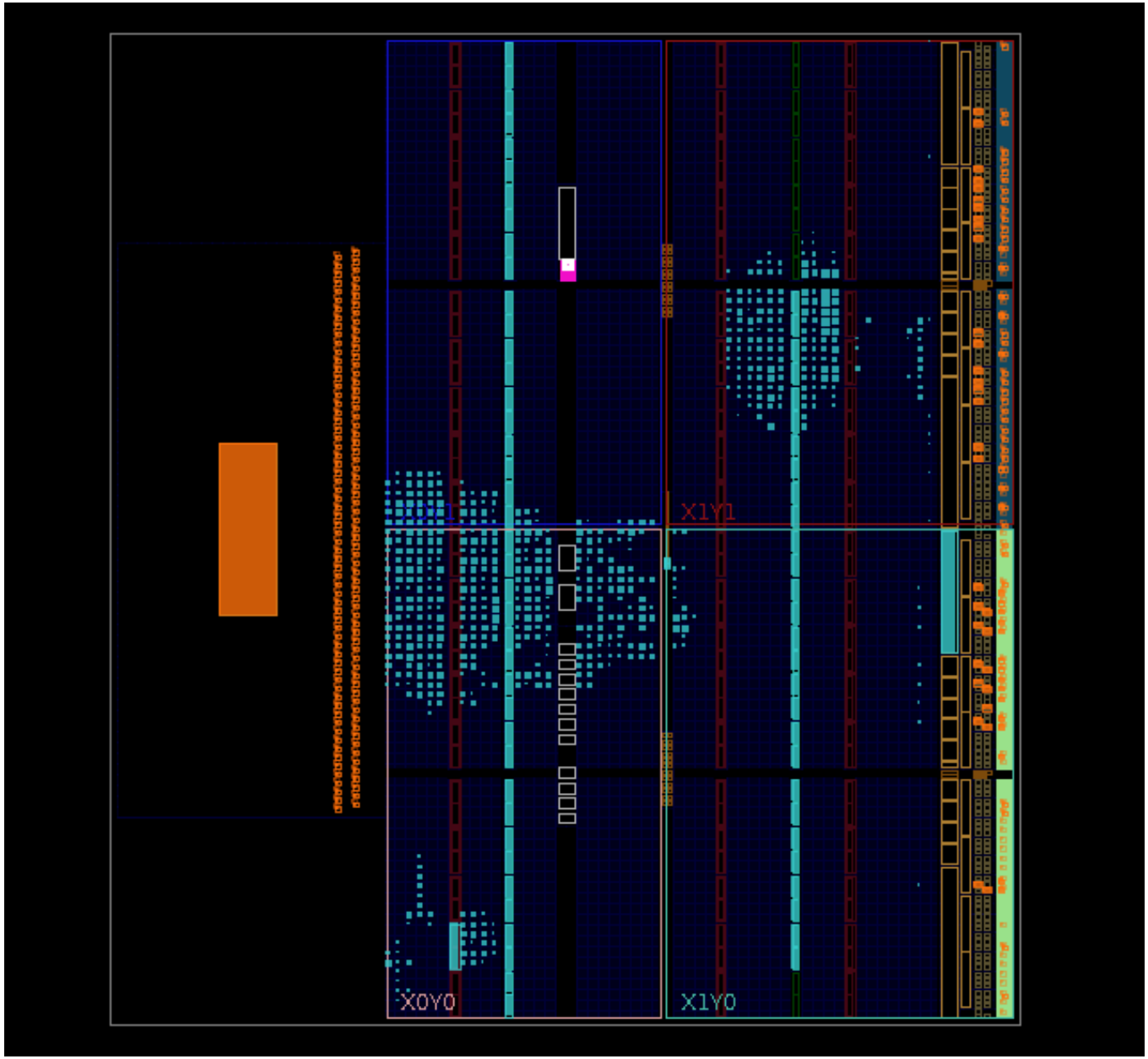
- New prototype
- Independent tests
- DAQ tests
- Phase-0 preparations

Summary

- First feature extraction implementation on FPGA
  - Smoothing optimisation (Parameter, DSP-Slice consumption...)
  - t_0 extraction
  - Transfer to Kintex/$\bar{\text{P}}$ANDA-ADC
- Update of BWEC geometry in $\bar{\text{P}}$ANDA-ROOT
  - Detailed implementation
  - New materials are available
  - Event reconstruction and crystal mapping needs to be modified
- New sender boards have been arrived
  - Tests
  - Building second PROTO16 with new design

Backup

FE - Smoothing via Finite Impulse Response (FIR) Filter



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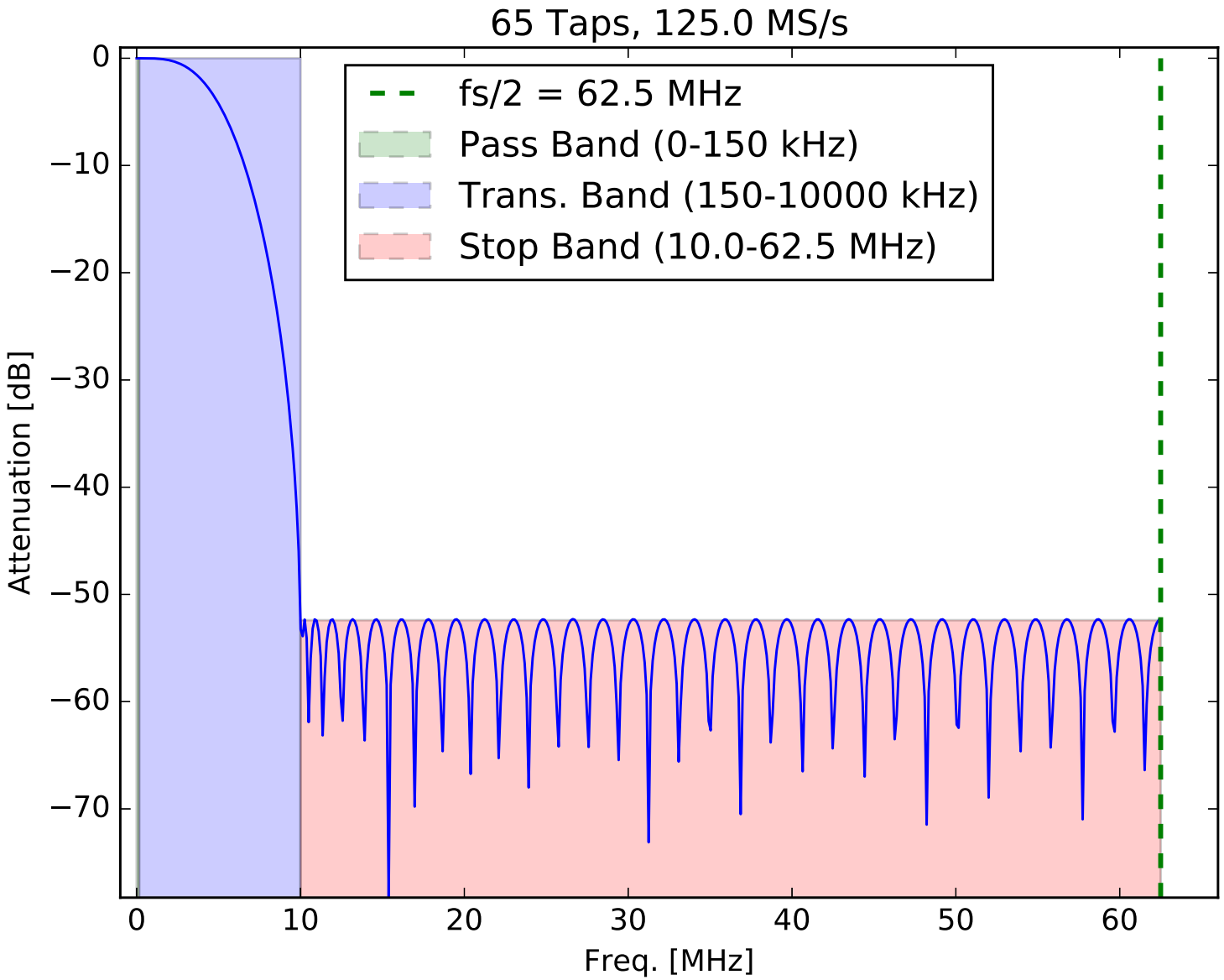

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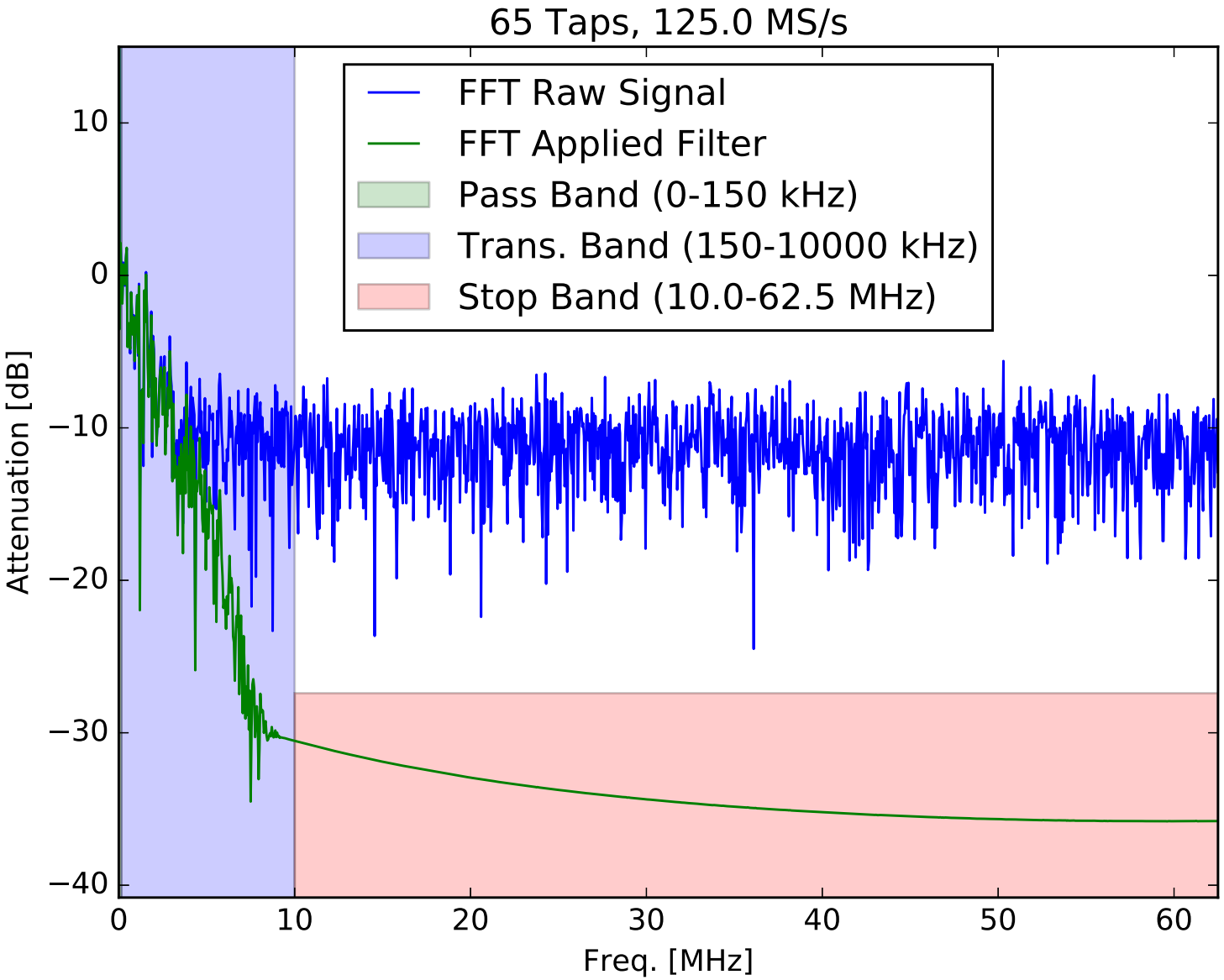

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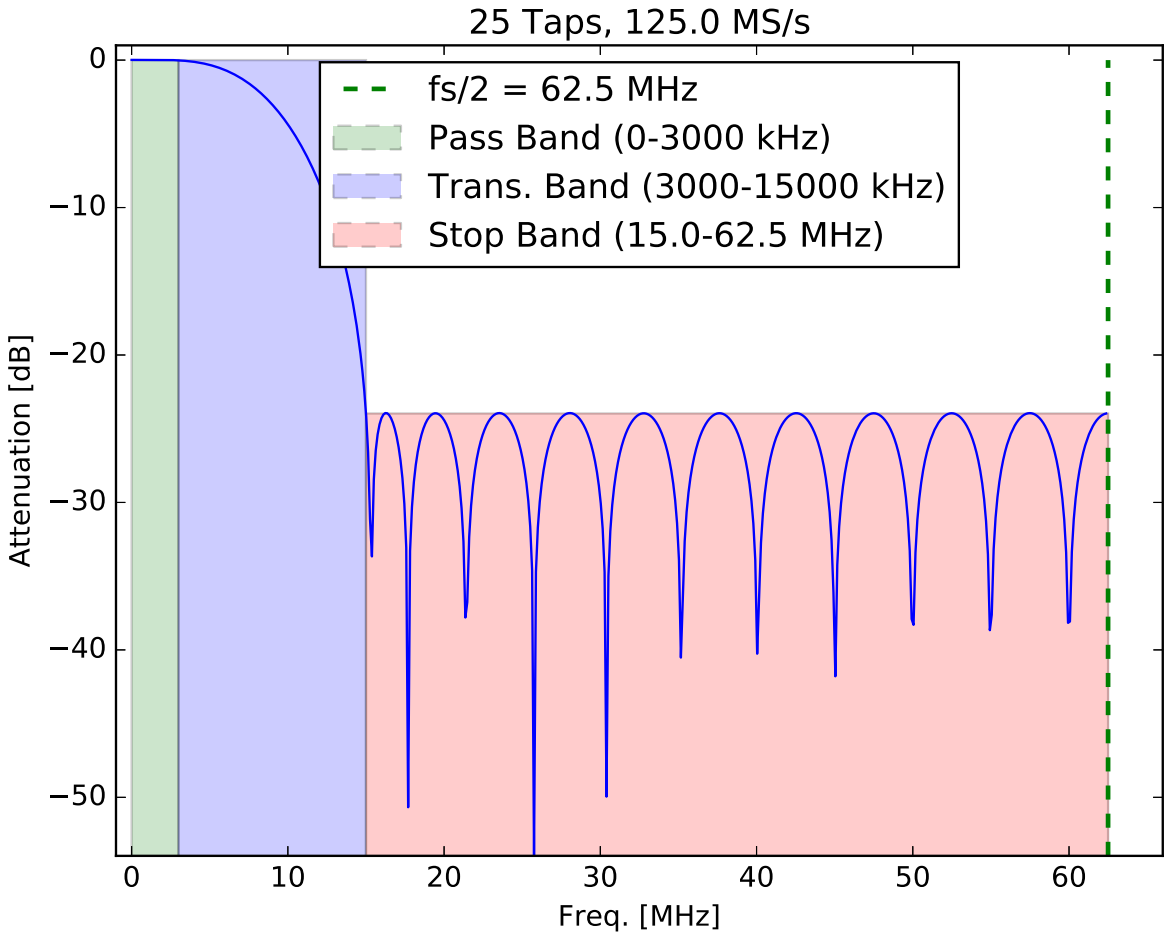

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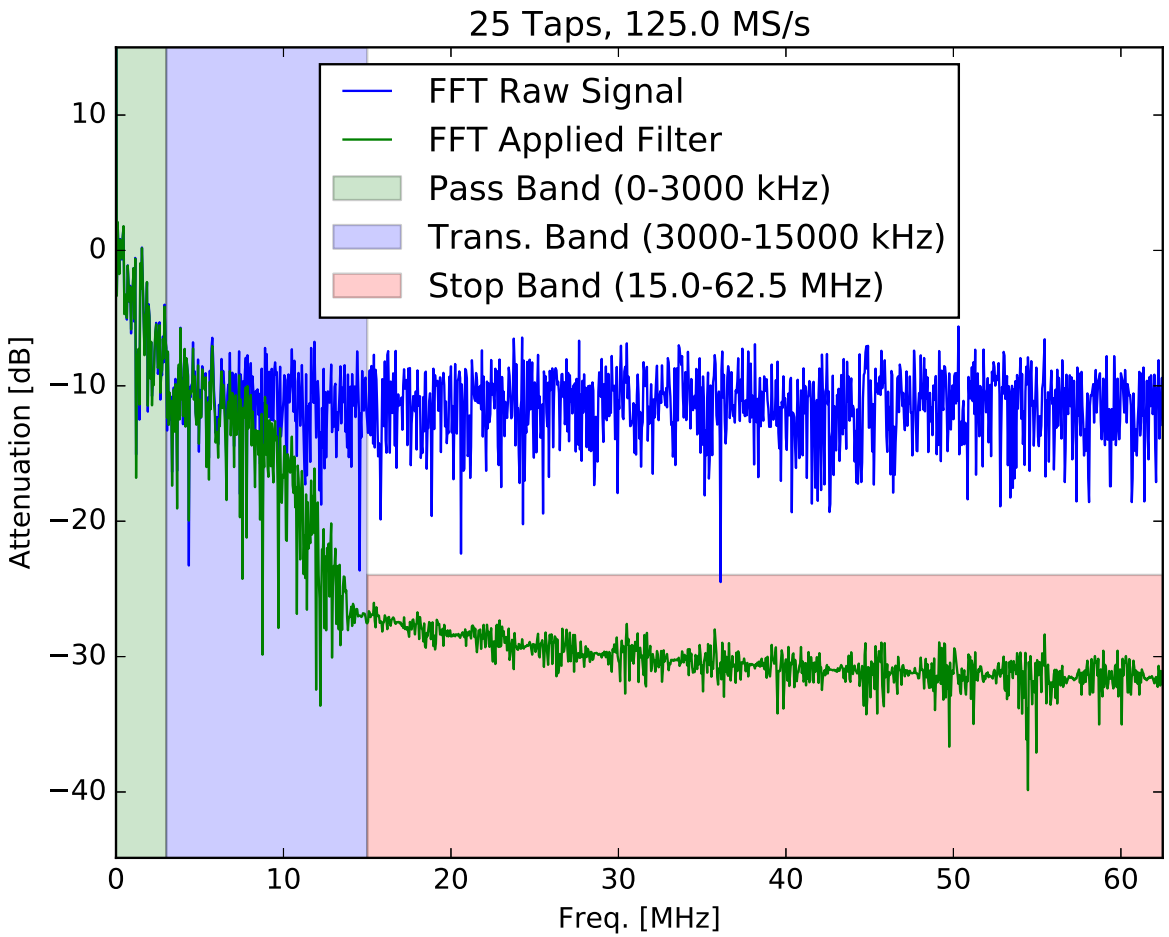

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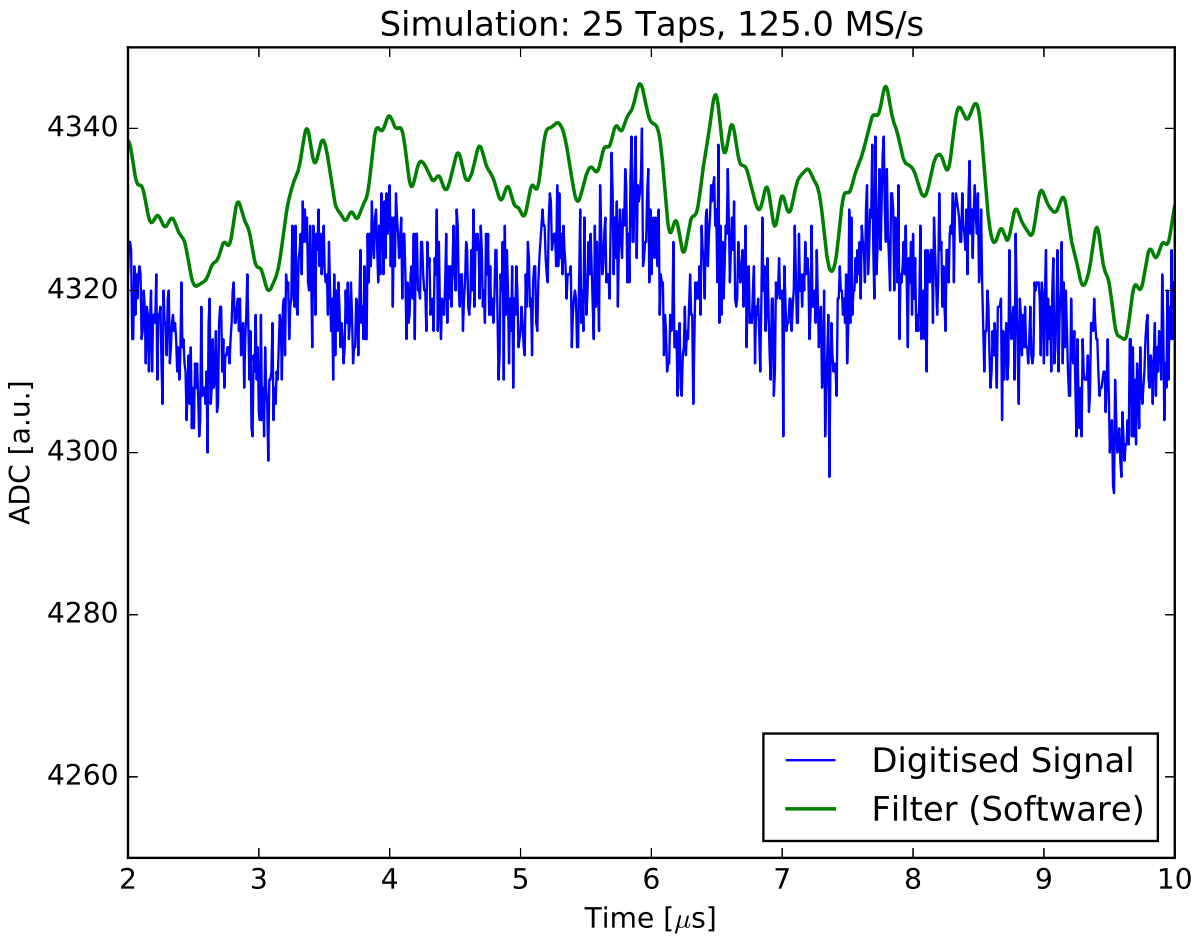

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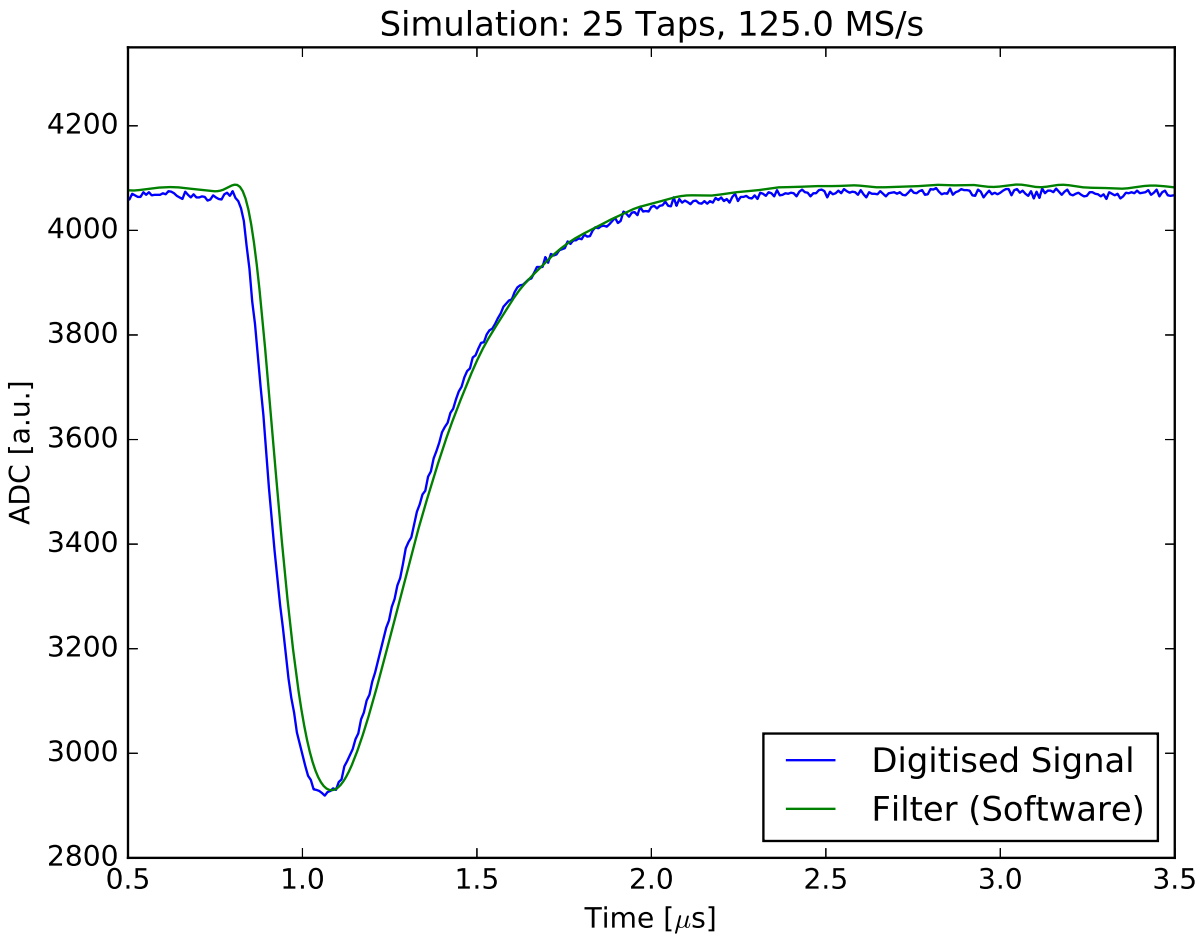
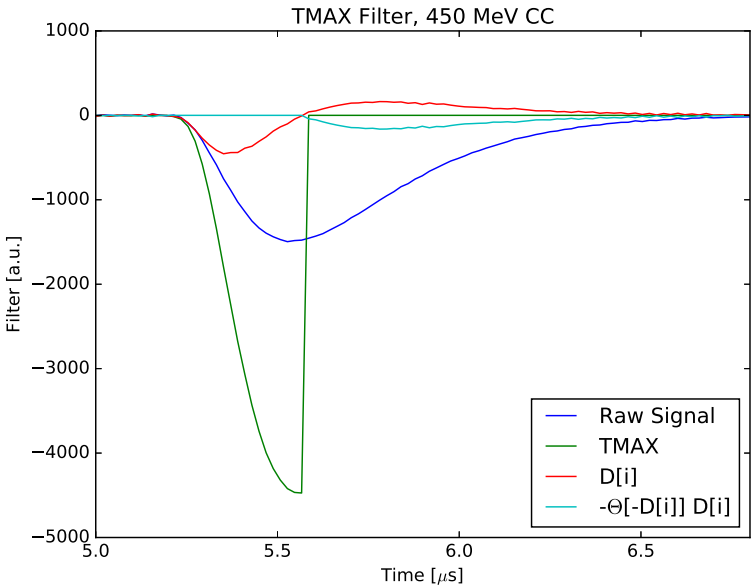
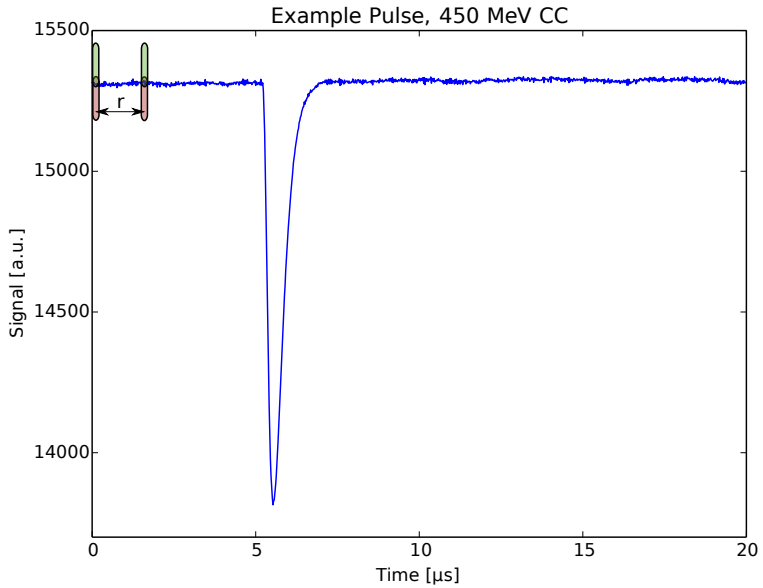


TMAX Filter





Derivative:

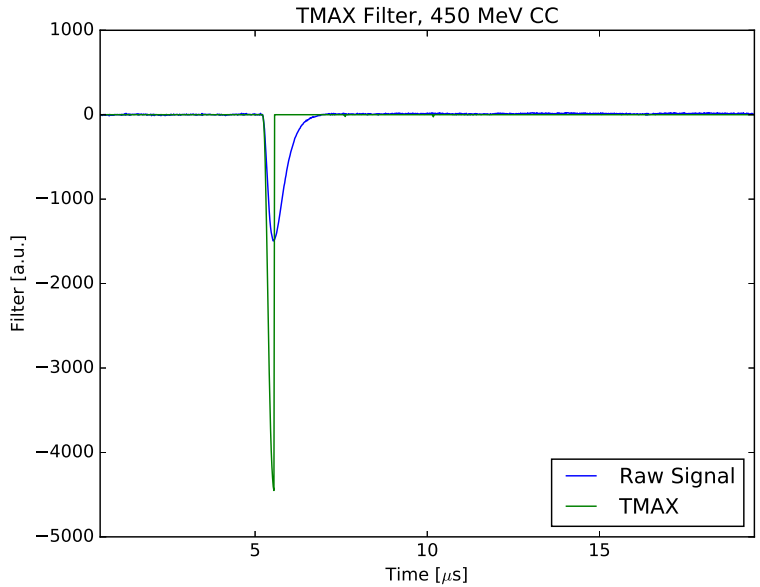
$$D[i] = T[i + r] - T[i]$$

Heaviside function Θ:

$$x \mapsto \begin{cases} 0: & x < 0 \\ 1: & x \geq 0 \end{cases}$$

TMAX:

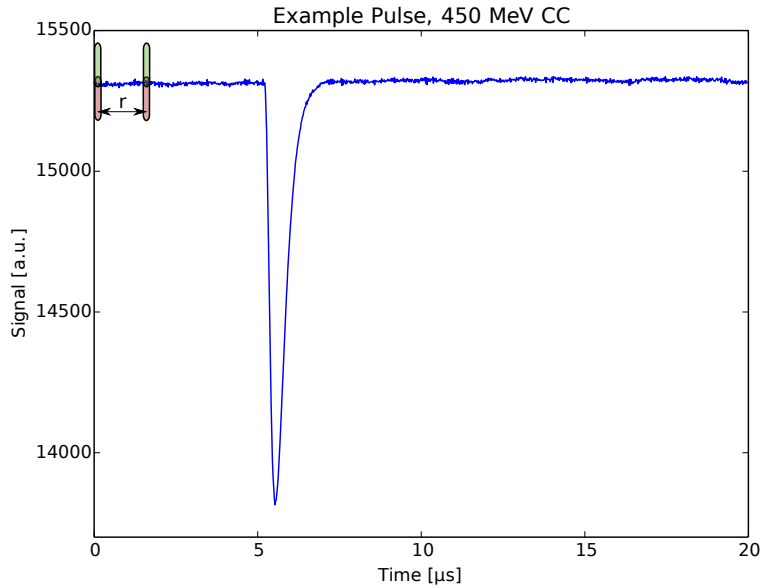
$$F_{TMAX} = \sum_{i=0}^{N} D[i] - \Theta[-D[i]] \cdot D[i]$$



TMAX Filter

TMAX Filter

- Sensitive on rising edge
- Cancels out falling edge
- No overshoot
- Short dead time



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