

# Current status of the strip development



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**JLU Giessen**



PANDA CM  
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# Activities

- First batch (barrel #3) of barrel strip sensors delivered by CiS and QA checked (2015/16)
- Situation of PASTA: First MPW prototype run still under evaluation, chip functional, list of modifications not closed yet
- Request: 1 FTE ASIC engineer for maintenance of PASTA revision 2 (→ Torino)
- Stalled funding situation: Most likely resumed funding from German ministry in 2018 for MVD
- Design of larger flex hybrid prototypes ready, waiting for a “go“
- Cooling concept shown to work (Thesis T. Quagli)

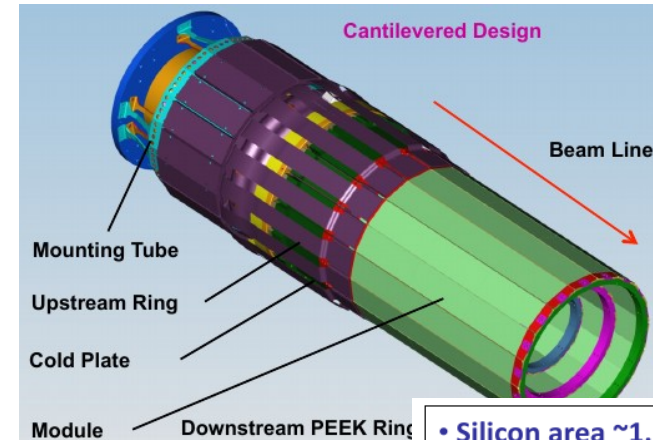
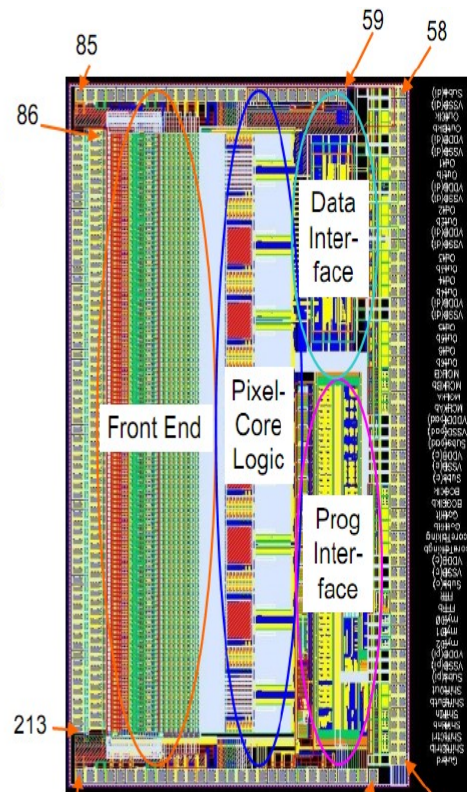
# Backup Strategy

## CLAS12 upgrade at JLAB:

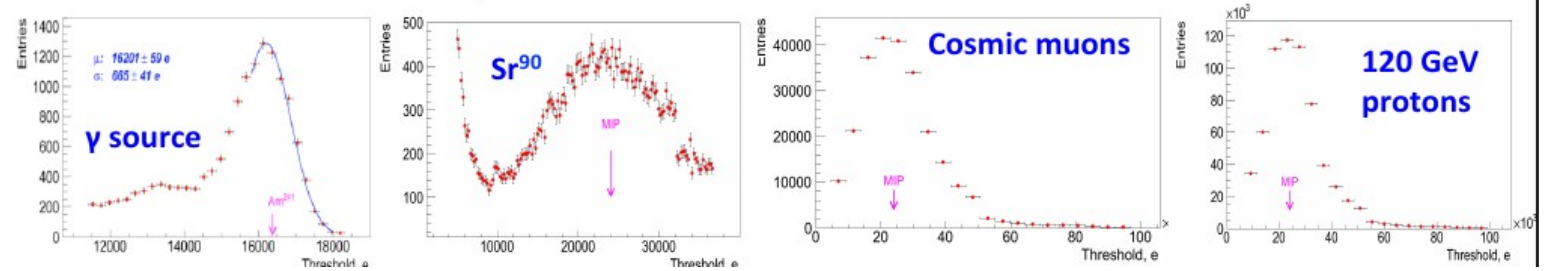
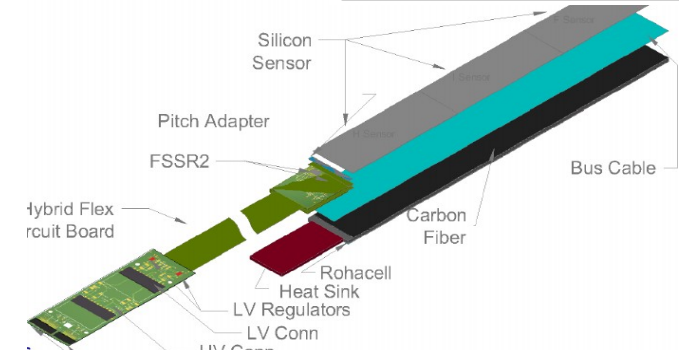
- SVT silicon tracker: single sided strip sensors read out with FSSR2 chip (Fermilab, BTEV)

### Fermilab Silicon Strip Readout Chip

- 128 channels / chip, 50  $\mu\text{m}$  input pitch
- Data-driven architecture - self-triggered
- 1 MHz input rate with < 2% missed
- Beam Cross Over (BCO) clock: from 128 ns
- DAQ synchronized with timestamp clock
- Zero-suppressed data readout
- 1-6 programmable serial outputs
- Double Data Rate (DDR) output
- Maximal data output rate 840 Mbits/s
- Anticipated data rate ~ 200 Mbits/s
- Data readout clock: use 70 MHz
- 24 bit data format for 'hit' channel
  - 12 bit Address
  - 8 bit BCO clock counter
  - 3 bit ADC
  - 1 Sync
- Power consumption < 4 mW / channel
- 2.5 V supply separated on chip
- Radiation hardness 5 Mrad



- Silicon area ~1.5 m<sup>2</sup>
- Channels: ~34,000
- Bonds: ~200,000



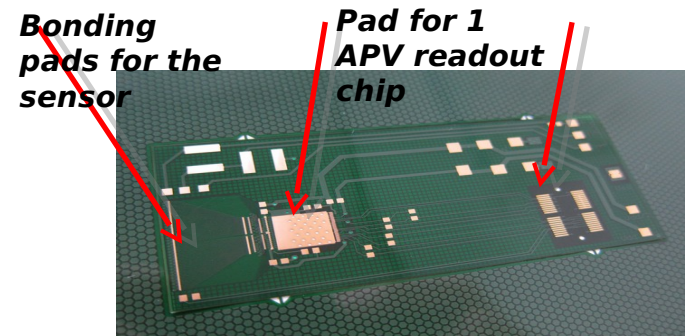
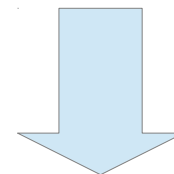
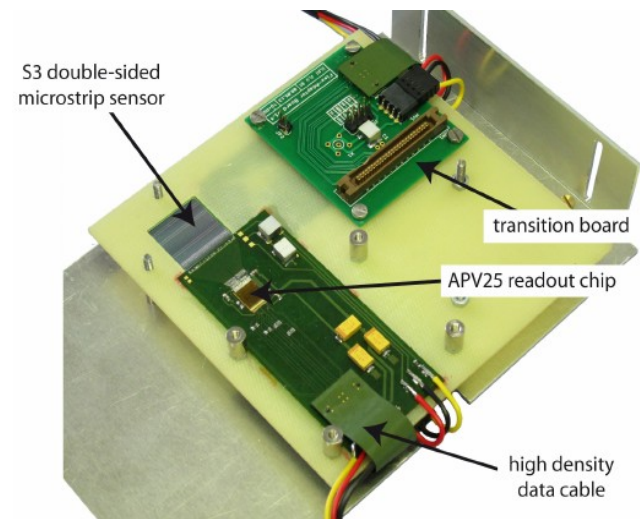
# Readout Hybrids

- Concept of integrated Flex PCB w. pitch adaptor
- Prototype for one APV25 produced and tested ok
- Design for multi FE flex ready since 2016, production on hold due to funding situation

**Applied for funding once more for next year**

Next step (3 parallel branches)

- Production of single FE flex for PASTA
- Production of multi FE flex for APV25
- Production of single FE flex for FSSR2





# Beam Telescope



## **StripTracking Station:**

- sensors 50 $\mu$ m pitch 2x2cm<sup>2</sup> and S1,S2 PANDA sensors+ APV25 for tracking in up to 4 planes
- up to 2 DUT boxes for varying assemblies, e.g. prototype sensor modules
- characterisation of DUT in beam + tracking for spatial resolution studies

## Module Controller for Strip Detector - report as of May 2017:

- manpower : H. Sohlbach app. 5 h per week until end of 2017 plus support from Giessen Group
- final goal: VHDL-based FPGA-design ready to be transferred into an digital ASIC
- status:
  - interface for Pasta [1]: design, implementation and functional simulation completed
  - data buffering and Pasta-style frame handling: design and implementation completed
  - triple-redundancy: design completed, implementation 50%, functional simulation t.b.d.
  - slow-control: in design, implementation 50%
  - e-link-ports: t. b. d.
  - mapping, clustering, hitfinding: in design, implementation 30%
  - testbench for full mdc design and input data of 11 pasta-chips completed

[1] A. Goerres, Pasta-Digital Interface, private comm. (2013)