STT Readout Status

Peter Wintz (FZ Jülich) for the STT group

61. PANDA CM, June-7th, 2017

Outline STT Readout Status

- Readout Overview
- ASIC/TRB System
- ADC-based System
- Summary

STT Readout Overview

- STT with drift time and charge readout for PID by dE/dx

- Two readout concepts for charge information
  - pulse width by time-over-threshold:
    - PASTTREC-ASIC with LE/TE-discriminator on front-end board, LVDS output
    - TRB readout system, ASIC control by central FPGA
  - pulse area by waveform sampling:
    - no front-end electronics, direct straw cabling (coax, ∅=1.1mm)
    - op-amp & sampling ADC at back-end, waveform readout & processing by FPGA

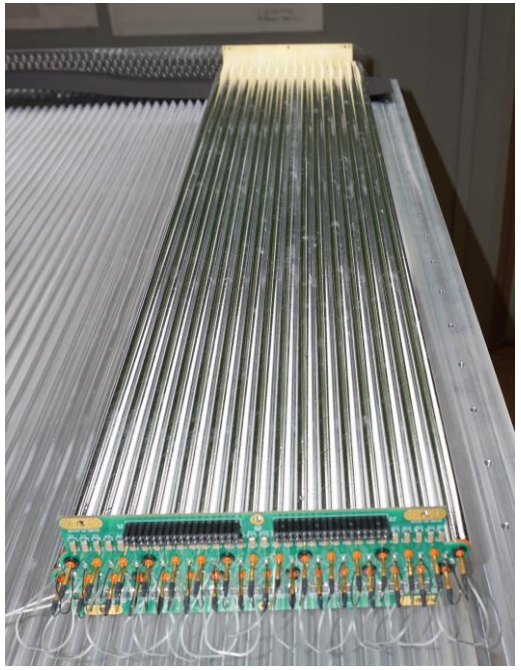
- Readout decision by Q2/Q3-2018
- Decision based on pre-series system setups and in-beam tests
- Decision process started, control panel installed, currently: definition of criteria & deliverables

- Pre-series system set up ongoing, HW available or in production

Status ASIC/TRB Readout

- ToT separation power for PID demonstrated by 2016´ in-beam tests
- Large signal dynamical range covered, dE/dx: ~ 5 - 50 keV/cm
- PASTTRECv1 - ASIC design verified, no design iteration necessary
- DAQ stable operation since ~ 1 year, 144ch test system, low NL, low thresh.

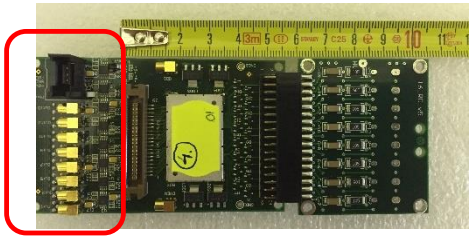
- ASIC/TRB3 readout system in phase-0 at HADES
- Two PANDA straw tracking stations with ~1800ch
- Set up during 2018, ready for beam 2018/19



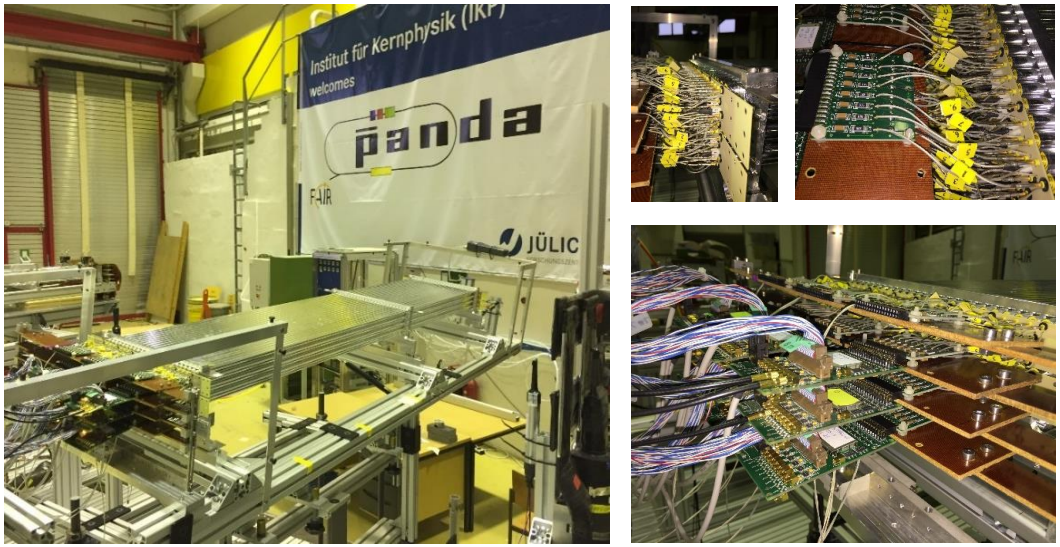
1st full STS1 module (2x16 straws) with FEE adapter board.

ASIC/TRB Test System

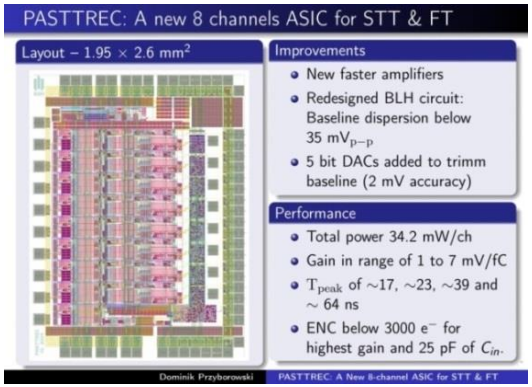
- FE-boards with 2 PASTTREC-ASIC (2x 8ch), analog out (skip in final layout)
- LVDS for 16ch out + ASIC ctrl (0.5mm micro TwPair, 20 pairs), LV supply (5V)
- TRB3 readout, ~256ch per TRB3 board, ASIC control by central FPGA
- SODANet for time synchronization of multi-board system
- DAQ system (CTS) with online monitoring (TDC rates)



FE-board with 2xASIC, HV board. Analog out (red box)



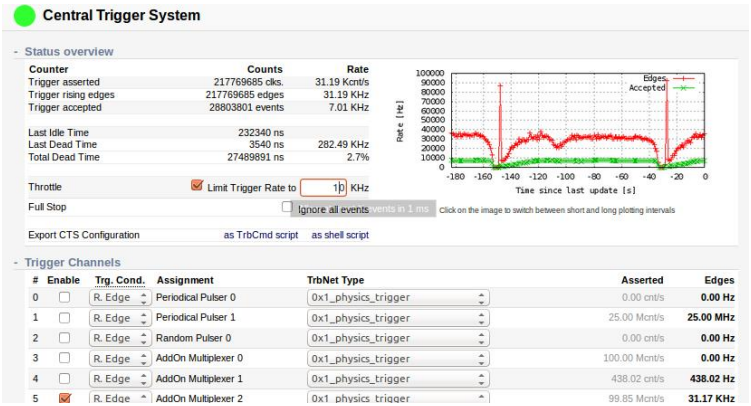
Straw test system and front-end electronics.



PASTTREC parameters (design by AGH Krakow)

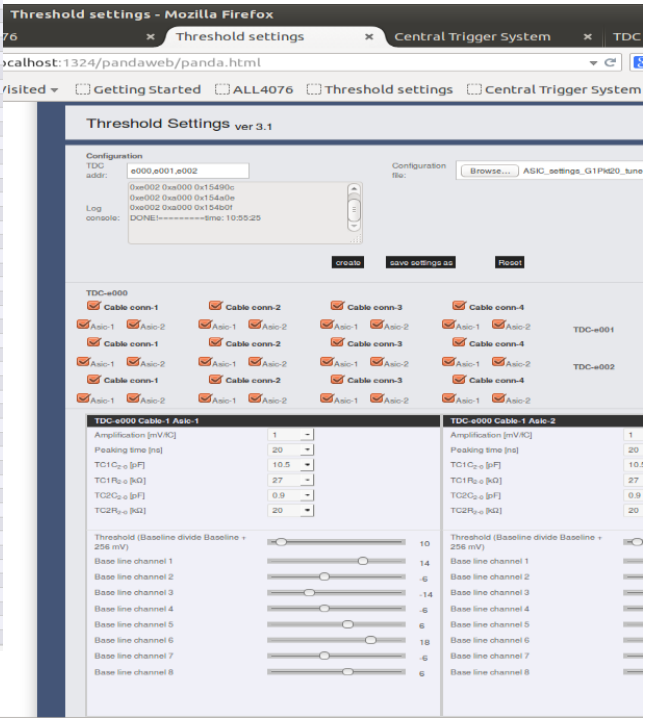
Readout DAQ & Control System

- By AGH & JU Krakow
- Central trigger system (CTS, GSI) for DAQ, external or channel trigger
- TDC registers, channel count rates monitor (ex. below, 6mV, no HV, 10sec)
- ASIC control (gain, PkT, TC, BL restor., thresh, individual ch BL ..)



Reg	Channel	e000	e001	e002
c000	0	32	32	32
c001	1	475	4	0
c002	2	0	0	0
c003	3	0	0	0
c004	4	0	0	0
c005	5	0	0	0
c006	6	0	0	0
c007	7	0	0	0
c008	8	0	0	0
c009	9	0	0	0
c00a	10	0	0	0
c00b	11	0	0	0
c00c	12	0	0	0
c00d	13	0	0	0
c00e	14	0	0	0
c00f	15	0	0	0
c010	16	0	0	0
c011	17	0	0	0
c012	18	0	0	8611
c013	19	0	0	0
c014	20	0	0	0
c015	21	0	0	0
c016	22	0	0	0
c017	23	0	0	0
c018	24	0	0	641
c019	25	0	0	0
c01a	26	0	0	0
c01b	27	0	0	0
c01c	28	0	0	6
c01d	29	0	0	0
c01e	30	0	0	10004
c01f	31	0	0	0
c020	32	0	0	2528
c021	33	0	0	0
c022	34	0	0	8023
c023	35	0	0	0
c024	36	0	0	0
c025	37	0	0	0
c026	38	0	0	16
c027	39	67	0	4
c028	40	0	0	6268
c029	41	0	0	0
c02a	42	0	0	1
c02b	43	0	0	0
c02c	44	31	0	0
c02d	45	0	0	0
c02e	46	0	0	0
c02f	47	0	67	239
c030	48	0	5	0

htm scripts

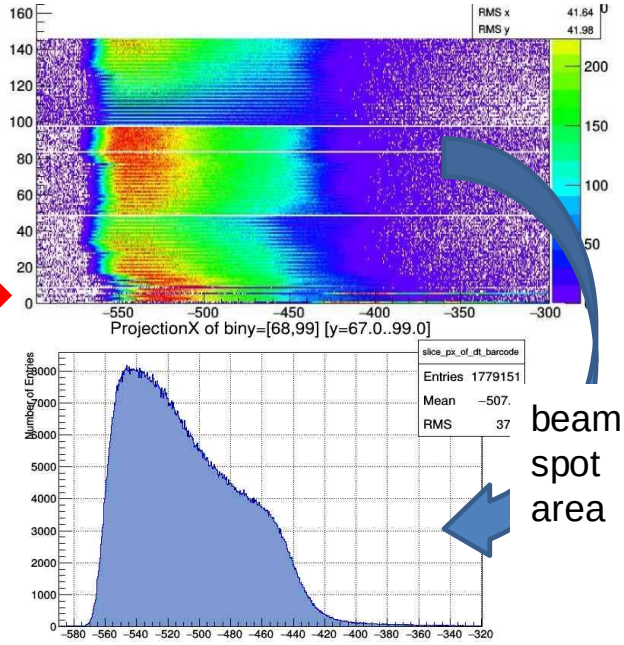


ASIC/TRB – Readout Status

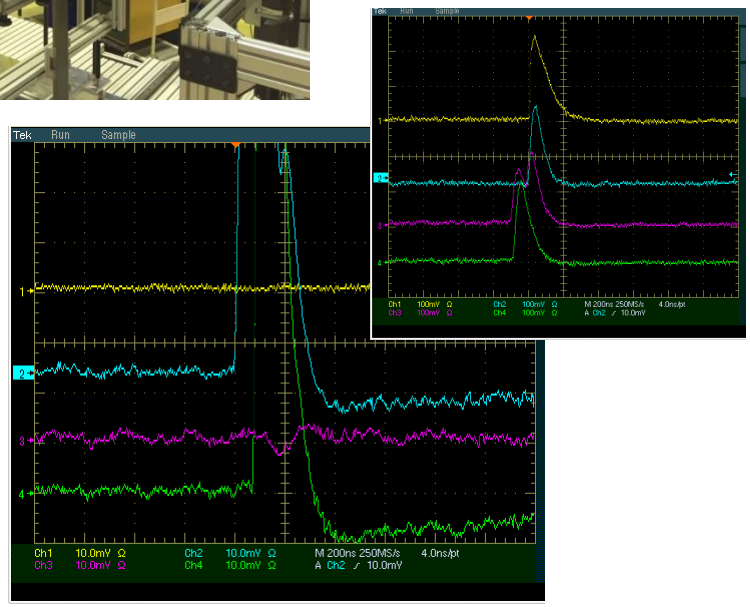
(Raw Spectra from April 2016 Beam Time)

In-beam position of straw setup (beam from the right)

FEB replaced later (ch1-16)

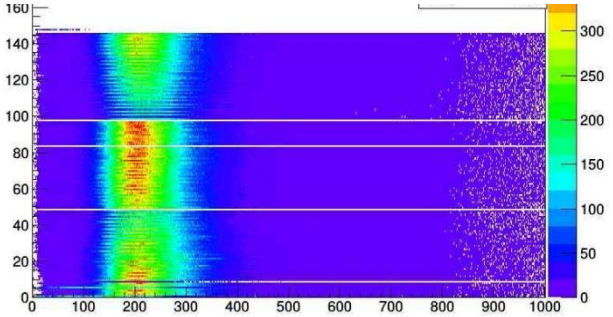


beam spot area



ASIC analog output signals (in-beam), NL <5mV (stable), thresh. at 10mV

TDC time (top) and time-over-threshold (below) vs channel

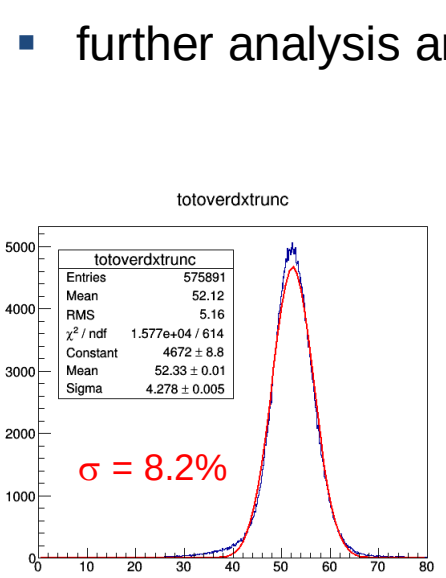


dE/dx Separation by Time-over-Threshold

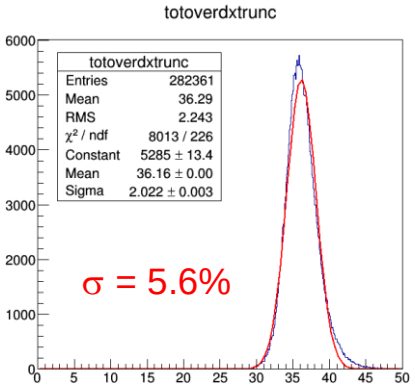
- ΣToT / Σdx per track seems better than Σ (ToT/dx)
  - better gaussian shape, only low truncation necessary
  - no ASIC saturation (e.g. ion TC) seen for 600 MeV/c deuteron (dE/dx ~50 keV/cm)

$$*S = \frac{\langle ToT_1 \rangle - \langle ToT_2 \rangle}{\frac{\sigma_1}{2} + \frac{\sigma_2}{2}}$$

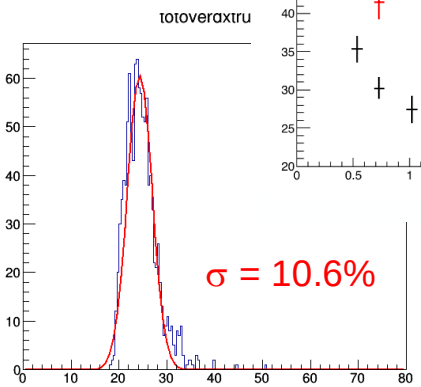
- prelim.: S ≅ 5.1 deuteron separation, compare to S ~ 9 in TDR (π/K at 0.23 GeV/c)
- very prelim: S ≅ 8.1 separation power for MIP & 600 MeV/c deuteron
- further analysis and improvements ongoing



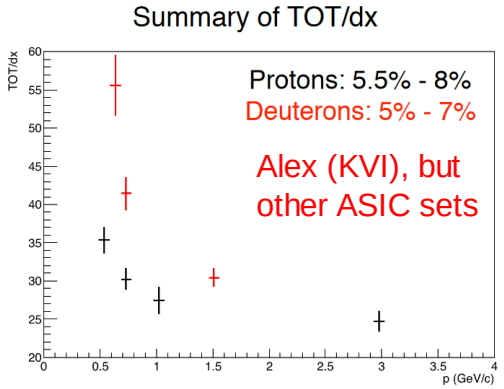
600 MeV/c deuteron



1500 MeV/c deuteron



Cosmics (MIP)



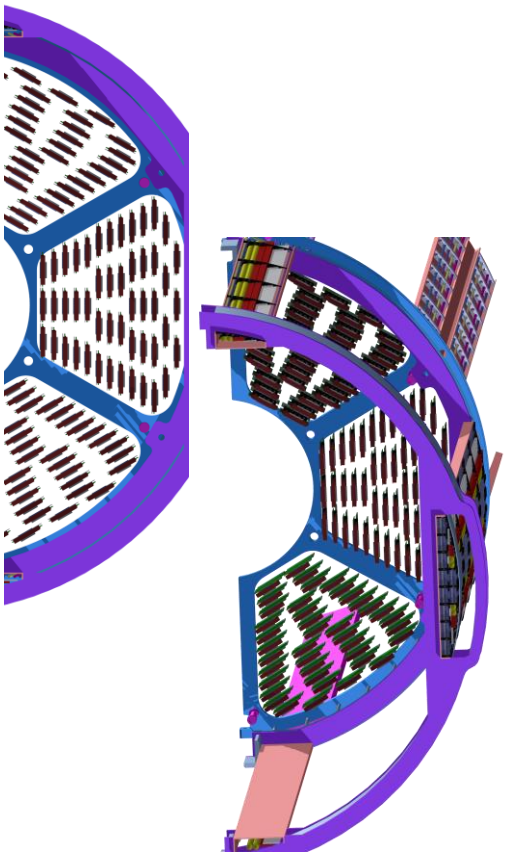
ASIC/TRB Front-End Layout

Tasks done:

- Positioning of 134 FE boards per semi-barrel and
- Individual straw and FEB-channel association
- Challenging for close-packed straw geometry with increasing straw number in radial layers

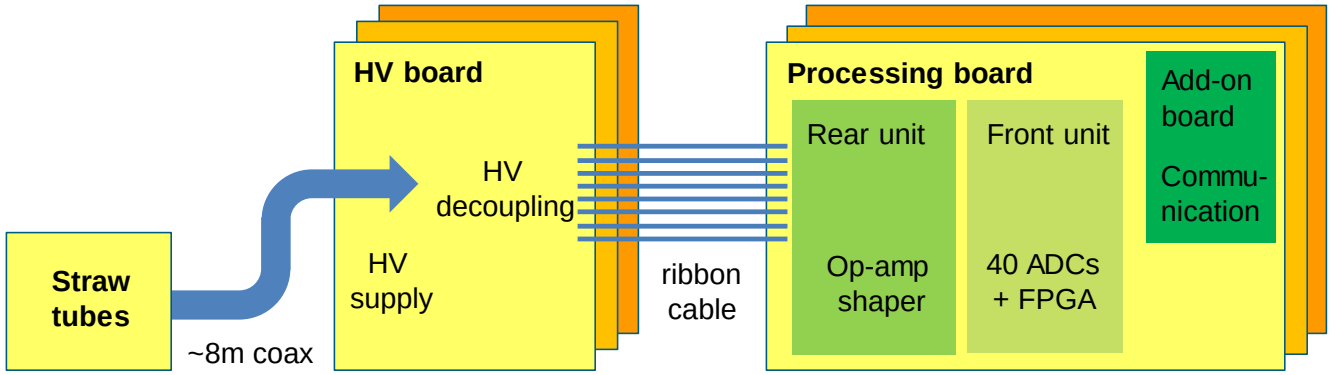
Next:

- One STT sector set up as pre-series system
- Cable routing scheme
- Cooling scheme for 2x64 Watt (forced convection)



ADC-Based Readout System

- “Front-end electronics free”
- Direct straw cabling, mini coax (∅=1.1mm), tested HV stable
- HV supply, HV decoupling backend
- Integrated op-amp, ADC and processing FPGA, add-on communication
- 3-stage op-amplifier, 20ns PkT, gain factor 400, 20 MHz BW, 100 mW
- Low power 4-ch ADC (HMCAD1520), 160 MSPS, interleaving mode (1000MSPS)
- One central FPGA (Xilinx Virtex 7) for 40 ADCs per readout board (160 ch)

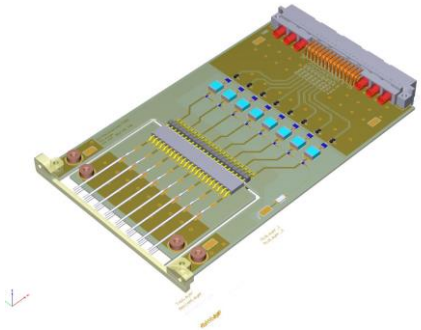


Scheme of ADC-based readout system

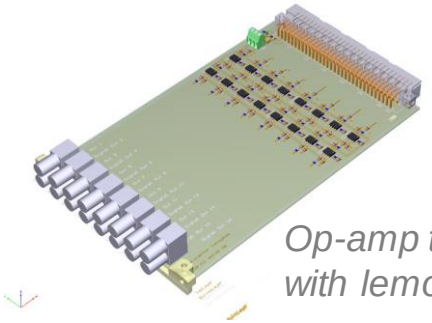
HW Designs

- HV crate with decoupling boards, coax lines with plug instead of soldering
- Samtec ribbon cable to processing crate, cross-talk tests next
- Testcrate with additional amp-board for test of signal analog part
- Pre-series (final) crate with more slots (416 ch per crate, 26 boards)

HV crate for tests with HV decoupling boards and additional amp board.



HV supply and decouple board. Plug for coax lines.



Op-amp testboard with lemo out.

Samtec ribbon cable (2x16ch)

Status ADC-based Readout

- 16 ch prototype test in-beam in 2016
- Amplifier characteristics verified (2x diff. gain factor + logarithmic tested)
- Signal processing algorithms developed
- Different ADC sampling rates and influence on time/spatial resolution tested

- Pre-series system set up next, ~ 400 ch, in-beam tests
- HW in production, RO board available in September for 1st HW tests
- DAQ system set up and tests
- Cosmic tests prior to next beam time

Summary

- Pre-series system set up (~ 400 ch) for both readouts in Q4/2017
- Cosmic tests (extended) next

- Beam time planned for March + April 2018
- Proton and deuteron beam at COSY, 0.5 – 3.0 GeV/c, dE/dx ~ 5-50 keV/cm

- In-beam tests for both readout systems
- Performance results as basis for readout decision
- Further criteria to be considered (costs, maintenance, ..)

- Readout decision planned for Q2/Q3 2018
- Then: full integration of readout system into PANDA (mech., DAQ, simu., ..)

JÜLICH FORSCHUNGSZENTRUM

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Thank you for your attention