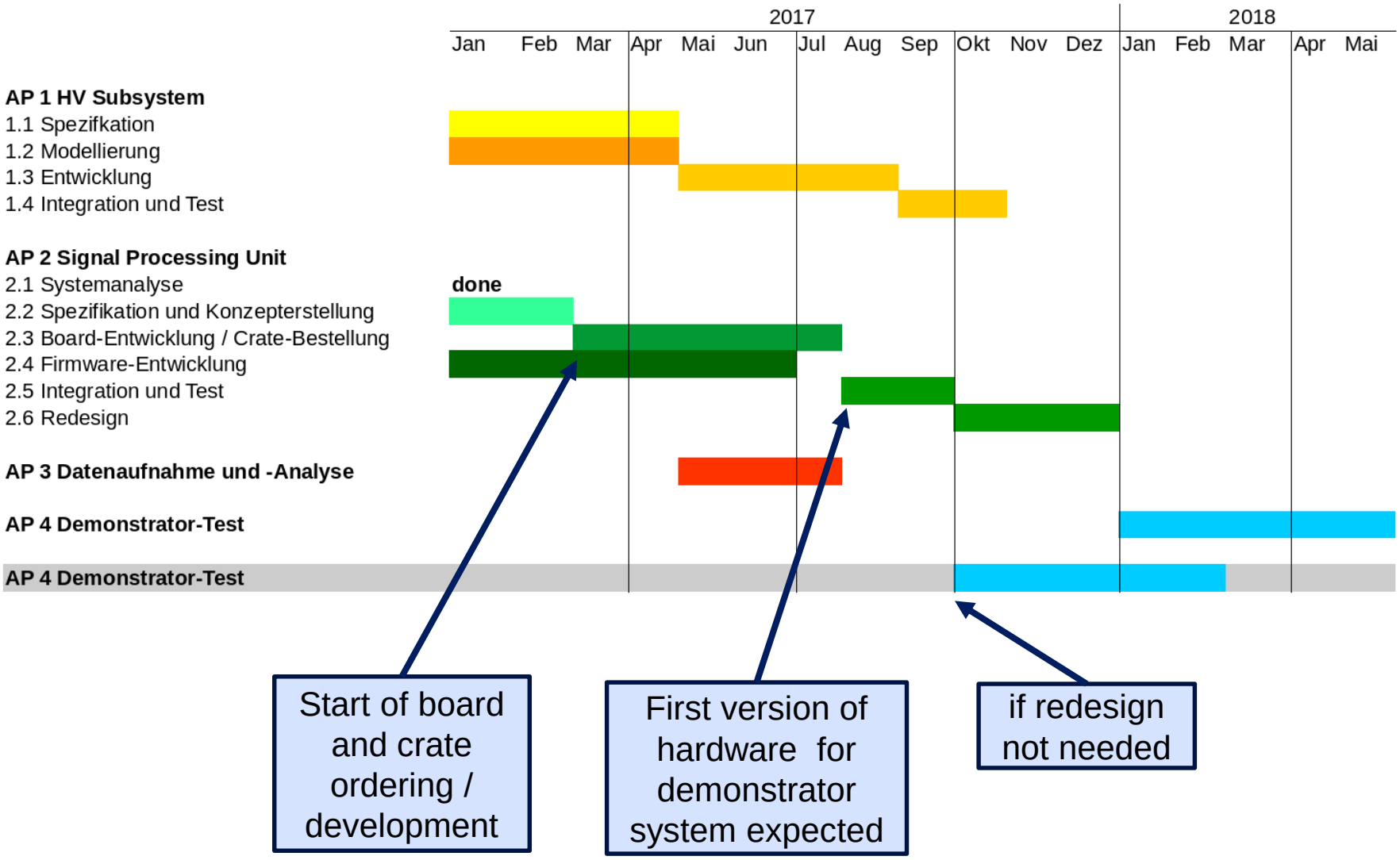
JÜLICH
FORSCHUNGSZENTRUM

PANDA STT Readout meeting

Status of ADC-based DAQ

15.05.2017 | A. Erven & L. Jokhovets

Timetable



Signal Processing Unit

Rear Transition Module (pre-Amplifier)

- Specification completed
- Schematics started

Processing Module (Sampling and Processing)

- Specification completed
- pre-Work for layout and definition of layer stack started

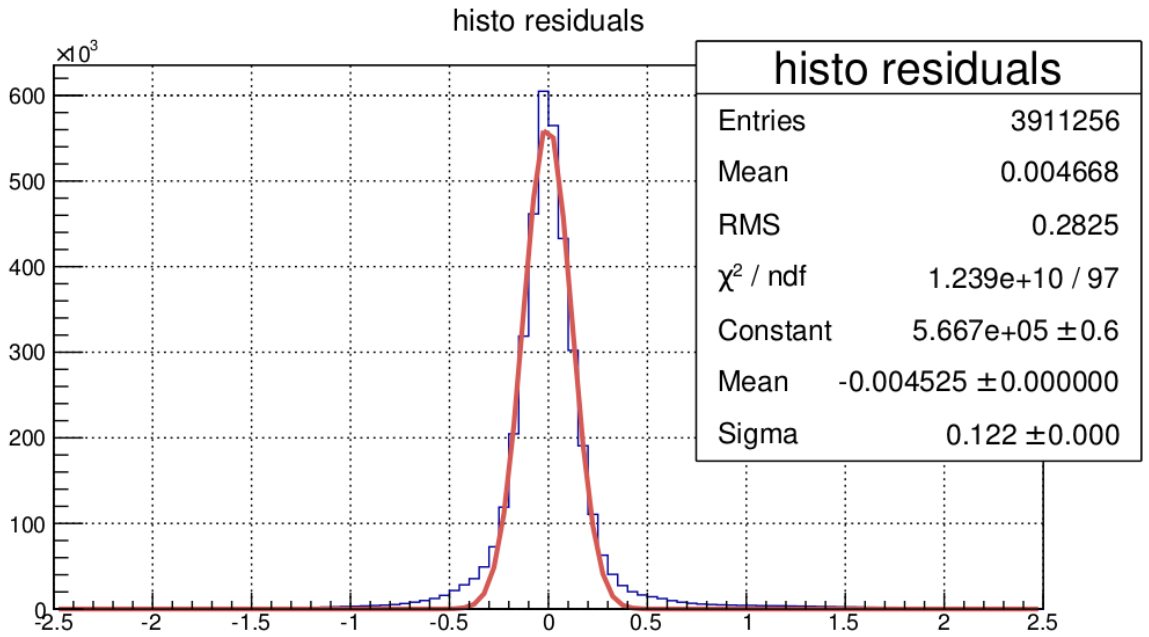
Crate-System

- Specification completed
- Order to be given soon

Tasks from Krakow workshop

Data analysis

- Results of analysis presented in Krakow confirmed by independent analysis from Krzystof:



Tasks from Krakow workshop

SODANET

- Communication with Myroslav
- Selected FPGA fits to existing designs for SODANET endhub
- Required Jitter-Cleaner will be included in design

→ Readout system designed to be SODANET-compatible