# STT Readout Meeting

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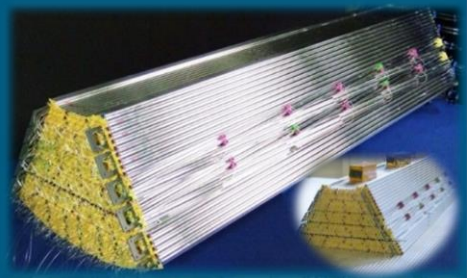
**eZuce | May-15th, 2017**



# Meeting Agenda

- Welcome
- Minutes Krakow Meeting & Open Points
- Readout Decision Process
  - Organisation/Timelines/Beam Requests
- Criteria & Deliverables for Decision
- Specific Topic: PANDA-DAQ implementation
- Decision Points for Today
- Next Meeting & Points
- Readout Status Updates

# Welcome

- Holger Flemming (PANDA experiment electronics) joined us for the Readout Decision Process
- Michael Kunkel (Postdoc in Juelich, CLAS@JLab) joined STT group
- Pawel Strzempek (JU Krakow) with successfull Ph.D. defense last week
- Alex & Solmaz (KVI Groningen) about to finish Ph.D. by end 2017

# Next: Meeting Minutes & Open Points

# Krakow Meeting Minutes

- Readout decision process started with Krakow workshop (Jan-30/31)
- Status reports (13) from all groups, discussion of next steps

- Discussed to set up “Decision Panel” to control the process (almost done)
- Timelines of readout decision process presented, aim for decision in Q2-2018
- Started to set up list of criteria & deliverables for the decision (continue today)

- TRB3 readout – SODANet implementation presented by Greg K.
- Official note: TRB3 HW suited for phase-1, but not phase-2 (GbE - BW limit per TRB3)
- TRB HW upgrade considered as general GSI/FAIR project, multiple interests in community

- PASTTRECv1-ASIC, no design change necessary from 2016 beam tests, 5-50 keV/cm dynamical range covered with no (ToT) saturation seen
- Next ASIC production (PASTTRECv1) submitted (additional phase-0 straw setup, 1600ch)
- PCB FE-boards with slight re-design (reduced size, w/o analog output ch), design in progress

- ADC / op-amp prototype (14 ch) in-beam tested (Dec-2016), time/spatial resolution aims fulfilled, input for pre-series board design (design finished & HW in production in the meantime)

# Open Points

Decision points for today:

- Decision process organisation, timelines, test systems & measurements
- DAQ specs for test measurements: (clock) trigger, ch rates, data buffer
- PANDA-DAQ (SODANet) implementation, necessity before RO decision?
- Agreement on readout capabilities / restrictions
  - ASIC/TRB readout: on purpose readout restriction to time, time-over-threshold
    - ASIC with parallel analog signal outputs, only used for prototyping/debugging
    - reason: limited detector front-end area, reduced PCB, power&cooling, #cables
  - ADC-based readout with full waveform sampling
    - only time, pulse area (= charge info) up to now
    - option of additional pulse/waveform data: (i.e. peak ampl., TE-time, BL, NL, ..)
    - implications for readout FPGA / board design, data buffer, bandwidth-limit
- Readout system / cable layout
  - STT front-end – cabling – RO rack ↔ PANDA installation & STT maintenance
  - one-step installation scheme preferable, cable routing to top-first RO racks

# Next: Decision Process Organisation

# Decision Process Aims

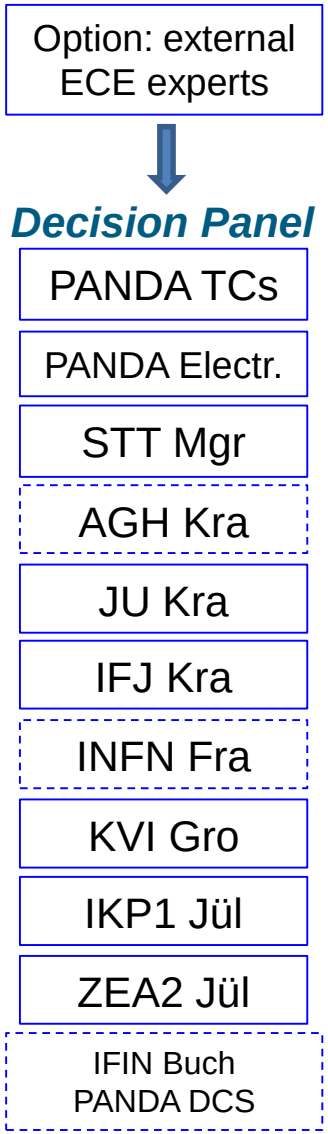
- Set up “pre-series” systems for both readouts with close to final layout
  - In-beam tests, high signal dynamical range & rates: 2× ~400 ch straw detectors
  - Set up one complete STT sector (700 ch) for ASIC/TRB readout (front-end area)
- Approval of system readiness
  - verify fulfillment of certain criteria & deliverables
  - techn. specs & financials
  - robustness & complexity (maintenance, work load, MP)
- “Pre-series” test of readout system is part of official milestone FAIR-M8

- After decision: enter final production stage, slight re-designs not excluded
- Full integration of the RO system into PANDA: mechanics, DAQ, simulation & analysis
- Test system (straw + RO) available for PANDA-DAQ implementation

“Failure-free” STT readout system mandatory for PANDA running

# Decision Process Organisation

- Set up a Decision Panel for process control (done)
  - One person from each involved STT group
  - PANDA-integration aspects: TCs(2), Exp-Electr.(1), STT-Mgr
- Option: in case of ambiguous opinions, add two external experts from ECE panel (STT evaluation)
- Task of decision panel:
  - verify readout system designs & requirements for PANDA-STT
  - define criteria & deliverables for the decision (official document)
  - address open points early (but HW main designs finished)
  - evaluate both systems
  - decide on best-suited readout



# Timelines for Decision Process

- Jan-17: Start of readout decision process with Krakow meeting
- May-17: process organisation, decision points, status updates, beam requests
- Jun-17: COSY beam meeting (CBAC) in Jülich (beam for ≥ Mar-2018)
- July-17: next eZuce meeting (propose), status updates
- Sep-17: status update of readout systems
- Dec-17: status of cosmic run tests and preps for beam time in Q1-2018

- Q1/Q2-2018: in-beam tests, proton & deuteron beams at COSY
- Q2-2018: reporting on final results
- Q2-2018: decision on final readout system

PANDA-STT system timelines:

- End-2021: PANDA-STT site acceptance test (FAIR-M9), option: COSY tests
- 2022: STT system ready for installation at FAIR
- 2023: system readiness for beam

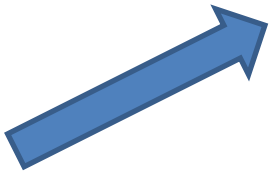
# WP Organisation

- MP situation very critical, will remain critical, account for in decision process
- Exploit experiences & synergies (same analysis SW, calibration&tracking methods)
- Focus on most important issues

- Workpackage (WP) organisation
- Contact person(s) for each WP
- 3 contributing groups for each system

WP.org example

| FE/Analog |
|---|
| Digitizer |
| DAQ |
| Online/FPGA |
| Offline Analysis |
| Install & Tests |



| ***ASIC/TRB-RO.org*** | ***ADC-RO.org*** |
|---|---|
| ASIC: Marek/Tomasz | HV-decouple/cables: Thomas, Henner |
| FEB, cables: Marcin | Amp/ADC: Andreas/Ljuba |
| TRB3/DAQ: Greg | Online/FPGA: Ljuba/Pawel K. |
| Online/FPGA: Greg | DAQ: Andreas/Ljuba |
| Test systems: Peter/Michael | Test systems: Pawel K., Krzysztof, Valeriy |
| STT-FE: Peter/Artur | |
| Offline analysis: Peter | Offline analysis: Krzysztof |

merge (ROOT analysis, cuts, filters, calibration, tracking)

# MP & Financial Resources

- MP calculation needed (FTEs / year) for
  - RO system production & installation, test procedures
  - Recipe for install & tests has to be set up
  - Maintenance: system operation & set-up (roll-in & -out once per year)

- Costbook for pre-series systems to be collected (complete)
  - All components, manufacturing, design works, testing
  - Collection of all production steps
  - List of all involved manufacturers

- Solid calculation of no. of spare components for final system, implement expected/experienced failures (PANDA running time 6 months/year x 10 years)

# Testbeam Request

- Proton/deuteron beams at COSY well suited, dE/dx range ~ 5-50 keV/cm, broad/narrow beam spot possible
- Set up beam area and beam tunes in 2016 completed
- 3(4) diff. momenta was set up by COSY per beam week
- Beam intensity / beam profile can be changed by ourselves

- Testbeams proposed for readout decision (plan, to be requested and allocated)
  - 1 week proton beam in Mar-2018 (earliest date)
  - 1 week deuteron beam shortly after (break for beam target source change)
  - 3x diff. momenta for each beam week

- Optional beamtime in 2018 at COSY
  - PANDA-DAQ tests
  - (would prefer after readout decision, takes time to prepare)

# Next: Criteria & Deliverables for Decision

# Criteria & Deliverables for Decision: Basis

- Readout requirements for PANDA-STT, basis is
  - STT-TDR document
  - Evaluation report from ECE-panel, full TDR approval, recommendations how to proceed with STT
    - Final system prototype/ spare module to conduct a production readiness review
    - Expose electronic chain to full dynamic range of pulse heights by in-beam tests
    - Failure studies!, ..

- New situation: staging of PANDA luminosity
  - Phase-1: reduced lumi with L $\times 1/_{20}$, phase-2 with full lumi L
  - First running years with less intensities and data rates

- Option to have RO staging & upgrade for phase-2 (if cost-effective of course)

# Overview: Test Systems & Measurements

- Two straw test systems for both readouts (in progress, straws avail.)
  - each with ~ 400 straws, 16 layers x 24 straws, ≥ 24 hits per track (≅ PANDA-STT)
  - full readout chain and all components, ~ 8-12m cabling length front- to back-end
  - in-beam tests, some aging expected, no later use of straws in PANDA
- One complete STT sector in prototype frame (to be done, Q1-2018)
  - ~ 700 straws, final straw modules, mounting techniques & alignment checks
  - front-end electronic area design & cooling for ASIC/TRB system
  - only cosmic tests, straw sector modules can be used later
- Beam tests at COSY
  - Proton/deuteron beams, 0.5 – 3.0 GeV/c, dE/dx range ~ 5-50 keV/cm
  - High particle rates, signal dynamical range, BL/shaping stability, DAQ tests
- Cosmic data-taking (MIP)
  - Clean tracks, vary track angles (signal propagation time), precise timing
  - Spatial resolution and efficiency determination

# Main Criteria for Readout Decision

- Signal pulse and pulse shape detection capability
  - ASIC properties, LE-/TE-time detection in TRB-FPGA
  - Op-amp/ADC props and waveform analysis (FPGA, SW)
  - High-rate and high signal dynamical range, hit detection efficiency & resolution
  - ~ 400 channels test systems, channel divergence
- Drifttime measurement by signal leading edge time
  - Time resolution, spatial isochrone resolution and radial efficiency
  - Method: r-t isochrone calibration, $\chi^2$ - track reconstruction, residuals
  - Final system resolution (mech. system, calibration, SW, tracking, ..)
- Energy-loss measurement by signal pulse shape
  - Pulse width (ASIC/TRB) or pulse area (ADC)
  - Calibration methods, channel divergence (amplifier dispersion)
  - dE/dx separation power, different proton momenta, proton/deuteron at same momentum

# DAQ Criteria

- Bandwidth limit test per readout board
- Time synchronization for multi-boards
- Data buffer, single channel rates, time window with time ordered hits

- Possible DAQ rates with straw in-beam tests (particle bunch & bursts at COSY)
  - straw space charge effects limit max. single chan. hit rates: ~ $1.5\times10^4$ $cm^{-2}$ $s^{-1}$
  - ~ $1\times10^5$ $s^{-1}$ trigger limit if broad beam (broad spot ~3×3 $cm^2$)
  - ~ $5\times10^5$ $s^{-1}$ max. trigger for short period with space charge effects
- ~ $4\times10^6$ hits/s per readout board (100 straws, $4\times10^4$ hits/s each straw for clean signals)
- ~ 20 MB/s DAQ (5 Byte data word ?), clean signals
- ~ 100 MB/s DAQ short periods for max. bandwidth test

- Phase-1: 50 / 20 MB/s (max./avg.) per board, can be tested with beam by us without problem
- Phase-2: = Phase-1 × 20

# DAQ Modes & Test Criteria

1. Beam trigger (=scintillator): clean timing for straw hits
2. Beam trigger + large time window (~2µs): ch multi-hit detection, ~ 350/700 ns COSY extraction time structure
3. Record additional reference time channel (beam scintillator) for timing tests, multi-hit detection, ..
4. Clock-trigger: ..

1. Cosmic data-taking: long-term stability, clean tracks, rates ~ few Hz

# Criteria & Deliverables for Decision

- Which information
- How to compare both systems (some different features)
- Which format ..

- .. Propose to set up specs tables, examples next slides, to be discussed ..

# Technical Specifications STT

| Item | Pre-series In-beam | PANDA Phase-1* | PANDA Phase-2 | Remarks |
|---|---|---|---|---|
| No. of straws | ~ 400 | 4224 | 4224 | |
| Gas mixture, pressure | Ar/CO2 (20±10%), 2 bar | | | |
| Gas gain (default) | 5x $10^4$ | | | HV=1800V (10% CO2) |
| Max. drift times | 140-200 ns (B=0T) | 200-250 ns (B=2T) | | Ar/CO2 (20±10%), |
| Time resolution (σ) | 1 ns | | | 1ns ≅ 50 μm |
| Spatial resolution (σ) | < 150 μm | 150 μm | | |
| I.P. for MIP | 185 I.P./cm | | | Ar/CO2 @ 2 bar |
| Charge dynamic range (eff.) | 2 – 200 fC | | | 2 fC = single cluster charge @ 5x$10^4$ gas gain, 10% eff. signal |
| dE/dx dynamic range (eff.) | 5 – 50 keV/cm | | | Ar/CO2 @ 2 bar |
| Max. no. hits / straw | 5× $10^4$ $cm^{-2}$ $s^{-1}$ (space charge limit) | 5× $10^4$ $s^{-1}$ | 1× $10^6$ $s^{-1}$ | Innermost layer |
| Avg. no. hits / straw | 2× $10^4$ $cm^{-2}$ $s^{-1}$ | 2× $10^4$ $s^{-1}$ | 4× $10^5$ $s^{-1}$ | all layers |
| Data rate per channel (max / avg) | 250 / 100 kB/s | 250 / 100 kB/s | 5 / 2 MB/s | for 5 Byte data word |
| Avg. no. of events | 1-2× $10^5$ $s^{-1}$ | 1× $10^6$ $s^{-1}$ | 2× $10^7$ $s^{-1}$ | Pre-series with single beam tracks |

**Phase-1 with factor 20 less luminosity than nominal*

# Tech. Specs: Readout Systems

| Item | ASIC/TRB | ADC-based | Remarks |
|---|---|---|---|
| Readout method | Discriminator with signal leading & trailing edge detection | Waveform sampling and pulse shape analysis | |
| Time resolution (delta-peak) | 1 ns | | |
| Readout boards | TRB3, TDC in FPGA technology, central FPGA | Sampling ADC, central FPGA readout | ADC: HMCAD1520, 12-bit, 160MSPS in quad-ch mode, FPGA: Xilinx Virtex 7 |
| Channels per readout board | 192 | 160 | 40× ADC(4ch), 1× FPGA |
| Readout HW | “PASTTREC”-ASIC as amp/shaper/discriminator, TRB3 | Custom op-amp, commercial ADC/FPGA | |
| Special features | Online adjustable gain (1-7 mV/fC), BLs, thresh., shaping parameters | higher ADC sampling in double-/single-ch mode, full wave form | Waveform information, BL determination, leading edge detection, signal area summation |
| Data word / output information | $time_{LE}$, time-over-threshold | $time_{LE}$, signal area | |
| Optional output | | | Additional data from ADC? BL, NL, max. amplitude, .. online monitoring? |
| Online monitor | Single channel TDC rates | | |
| TDC window/binning (typical) | 1 µs / 0.5 ns | | |
| Data buffer (epoque) | 500 µs | | |
| Data single word size | 5 Byte | ??? | TRB: ch, time, tot<br>ADC: |
| Data rate / board at full luminosity | 400 MB/s | | Inner-/outer layers to one board |

# Specs: Performance Tests & Results

| Item | | ASIC/TRB | ADC-based | Remarks |
|---|---|---|---|---|
| HW stability | BL, NL, thresh., amp, . | | | ~ 400 ch system |
| DAQ stability | In-beam / cosmics | | | |
| Drifttime measurement | Time resolution (test pulse) | | | |
| | Spatial resolution | | | Cosmics, mip |
| | Efficiency (radial) | | | Cosmics, mip |
| | Sensitivity | | | Threshold for pulse detection, 55Fe |
| | Time calibration method | | | |
| | Hit efficiency | | | |
| | Double-pulse resolution | | | After-pulse |
| dE/dx measurement | Covered range (5-50 keV/cm) | | | Amp/shaping saturation test |
| | Resolution | | | pulse width / pulse area |
| | Calibration method | | | |
| | Hit efficiency | | | |
| PID / separation power | Diff. proton momenta | | | |
| | Proton/deuteron at same momentum | | | |
| DAQ operation | Max. readout rate (in-beam) | | | |
| | Buffer time window | | | |
| | Deadtime / data-loss | | | |

# Next: PANDA-DAQ Implementation

.. Open discussion ..

.. PANDA-DAQ TDR & tests

.. ASIC/TRB3 readout system for PANDA-FT decided (?!)

.. STT readout system, at first: take decision which system, then available for DAQ tests

# Next: Decision Points Today

# Decision Points for Today

- Decision process organisation, timelines.. approval
- Test systems & measurements approval
- General system HW approval
- General system layout (front-end – cabling – RO rack) approval

- Open point: ADC waveform sampling and additional information (SW issue)
- Any other missing points?

- PANDA-DAQ implementation necessary/possible (man power)?
- Readout decision w/ or w/o SODANet / PANDA-DAQ (hardware setup)

- Topics for next meeting, propose meeting date in early July
- Any other topic?

# Next: Readout Status Updates