Minutes of the Krakow STT Readout Meeting (January-30/31, 2017) and connected incidents

The STT readout decision process started with the dedicated meeting workshop in Krakow on 30/31st of January this year. In total 13 status reports from all groups were given and the next steps werde discussed. (all presentation slides are listed on the meeting web page: https://indico.gsi.de/conferenceDisplay.py?confId=5290).

It was proposed and agreed to set up a so-called "Decision Panel" to control the decision process. Members of the panel are: 1 person from each involved STT group, STT SysMgr, PANDA electronics and PANDA techs representatives. In the meantime persons were contacted and formally agreed to join the panel.

Timelines for the readout decision process were presented and the aim is to take a decision in Q2/2018. Prior to this beamtests have to be executed for both readout systems which are planned for Q1/Q2 in 2018 at COSY. Beam time still has to be approved and scheduled by the CBAC in Jülich.

A list of criteria & deliverables (c&d) for the readout decision was started, containing technical specifications, test systems and measurements. The c&d list definition is still ongoing and is a major topic for the next meeting (taking place Monday, 15th of May).

Some selected specific and important information:

Greg K. reported on the TRB3 readout and SODANet implementation. The STT group puts an official note that the TRB3 HW is suited for the PANDA phase-1 experiment, but not for the phase-2 with full nominal luminosity. The limiting factor is the bandwidth limit per TRB3 readout board (GbE links). The STT group considers a HW upgrade of the TRB architecture as a general GSI/FAIR project, due to the multiple interests in the community with many groups using TRB readout systems.

For the STT specfic PASTTRECv1-ASIC it was stated that no design change or iteration is necessary. During the 2016 beam tests at COSY, with proton and deuteron beams covering a large dynamic dE/dx range of about 5-50 keV/cm, no (ToT) saturation was seen. Peter also pointed to the stable operation (low thresholds, no intrinsic oscillations) of the ASIC and much better handling compared to the ASD8-ASIC architecture for instance.

In the meantime, a next ASIC production (same PASTTRECv1 design) was submitted, in particular to not risk the additional phase-0 straw setup with about 1600ch readout channels. The PCB FE-boards will undergo a slight re-design, the additional analog output part will be skipped for the STT version to save space and reduce power consumption.

The FPGA/ADC/op-amp prototype (14 ch) was tested during the beam time in Dec. 2016. The obtained time/spatial hit resolution fulfilled the design goal, so that the next step of a pre-series readout board design could start. In the meantime the design is finished and the HW is in production. The pre-series readout boards are scheduled to become available by September this year. In case of initial HW test malfunctions a slight re-design and next board availability within 3-4 months is planned.