



# Update on SciTil hardware development

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### **Attenuation**

- Attenuation measured with SiPM pulses
  - Extrapolated to full length board
- Linear loss of 26% of maximum amplitude per meter
- Rise time increases by 0.13 ns per meter



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## Crosstalk

- Using sinusoidal signal •
- SiPM Signal risetime in order of • **1 ns** 
  - corresponds to 350 MHz >
  - Approx. 2.5% crosstalk level
- **Crosstalk level higher for** • vertical neighbours
- With a real signal crosstalk only • appears with >1V amplitudes (above expectation)
  - At a approx. -53 dB (0.2 %) level for 1.5 V





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## **Railboard Design Update**

- Signal shields merged and width reduced
- Potential thickness increase to 35 μm
- Width of area occupied by connections reduced
  - → material budget reduced
  - Previously approx. 2.4%  $X_0$

		0,2 mm 0,36 mm 0,3 mm	
Тор	1	SG1	18 μm Cu
	_	0,29 mm	100 µm FR4
	2	S1 S1	18 µm Cu
	-	0,18 mm	100 µm FR4
	3	SG1&2	18 µm Cu
	4		100 µm FR4
	4	52	18 μm Cu
	5	\$G2&3	E
	6	S3	E
	7	SG3&4	E
	8	<b>S4</b>	2 mm
	9	SG4&5	E I
	10	S5	E
	11	SG5&6	E
	12	S6	E I
	13	SG6&7	E
	14	57 S7	E
	15	SG7	E
Bottom	16	}	
		Screening ground	anal ground



## **Railboard Design Update**



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## **SiPM Configuration**

- SiPMs will be connected in series or in hybrid<sup>[1]</sup> configuration (insert image right)
- Simplifies readout (1 channel for 4 SiPMs)
- Serial connection improves signal rise time
- Hybrid connection can only provide one voltage value to all 4 SiPMs





[1] Inspired by MEGII: arXiv:1301.7225

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8/10

TOFPET ASIC by PETsys Electronics

number of



## Front End Electronics (FEE)

#### Data will be processed by • the TOF PET ASIC produced by the company PETsys **Flectronics**



### SiPM famil on-chip circuit max channe max output Fully digita operation f power per o

number of channels	64	
TDC time binning	50  ps (25  ps optional)	
intrinsic time resolu- tion	21 ps r.m.s.	
charge measurement	time over threshold (ToT)	
dynamic range	$300 \ pC$	
${ m SNR}~({ m Qin}=200~{ m pF})$	25  dB	
coarse gain	G0, G0/2, G0/4	
SiPM familiy support	positive or negative sig- nal polarity	
on-chip calibration circuit	internal pulse genera- tor, programmable 6- bit amplitude	
max channel hit rate	160 kHz	
max output data rate	$\begin{array}{ccc} 320 \hspace{0.2cm} \mathrm{Mb/s} \hspace{0.2cm} (640 \hspace{0.2cm} \mathrm{Mb/s} \\ \mathrm{with} \hspace{0.2cm} \mathrm{double} \hspace{0.2cm} \mathrm{data} \hspace{0.2cm} \mathrm{rate}) \end{array}$	
Fully digital output	2 data LVDS links, DDR compatible	
operation frequency	80-160 MHz	
power per channel	8-11 mW	
SiPM HV fine biasing	range $500 \text{ mV}$	

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## Outlook

- Get the evaluation kit up and running again
- Do first timing measurements to familiarize myself with the ASIC
- Talk to PETsys about custom FEE development
  - We might reuse some commercial components





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