BERGISCHE UNIVERSITÄT WUPPERTAL

The DIRICH development - overview and first measurements

C. Pauly, Wuppertal university
for the CBM- HADES- and TRB collaborations

Contents:

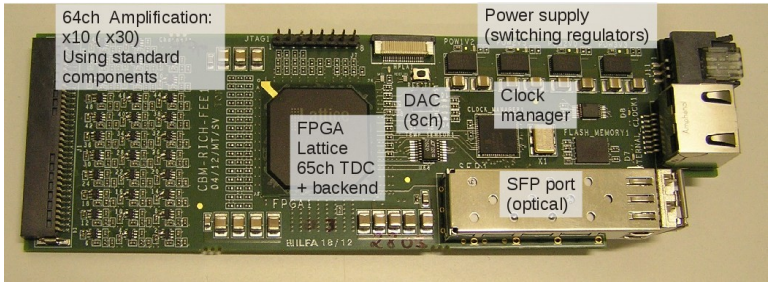
BERGISCHE UNIVERSITÄT WUPPERTAL

The way to DIRICH ...

Motivation: Readout for the **CBM RICH detector with ~1000 MAPMTs**, 64ch each
Use same PMTs and readout also for **HADES RICH (480 MAPMTs)**

Requirements: Powerful, inexpensive readout for ~60k channels,
good timing precision (better 1ns)
high rate capability, self-triggered, ...

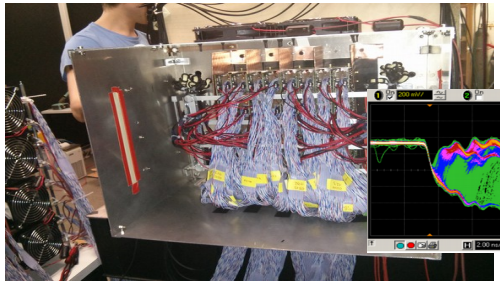
2012: 64ch TRBRICH module



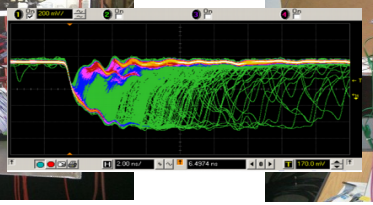
64ch FPGA-TDC (Lattice ECP3)
monolithic preamplifier (32ch on each side !)
discrimination and TDC on same FPGA
TRBnet data link via SFP

- worked in principal
  – but a bit to ambitious as first step
  – problems with analog input stage
  – no ToT

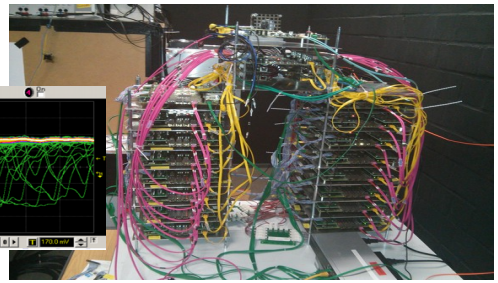
2014: PADIWA + TRB3



RICH prototype with
64 PADIWA modules



Digital signal
after cable



TRB3 stack
with 18 TRB3

Same principal,
but separation of discriminator (PADIWA) and TDC (TRB3)

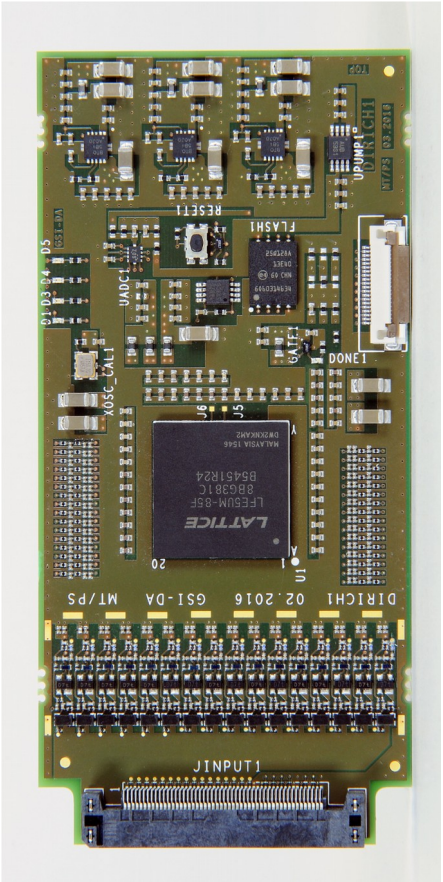
- It worked ! (→ thanks again for providing the components !)
- But quite a cable mess !

- Some problems with cross talk and efficiency
  - due to short digital pulses via LVDS flat cable

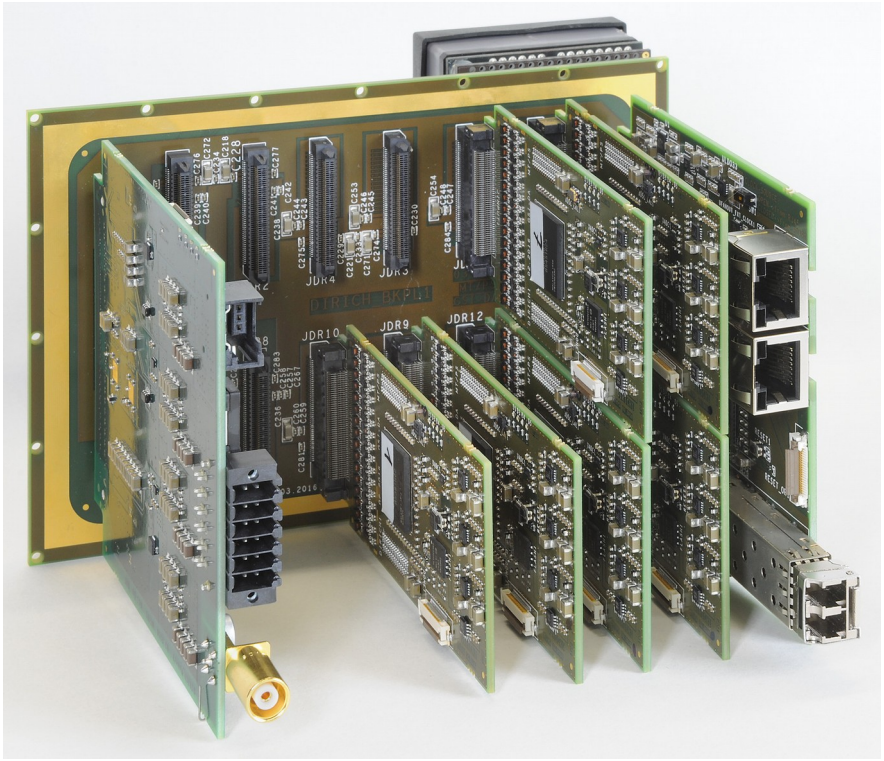
BERGISCHE UNIVERSITÄT WUPPERTAL

The DIRICH concept

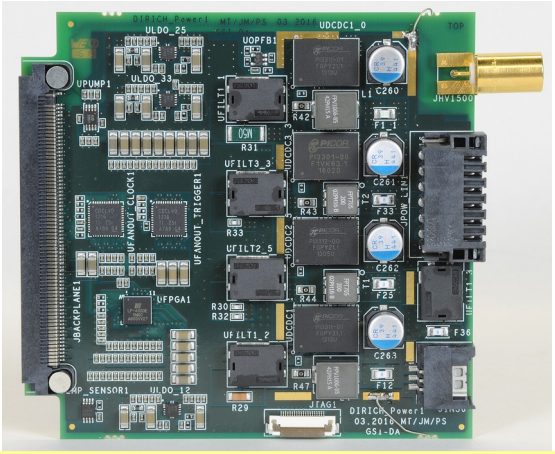
M. Traxler, C. Ugur, J. Michel, P. Skott, and many more
(TRB collab.)



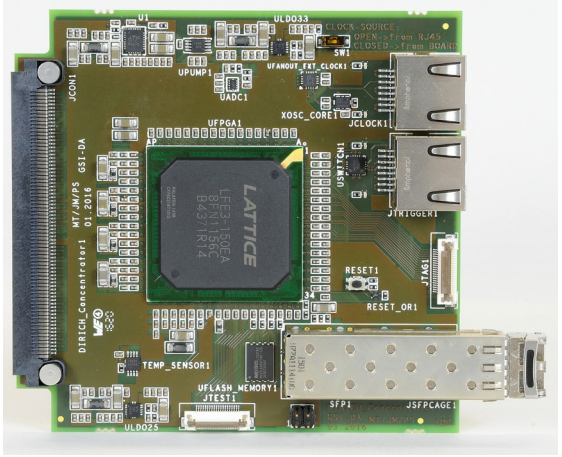
32ch DIRICH
frontend module



3x2 MAPMT backplane
(with few modules equipped)

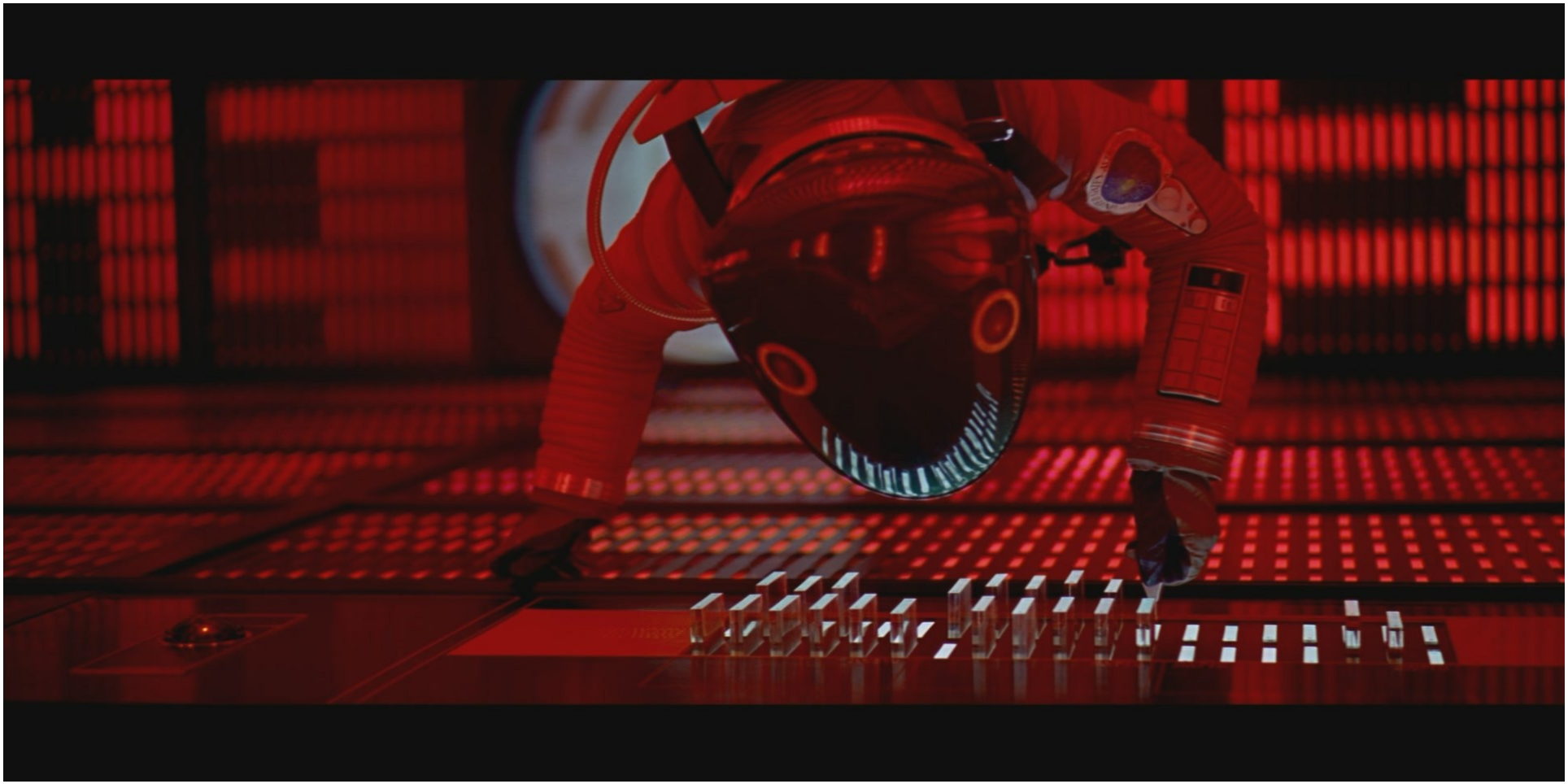


DIRICH-Power module
(LV + HV supply, DCDC)



DIRICH-Combiner module

Motivated by “HAL 9000”



Dave Bowman in “2001: A space odyssey”

The DIRICH concept

- Combine TRB3 TDC functionality and PADIWA discrimination functionality on single, FPGA-based module: **DIRICH ("Dirc Rich")**

DIRICH:
- Front-end module with 32ch per module
- Analog Discrimination using FPGA LVDS receivers (like on PADIWA)
- Leading+trailing edge measurement on FPGA-TDC (like TRB3), using same channel
- Low power consumtion (<2 W in total)
- No cable between PMT and TDC
- All connections via a single board connector

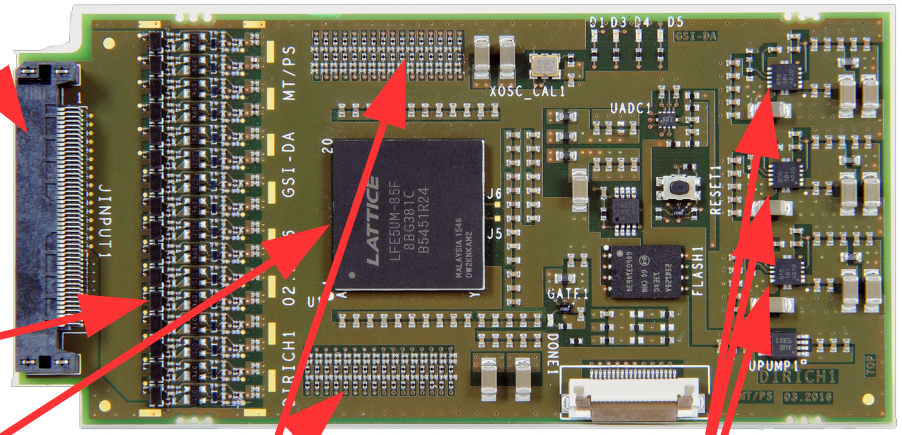
DIRICH Backplane:
- Carries 2x3 PMTs and 12 DIRICH+Power+Combiner modules for readout
- Provides all analog and digital interconnections between PMTs and DIRICH
- HV-distribution to 6 MAPMTs (common HV channel)
- Light- and gas-tight seal of radiator volume

DIRICH Combiner:
- Combine digital data of up to 12 DIRICH to single optical fiber link
- Provide common clock and trigger signals to all DIRICH boards

DIRICH Power:
- Provide all necessary LV and HV supply lines via backplane to all modules
- Possibly use DC/DC converter (thin cables)

BERGISCHE UNIVERSITÄT WUPPERTAL

DIRICH frontend module

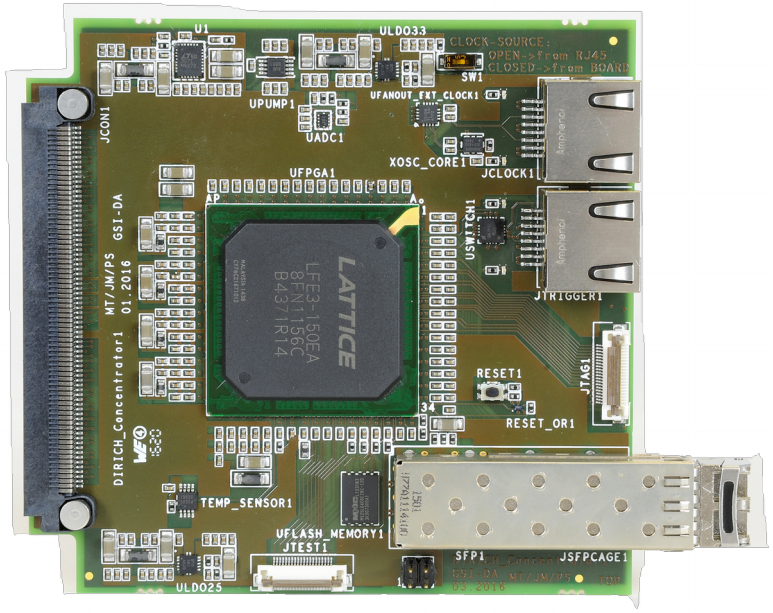


- 32ch analog amplification, discrimination, leading+trailing edge TDC, digital control all implemented on single FPGA with few discrete elements only
- **Galvanically isolated inputs** to minimize noise and ground loops
- Single-stage transistor amplifier, amplitude **gain ~30**, **high band width (4 GHz) amplifier: only 10mW per channel** (1.1V Vcc)
- Signal shaping to optimize time measurement
  Leading+Trailing edge time measurement on same channel using stretcher
- No signal integration: pure “amplitude measurement” (no charge measurement as on nXYter)
- Up to 50 MHz hit rate (burst)
- Accurate **Time-Over-Threshold measurement** (for amplitude, walk corr.)
- ADC measurement of LV supply for feedback

BERGISCHE UNIVERSITÄT WUPPERTAL

DIRICH combiner module

Lattice ECP3 FPGA
Same as on TRB3



Separate inputs for
- common system clock
- Trigger / Sync signal
Distribution via backplane

Digital data- and control lines
To each DiRICH via backplane
Power via backplane

2.4 Gbit data link via SFP

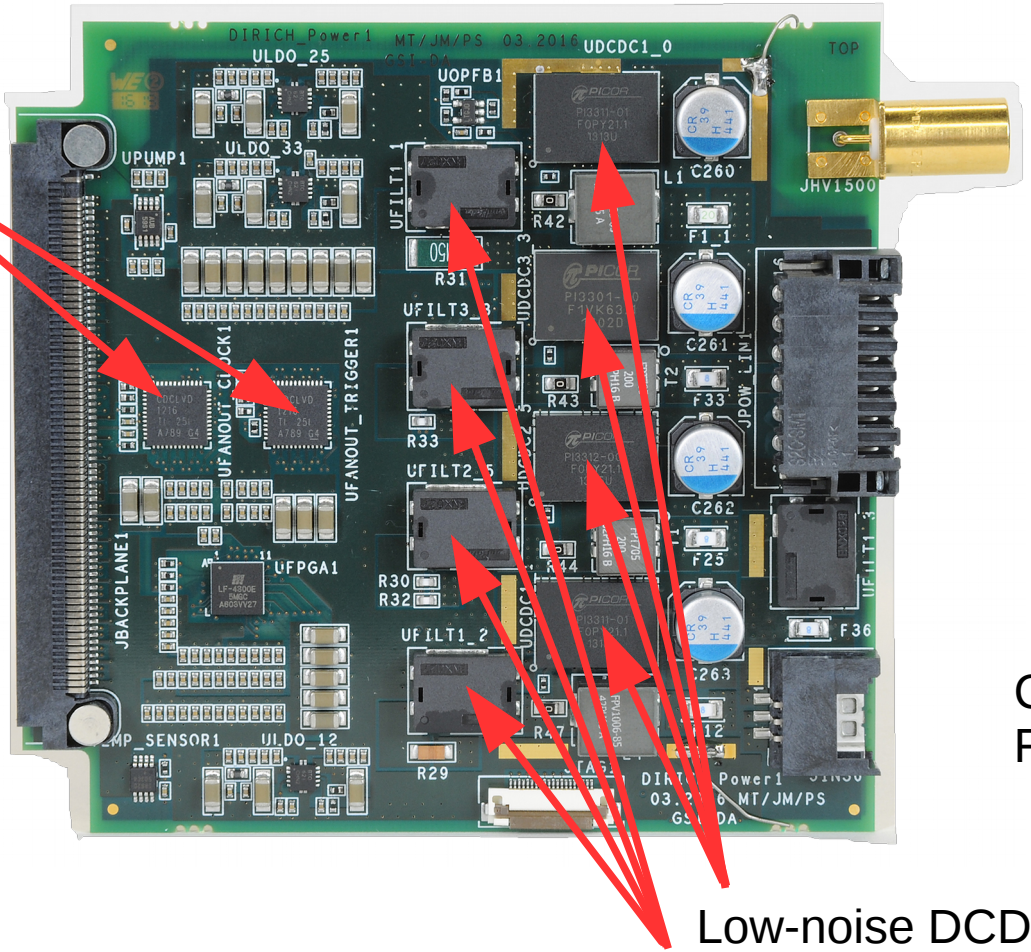
- Combines data from up to 12 DIRICH modules, (2 Gbit/s SERDES each)
- Single 2.4 Gbit/s SFP output link
- TRBnet protocol for data and control
- Slow-control, can switch/reboot individual DIRICH modules

- Later, upgraded version with 2x 5 Gbit/s link possible

BERGISCHE UNIVERSITÄT WUPPERTAL

DIRICH Power Module

LVDS fanout
For distribution of
Clock and
trigger/sync



HV connection
Common for all 6 PMTs
via backplane

External LV supply
1.1V / 1.2V / 2.5V / 3.3V
If no DCDC to be used

or

Common 30V DC supply
For DCDC convertes

Low-noise DCDC converter
with extensive filtering

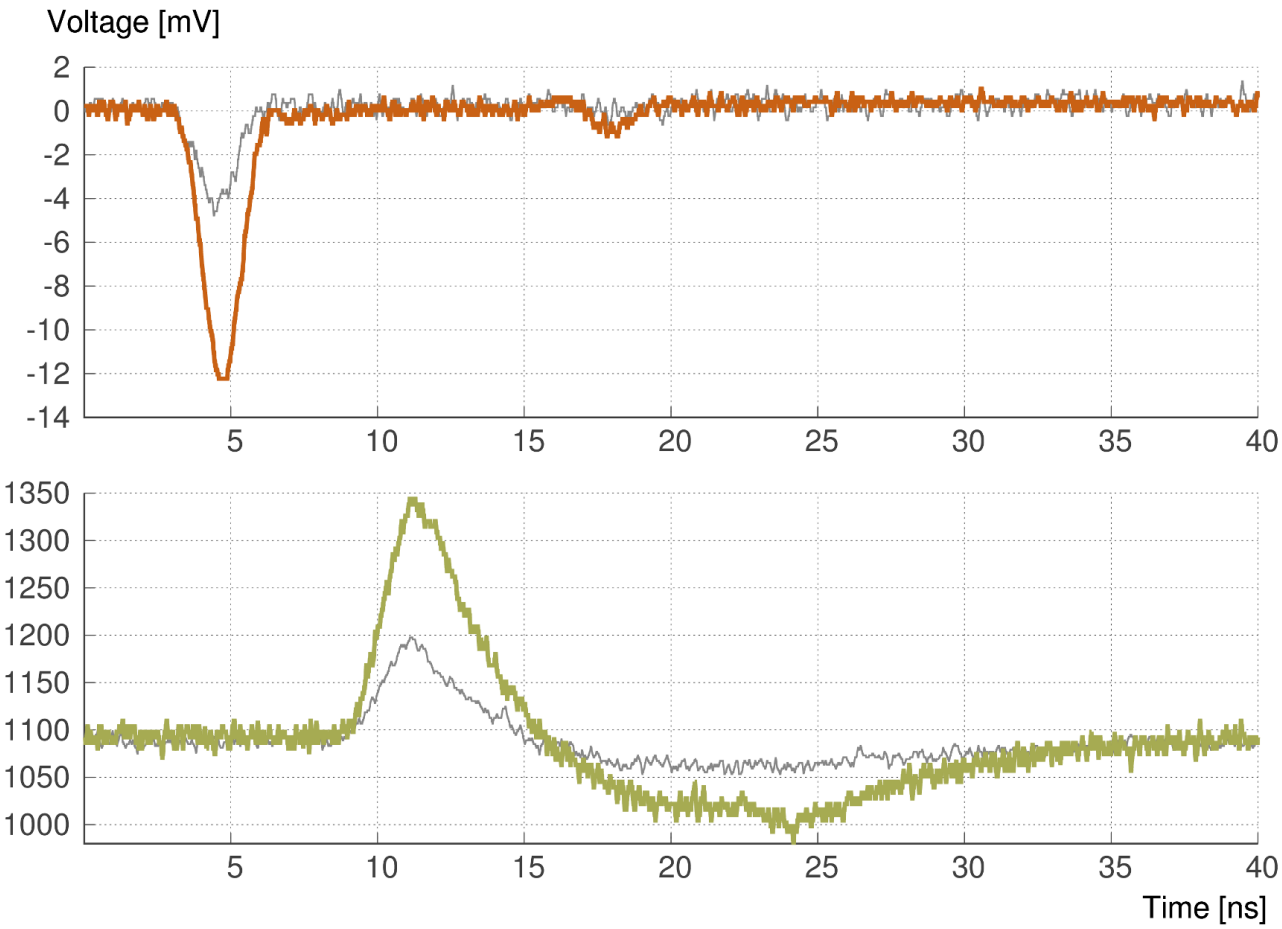
- Usage of DCDC converters optional
- Can also be powered externally (reduce noise, but requires thick cables, ~11A on 1.1V)
- Current monitoring

Preamplifier shaping

Typical PMTlike input signal (from pulse generator 4 mV / 12 mV)
and corresponding output from preamp, directly before entering the FPGA

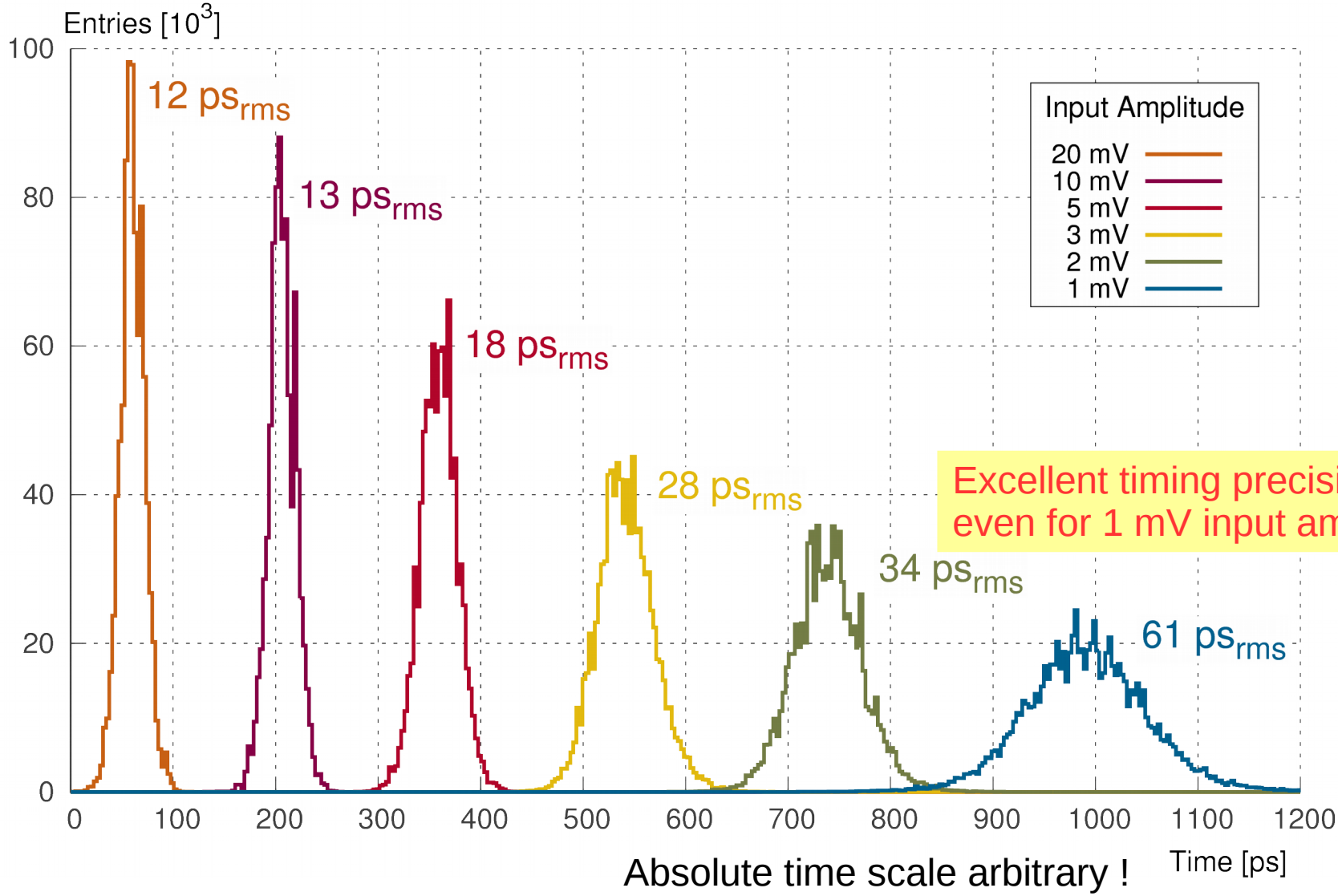
PMT-like
Input pulse

Preamp Output
before FPGA



DIRICH timing precision in the lab measured with pulser

Time difference between two channels receiving the same input signal



Excellent timing precision
even for 1 mV input amplitude !

Absolute time scale arbitrary !

BERGISCHE UNIVERSITÄT WUPPERTAL

DIRICH data rate considerations

- Present TRBnet data format:
  12 byte per hit: 4 byte leading-, 4 byte trailing edge, 4 byte overhead

- FPGA-TDC: <50 MHz hitrate /channel (short burst)

- **DIRICH** data link: 2 Gbit/s, max 150 MByte/s:
  → 150 MB/s = 12.5 MHit/s = **390 kHit/s/channel**

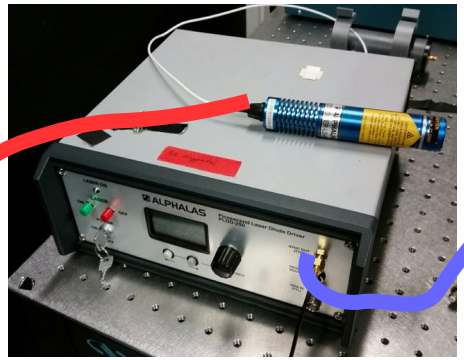
- **Present Combiner**: single 2.4 Gbit/s SFP, max 180 MByte/s
  → 180 MB/s = 15 MHits/s = **39 kHit/s/channel** (6x64 ch)

If higher rate is needed:

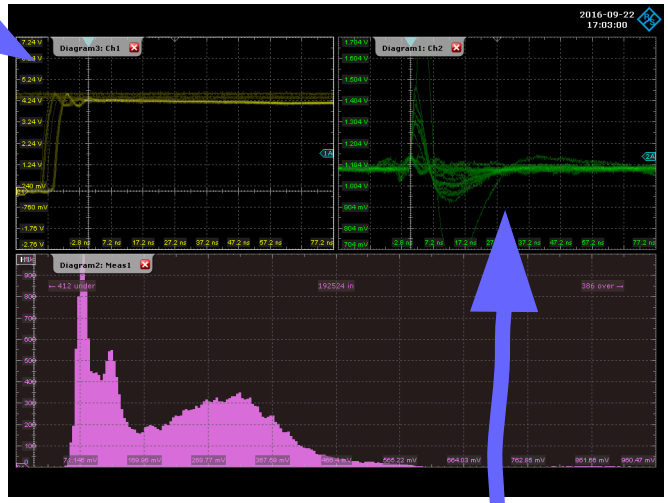
- Modification / sparsification of data format: eg leading edge+ToT
- New Combiner module with 1 or 2 4.8 Gbit/s links

BERGISCHE UNIVERSITÄT WUPPERTAL

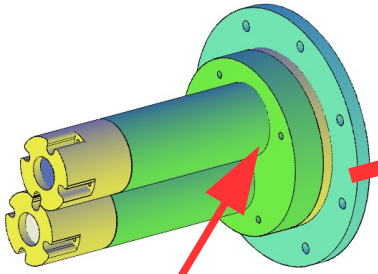
Single photon test setup at HADES cave



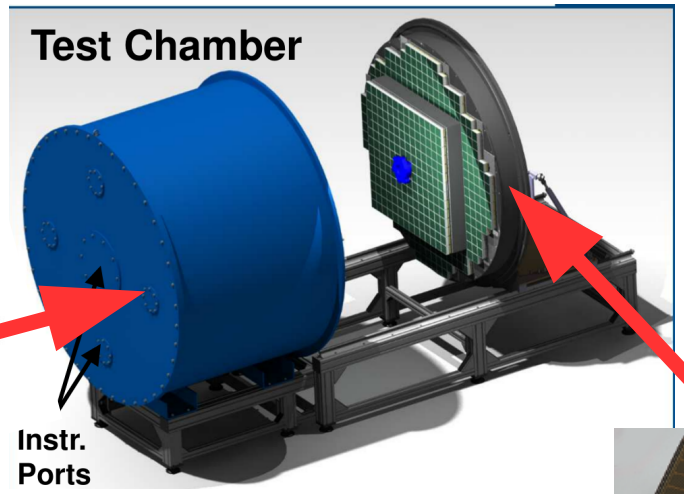
<40ps Laser pulser

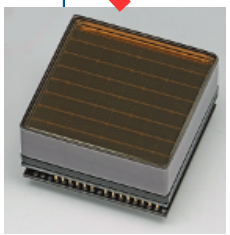


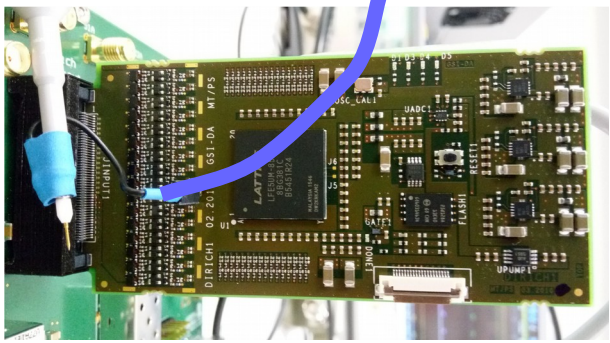
4 GHz scope,
offline trace analysis

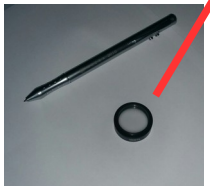


Second port
For LED (DC)
(background generation)

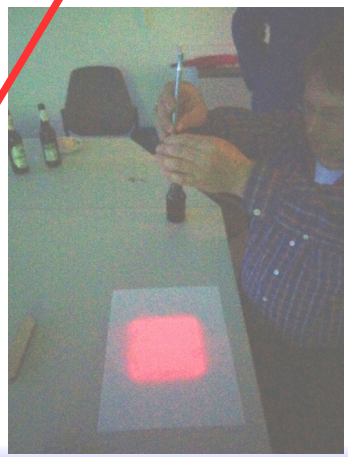








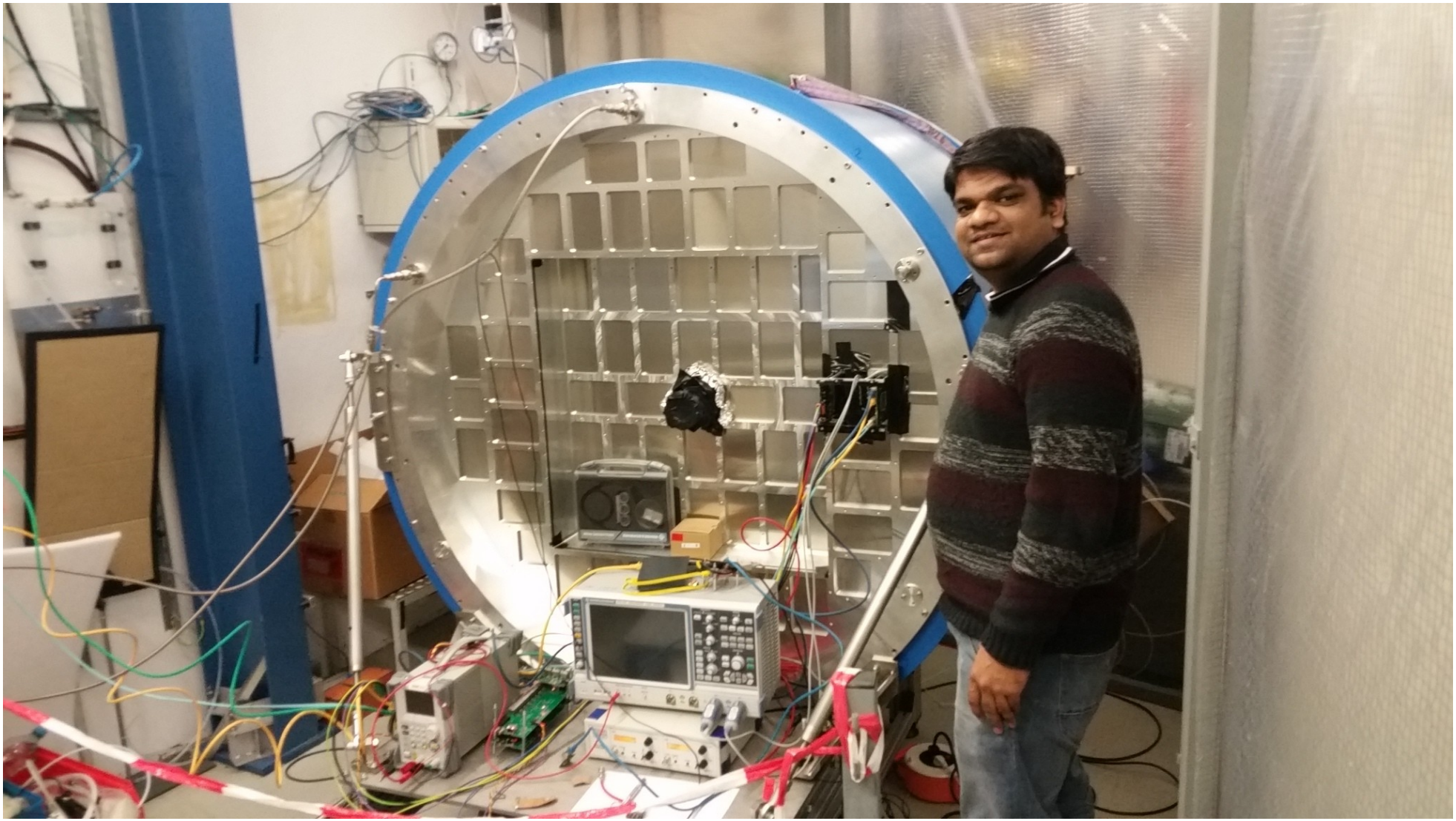
ThorLabs
square diffosor



Single PMT with 2x DIRICH
Scope with active probes (0.8 pF)
connected to DiRICH preamp output
(two single pixels)

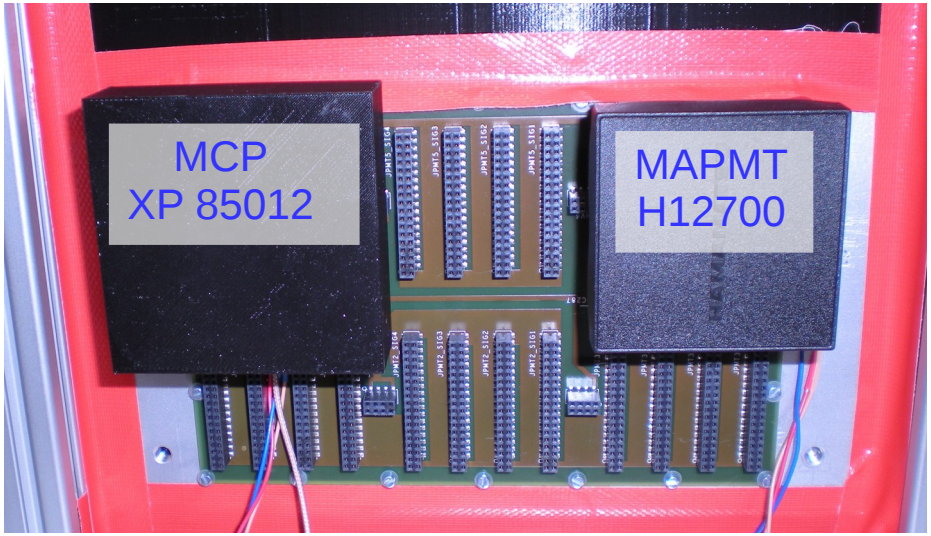
BERGISCHE UNIVERSITÄT WUPPERTAL

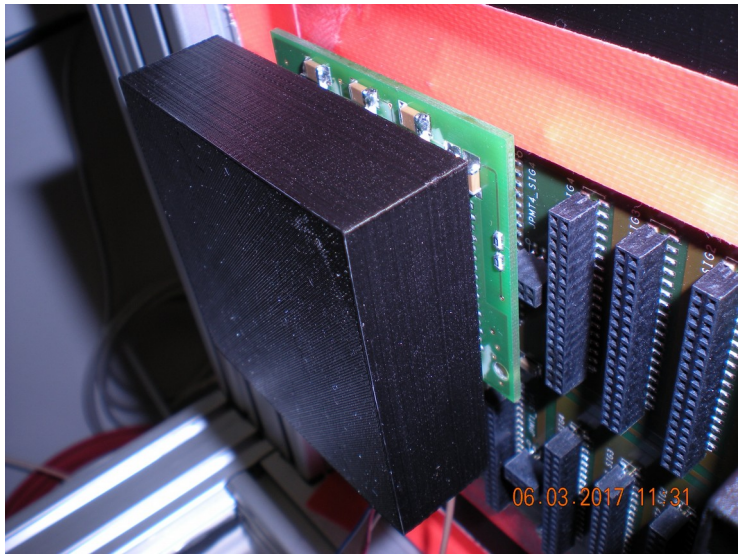
Two weeks ago in the HADES cave...



MCP → PMT adapter with Voltage Divider

- MCPs and MAPMTs have slightly different pinning and connector positions (and size)
- Adapter allows to put MCPs on “standard” 3x2 backplane for first tests
- Adapter includes passive Voltage Divider
- HV supply via backplane possible, but not recommended (“tested” up to 1900V)





BERGISCHE UNIVERSITÄT WUPPERTAL

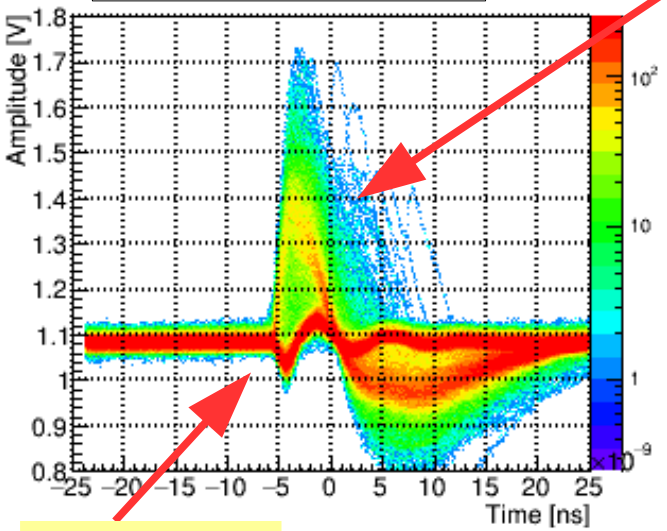
Scope trace analysis: PMT signal after preamp

- Laser pulser: a single photon in 10% of pulses, no photon/pixel in 90%
- Active probes mounted to DIRICH, measuring preamp output signal
- Digital scope to store individual traces, up to 100 acquisitions/sec
- Trigger on laser sync signal
- Offline analysis of scope data → persistency, leading / trailing edge, ToT, ampitude...

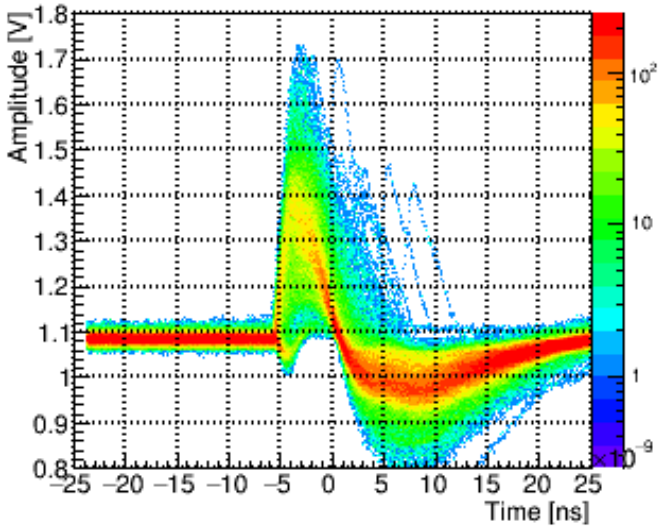
All traces

Single photons

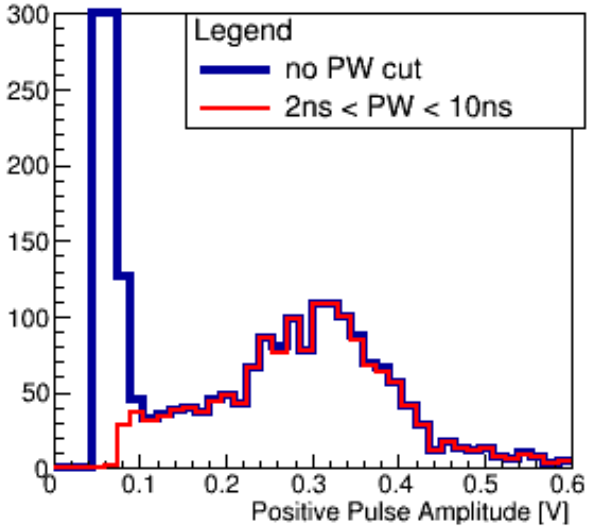
Capacitive Cross talk



Cut on ToT > 2ns



Amplitude spectrum



BERGISCHE UNIVERSITÄT WUPPERTAL

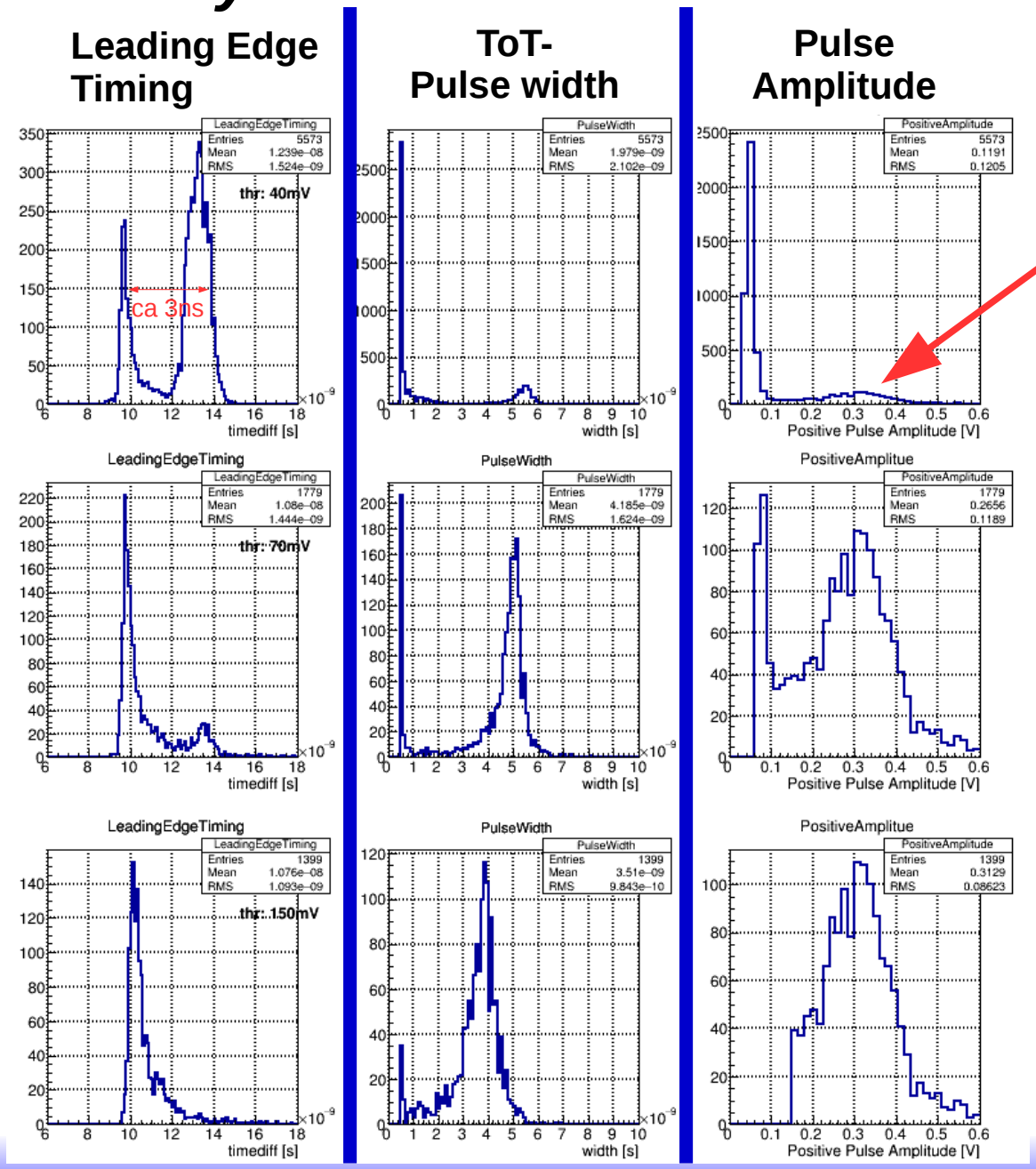
Time, ToT, amplitude from scope analysis – no TDC yet !

Threshold:

40 mV

70 mV

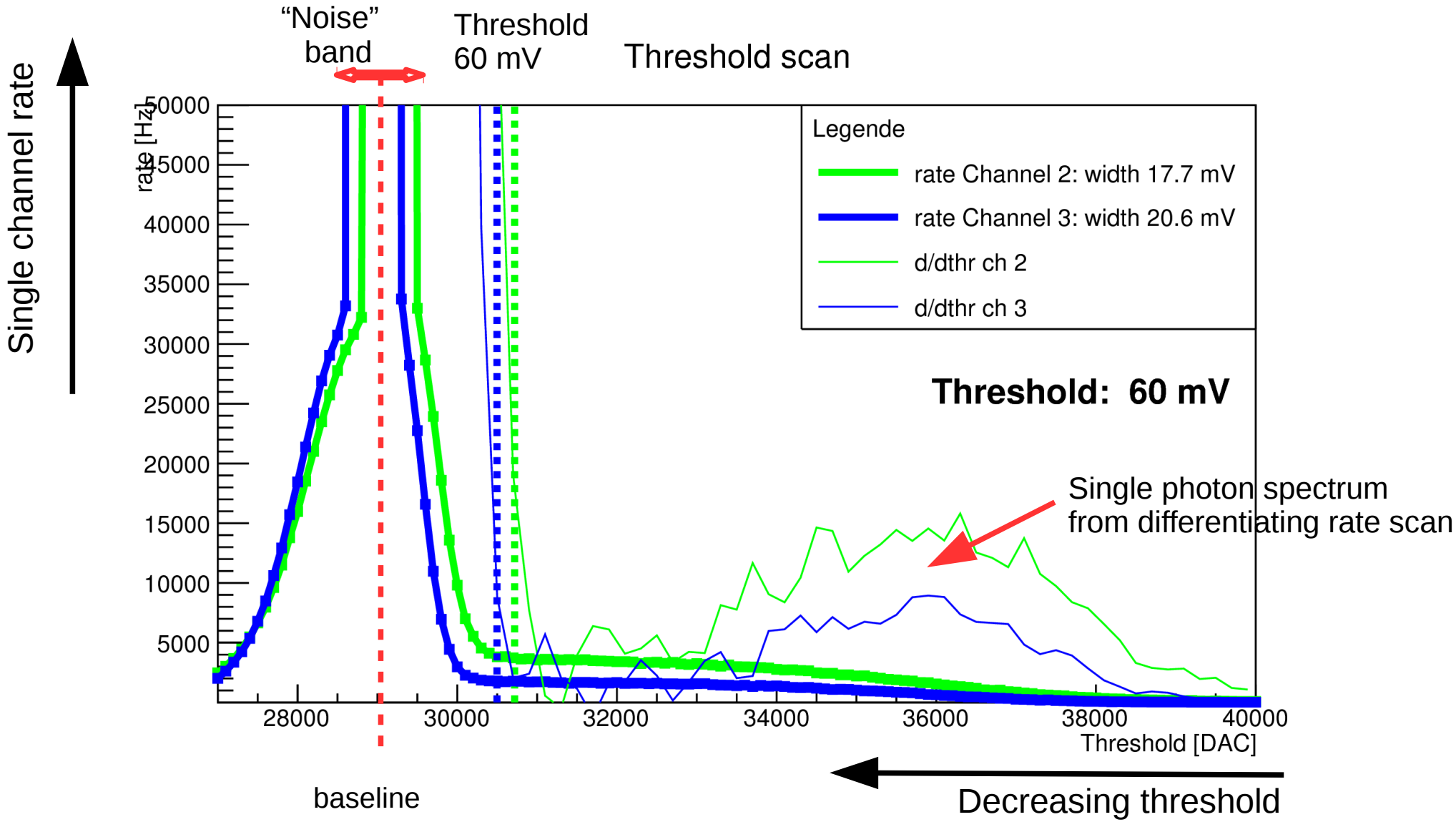
150 mV



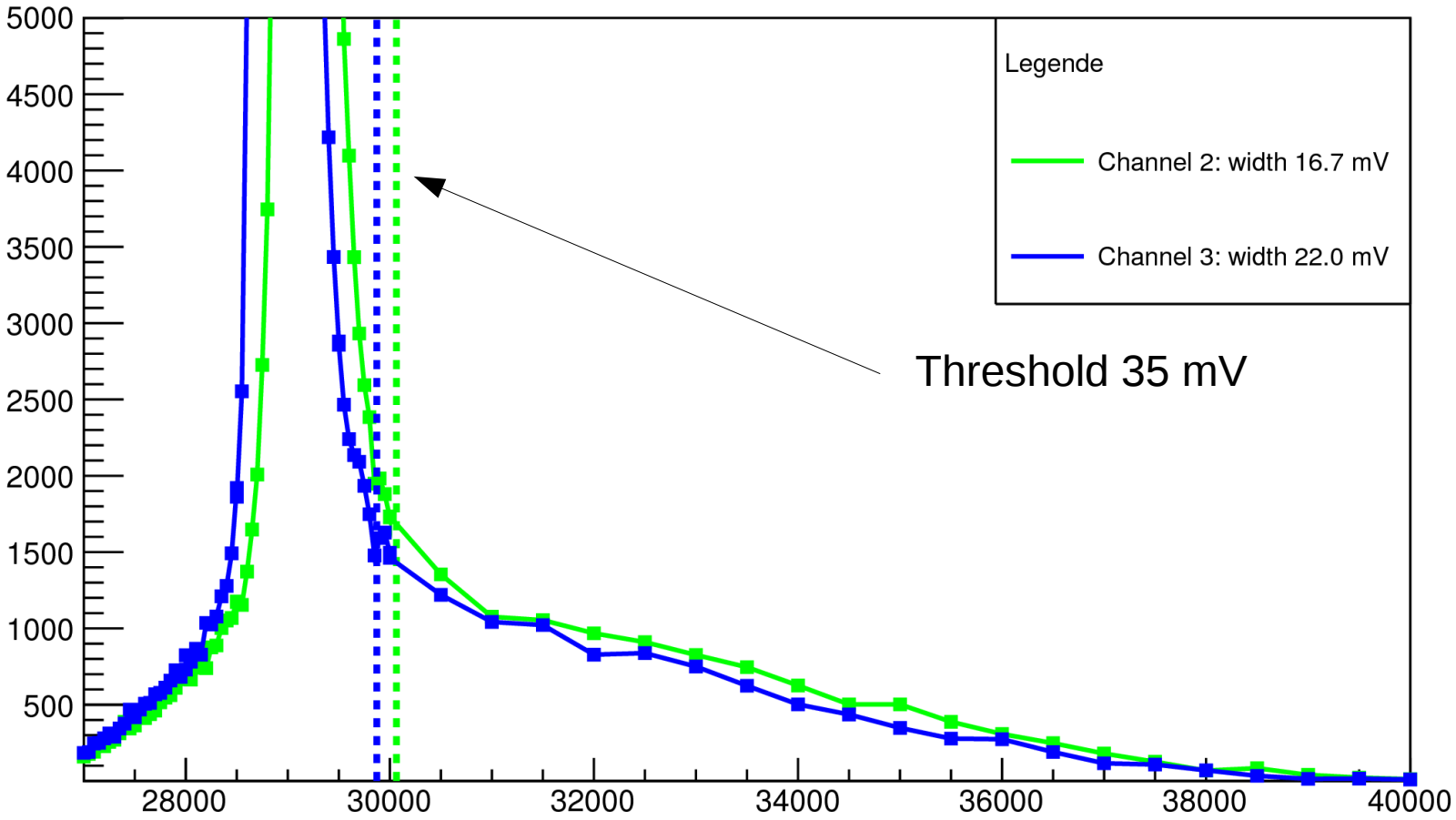
Single photon signal

BERGISCHE UNIVERSITÄT WUPPERTAL

Using FPGA-TDC / scalers: DIRICH threshold scan MAPMT



DIRICH threshold scan MCP



Very first scan for MCP

- Reasonable behavior
- Higher dark rate than PMT (1 kHz per channel)

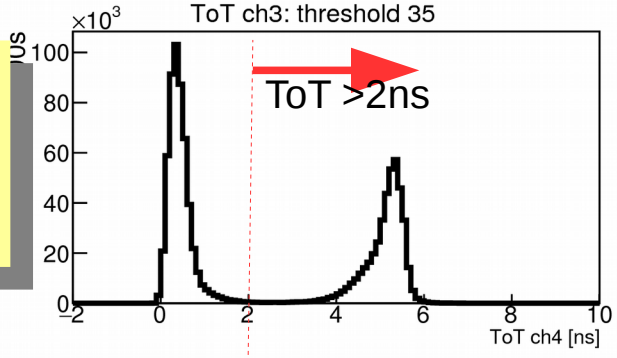
BERGISCHE UNIVERSITÄT WUPPERTAL

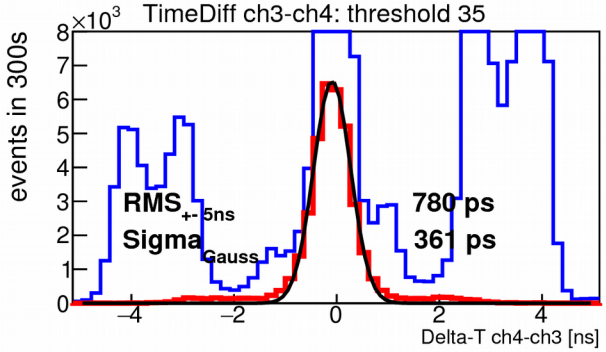
First FPGA-TDC measurements: MAPMT

Time-over-Threshold

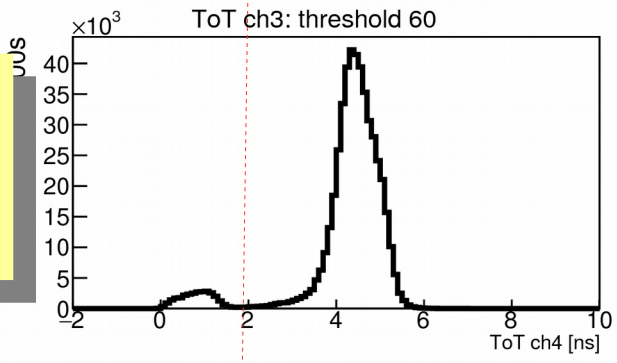
Time-diff ch1-ch2

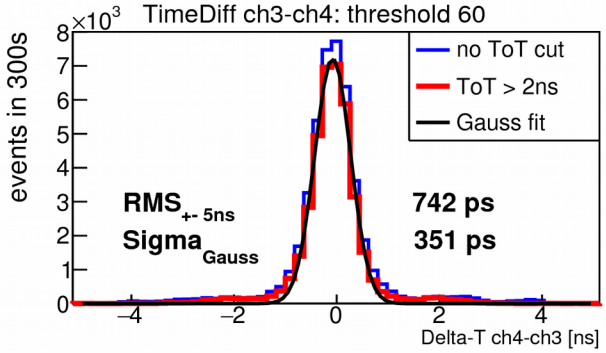
35 mV



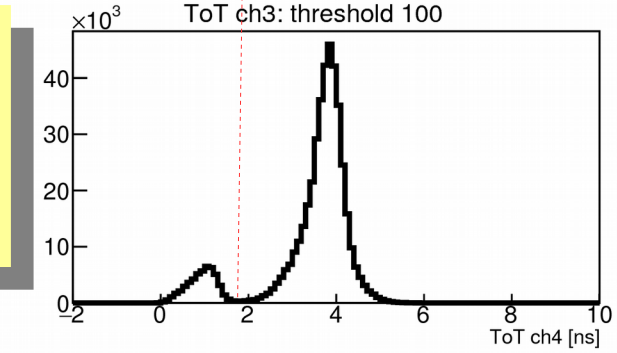


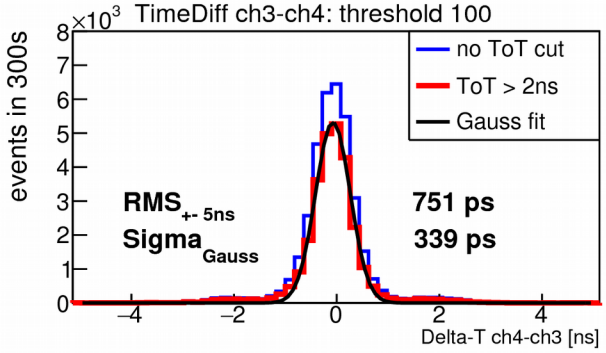
60 mV





100 mV





- ToT spectrum: two distinct peaks:
  - real photons at ToT > 2 ns
  - cross talk “wiggle” at low ToT
- 35 mV: wiggle signal picked up
  → well suppressed by ToT cut
- ToT degrades for higher thresholds

Timing precision full system:

from delta-T between 2 channels:

750 ps RMS
350 ps Gaussfit

PMT Transit Time Spread: **290 ps**

expected delta-T width:
√2 * 290 ps = 410ps

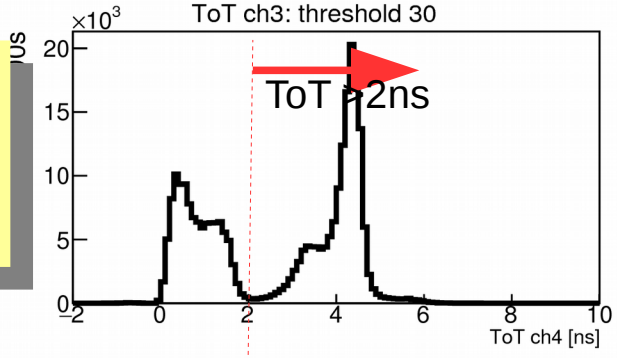
BERGISCHE UNIVERSITÄT WUPPERTAL

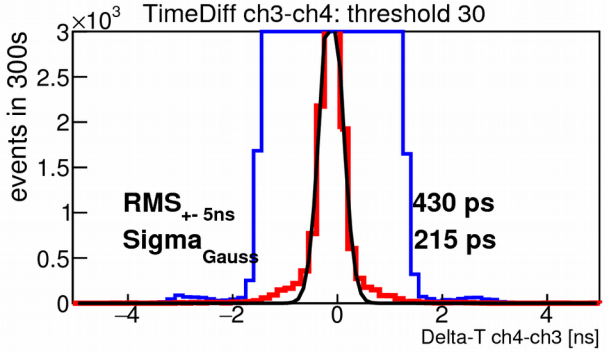
First FPGA-TDC measurements: MCP

Time-over-Threshold

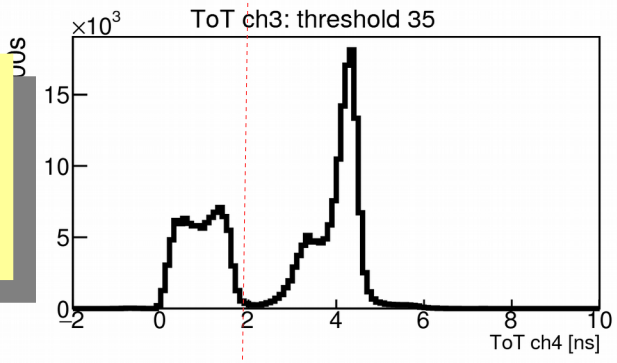
Time-diff ch1-ch2

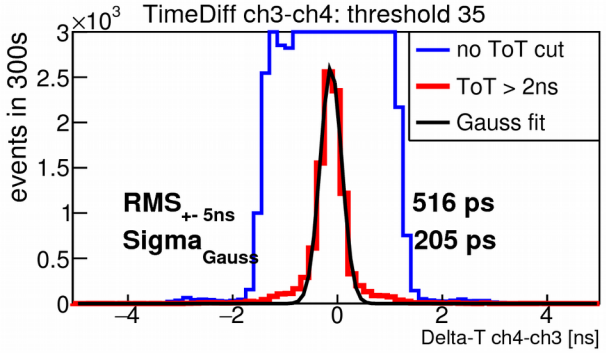
30 mV



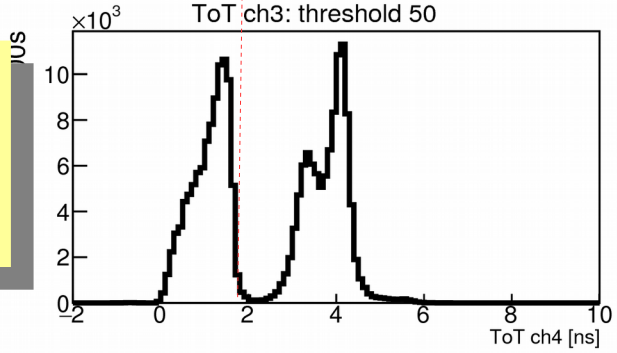


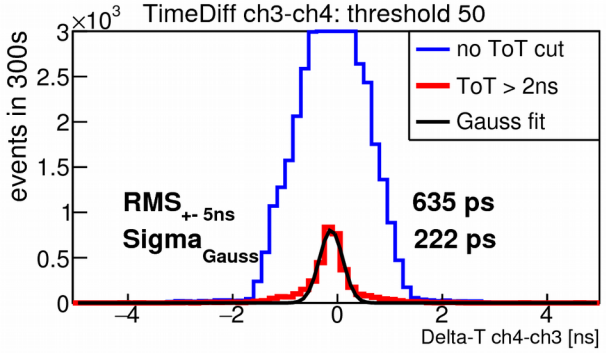
35 mV





50 mV





- XP85012 MCP at 1900V
- MCP signal has lower amplitude
  → need low threshold !

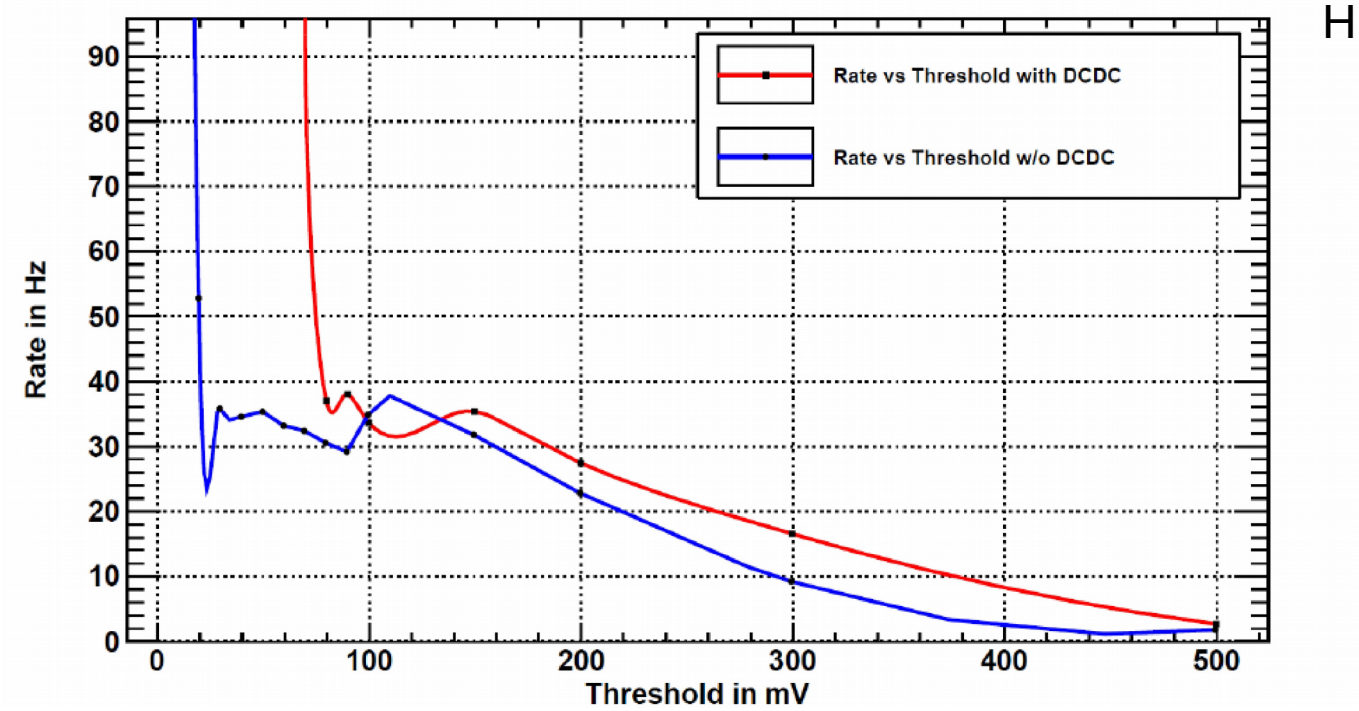
Timing precision full system:

from delta-T between 2 channels:

500 ps RMS

220 ps Gaussfit

Additional noise from DCDC converters



Hit rate vs noise using
- external power supplies
- onboard DCDC converters

- At present, the onboard DCDC converters on the Power module cause significant additional noise.
- Copper shielding already foreseen, and will be tested soon.

BERGISCHE UNIVERSITÄT WUPPERTAL

Summary and outlook

- New DIRICH readout chain has been developed,
  based on combination of PADIWA + TRB3 on single, compact board

- **Prototypes of all modules are available** and under test (test stand HADES, lab)

- Only minor design bugs discovered on DIRICH so far (split ground plain, PWM, …)
  DIRICH ver 2 is under production now

- Urgent need for manpower in the TDC development
  → At present, only TDC with 4 working channels available ! (but 32ch feasible !)

- "scope analysis" allows to predict precisely what to expect from TDC measurement
  → important tool for debugging analog part !

- **Very promising results for MAPMTs so far**
  → Timing precision limited by sensor itself, low noise figure, …
  → Efficiency to be studied in detail

- Very first test of MCPs promising as well, but needs further work and maybe tuning
  → lower amplitude, higher noise, different cross talk behavior
  → MCP adapter board allows to test MCP without need do build new backplane !

- **Test beam at COSY** planed for Mai/June 2017
  → Evaluate performance under realistic beam conditions

- **Start of mass production for HADES end of this year**

BERGISCHE UNIVERSITÄT WUPPERTAL

How much does it cost ?

Assuming a detector with **15k channels (30k channels), 240 MAPMTs (480 MAPMTs):**

480x DIRICH, 40x Power, Concentrator, backplane (960x DIRICH, 80x Power, Concentrator, backplane)

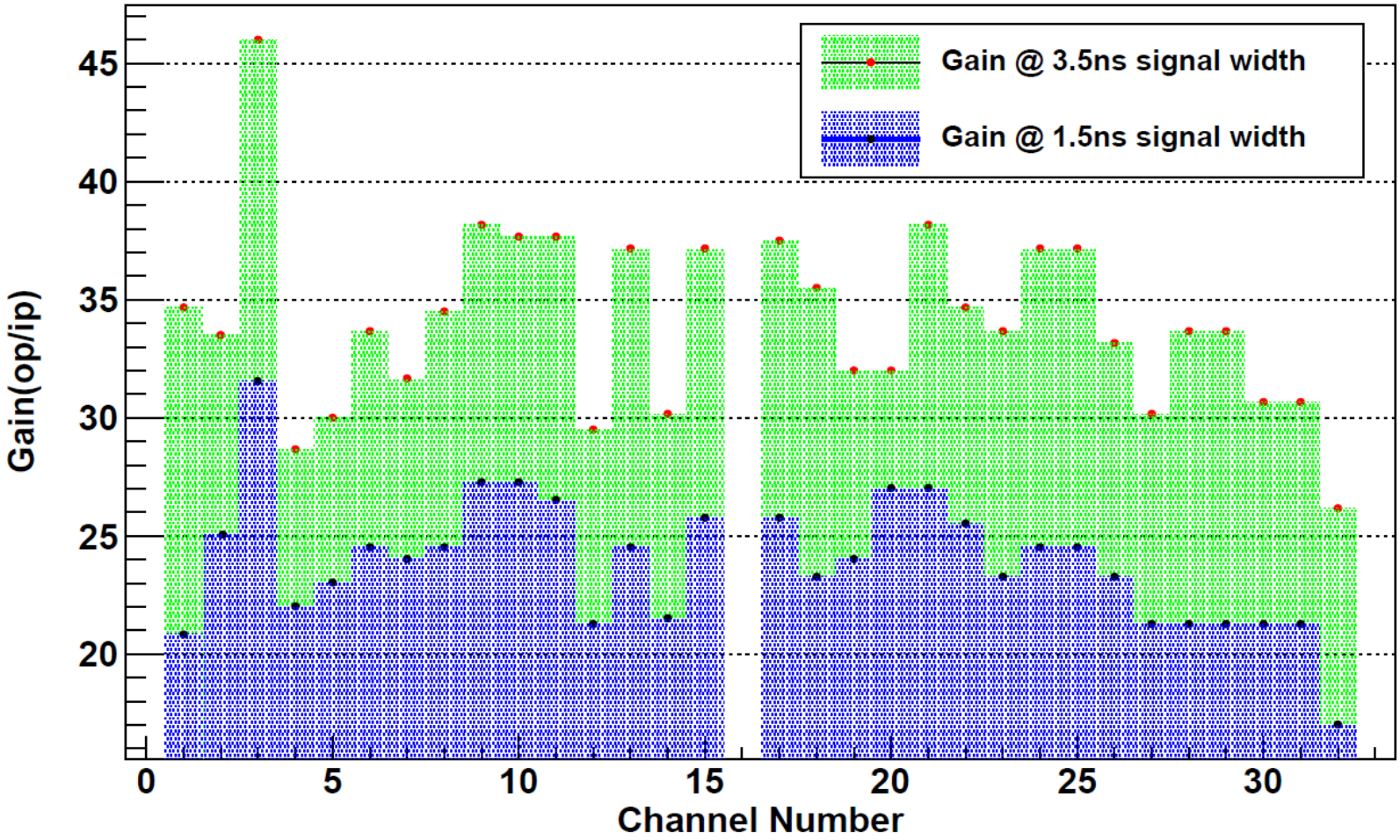
All prices **excluding VAT, only components, no setup costs, no production costs, 2017 !**
Significantly higher costs for smaller quantities !

			Single module	Full detector
DIRICH:			**140,- € (120,- €)**	**68k€ (116 k€)**
– PCB	33,- €	(17,- €)		
– FPGAs	41,- €	(41,- €)		
DIRICH Concentrator:			**300,- € (250,- €)**	**12k€ (20 k€)**
– PCB	75,- €	(29,- €)		
– FPGA	168,- €	(168,- €)		
DIRICH Power:			**230,- € (180,- €)**	**10k€ (15 k€)**
– PCB	80,- €	(35,- €)		
– DCDC	45,- €	(45,- €)		
– Filter	30,- €	(30,- €)		
Backplane			**330,- € (230,- €)**	**14k€ (19 k€)**
– PCB	185,- €	(100,- €)		
– Conctr.	135,- €	(120,- €)		
Total	**15k (30k) channels**			**104 k€ (170 k€)**

Backup slides

BERGISCHE UNIVERSITÄT WUPPERTAL

Gain per channel comparison of DiRICH preamp



- Lab measurement with pulse generator
- Typical PMT signal: ~3ns
- Gain seems to slightly decrease for very short signals

Vivek Patel, BUW

BERGISCHE UNIVERSITÄT WUPPERTAL

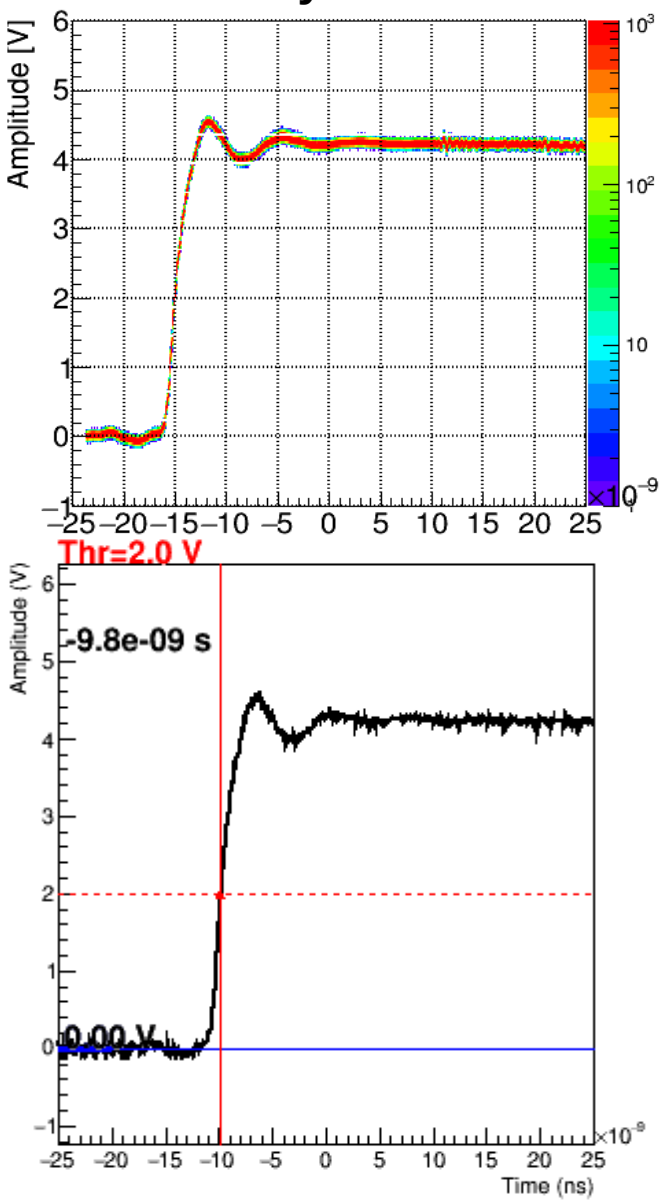
The HADES RICH Test stand

Triggered on SYNC only
No trigger on PMT signal
10k acquisitions

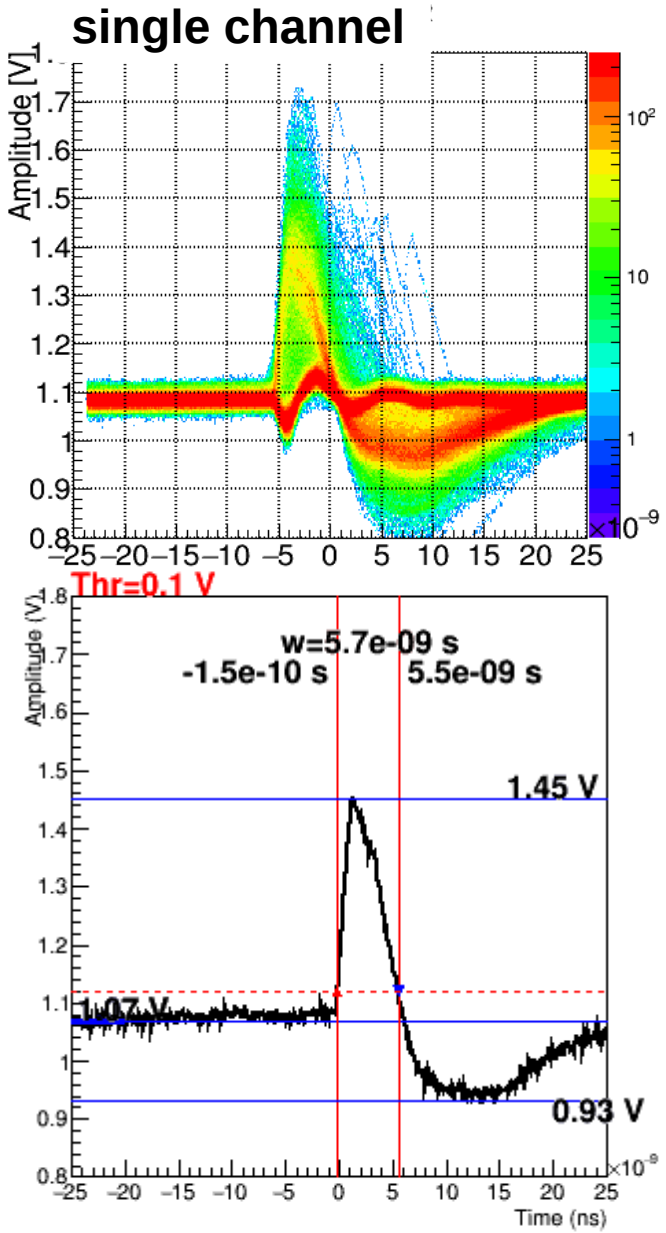
10 kHz Laser pulse freq.
~ 0.1 photon /pulse/pixel

Full offline trace analysis:
- leading / trailing edge time
- Pulse amplitude
- Pulse area
- Pulse width
- ...

Pulser Sync

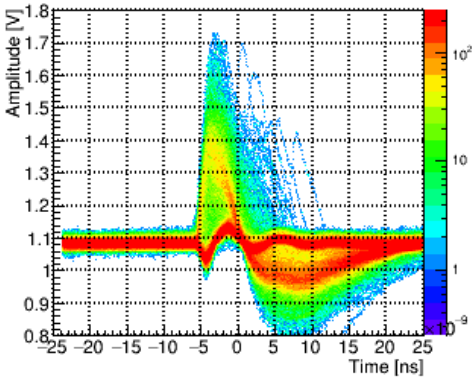
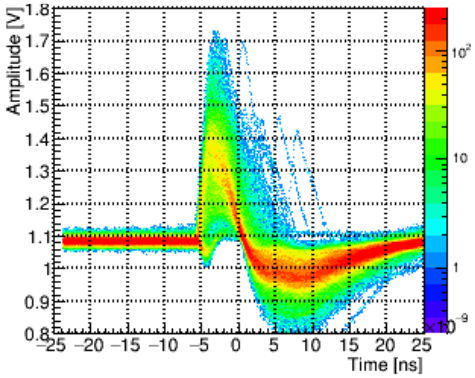
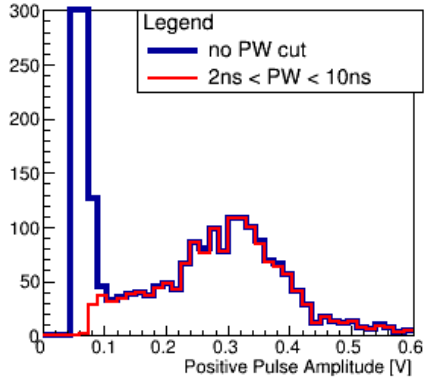
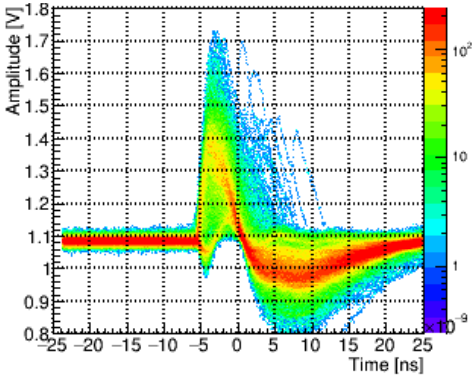
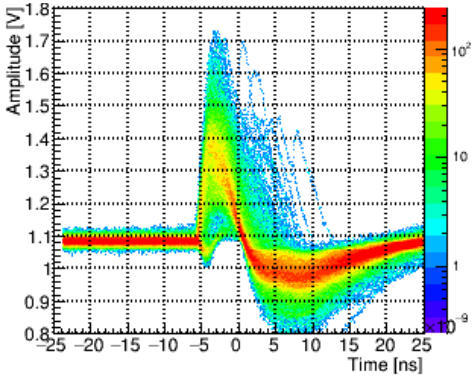
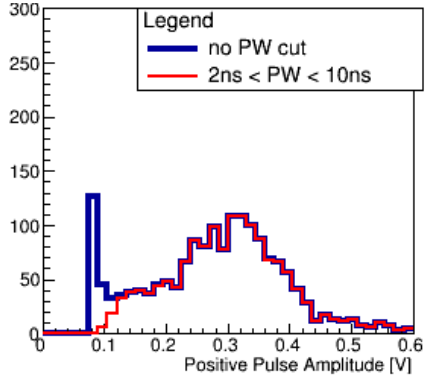
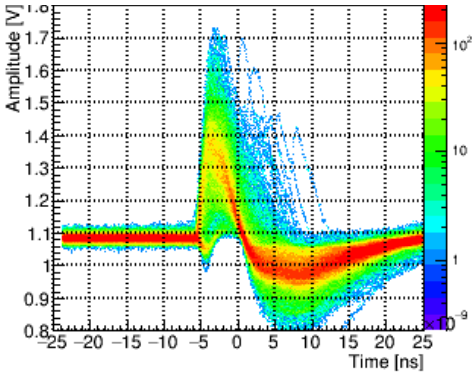
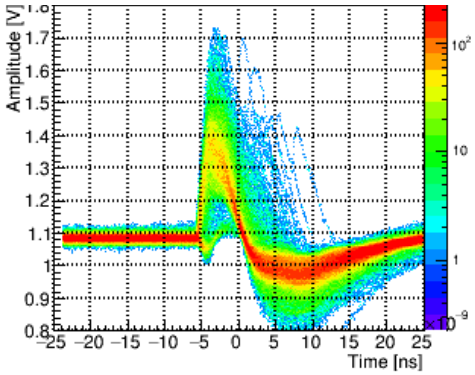
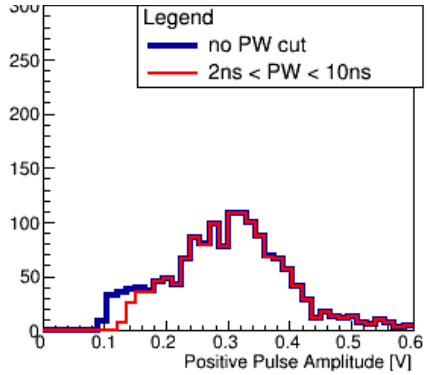


PMT single channel



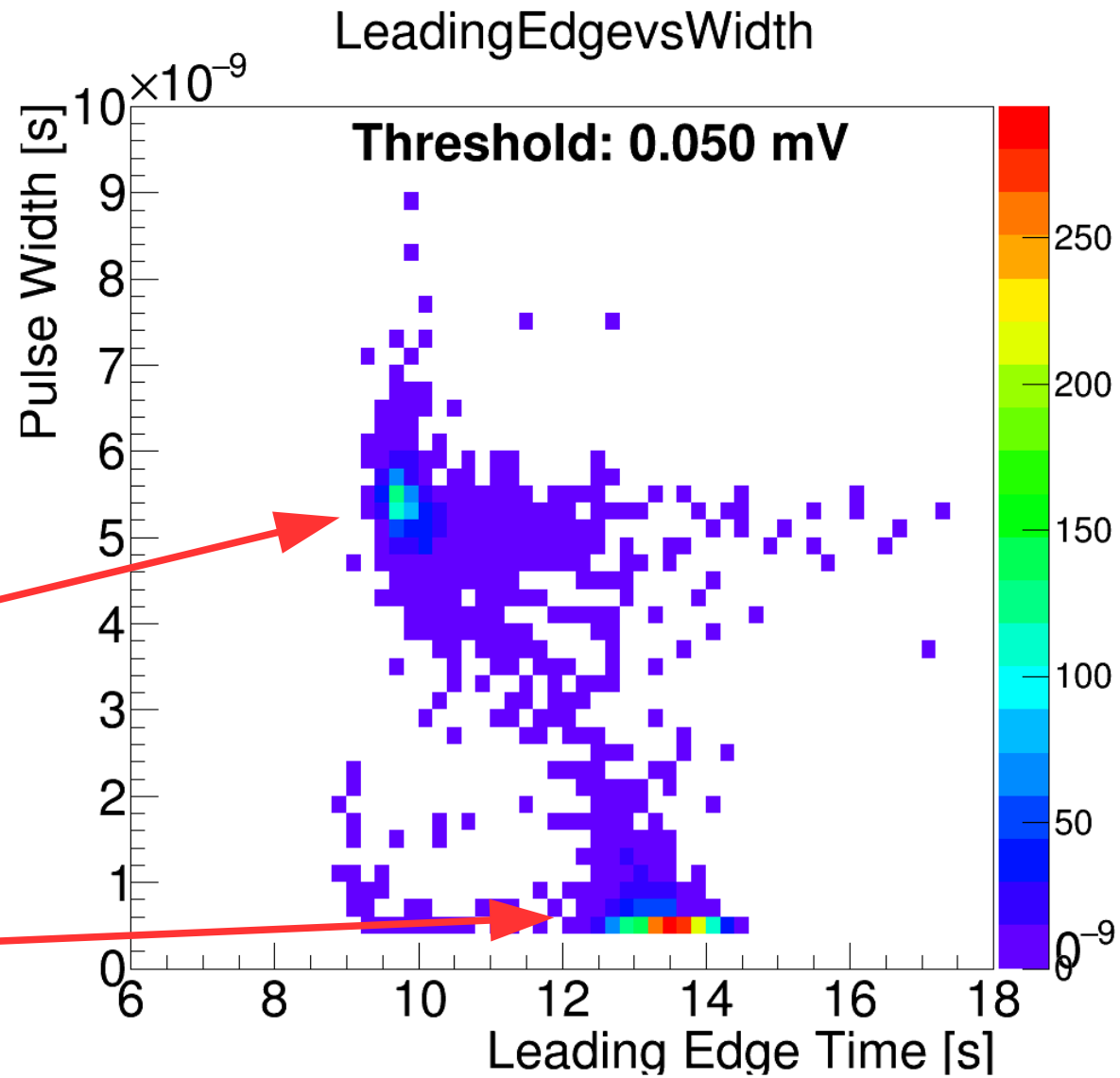
BERGISCHE UNIVERSITÄT WUPPERTAL

Effect of cut on PulseWidth

Signal threshold:	Cut on threshold only	Additional cut on PulseWidth: 2ns < PW < 10ns	Amplitude spectrum w / wo cut
50 mV			
75 mV			
100 mV			

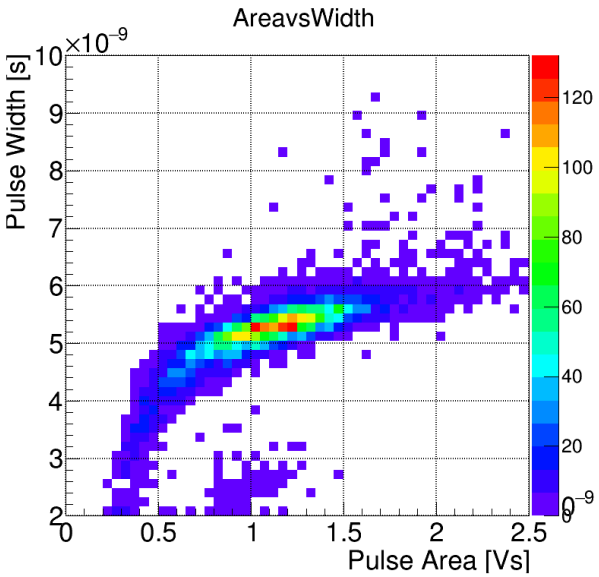
BERGISCHE UNIVERSITÄT WUPPERTAL

Leading Edge vs PulseWidth - possible walk effect ?

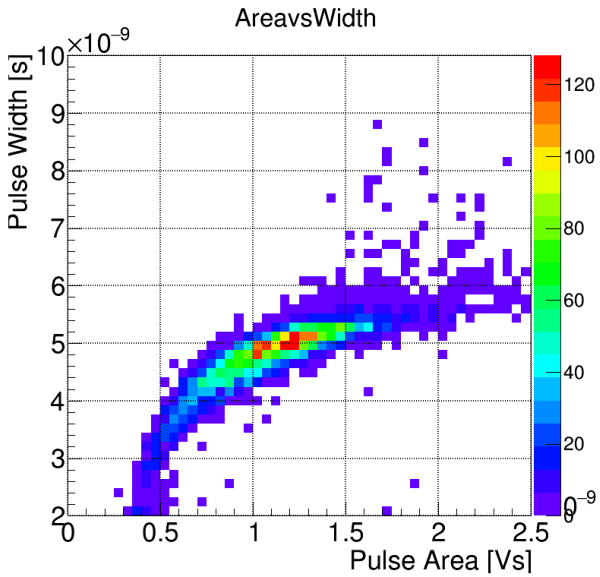


Amplitude - PulseWidth correlation

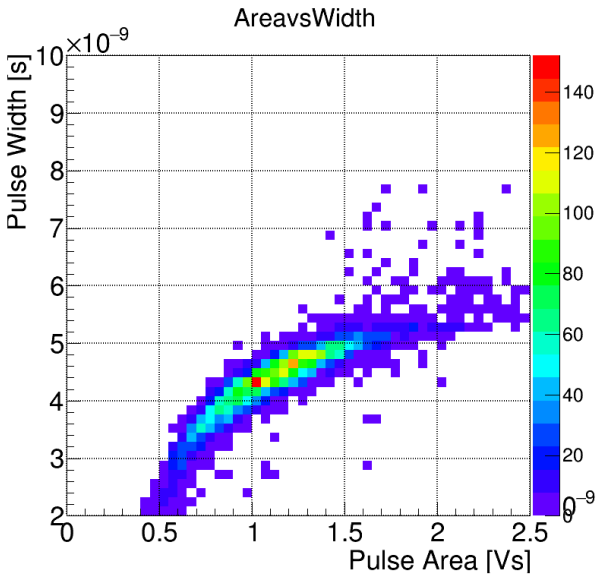
50mV Threshold



75mV Threshold



100mV Threshold



Correlation between PulseArea and PulseWidth

For 3 different thresholds.

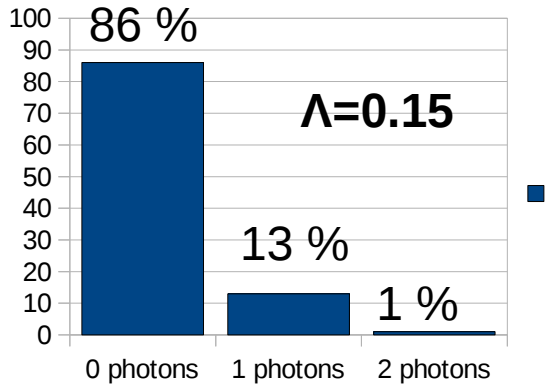
Photon efficiency

Acquisition trigger on SYNC only
→ **unbiased sample**

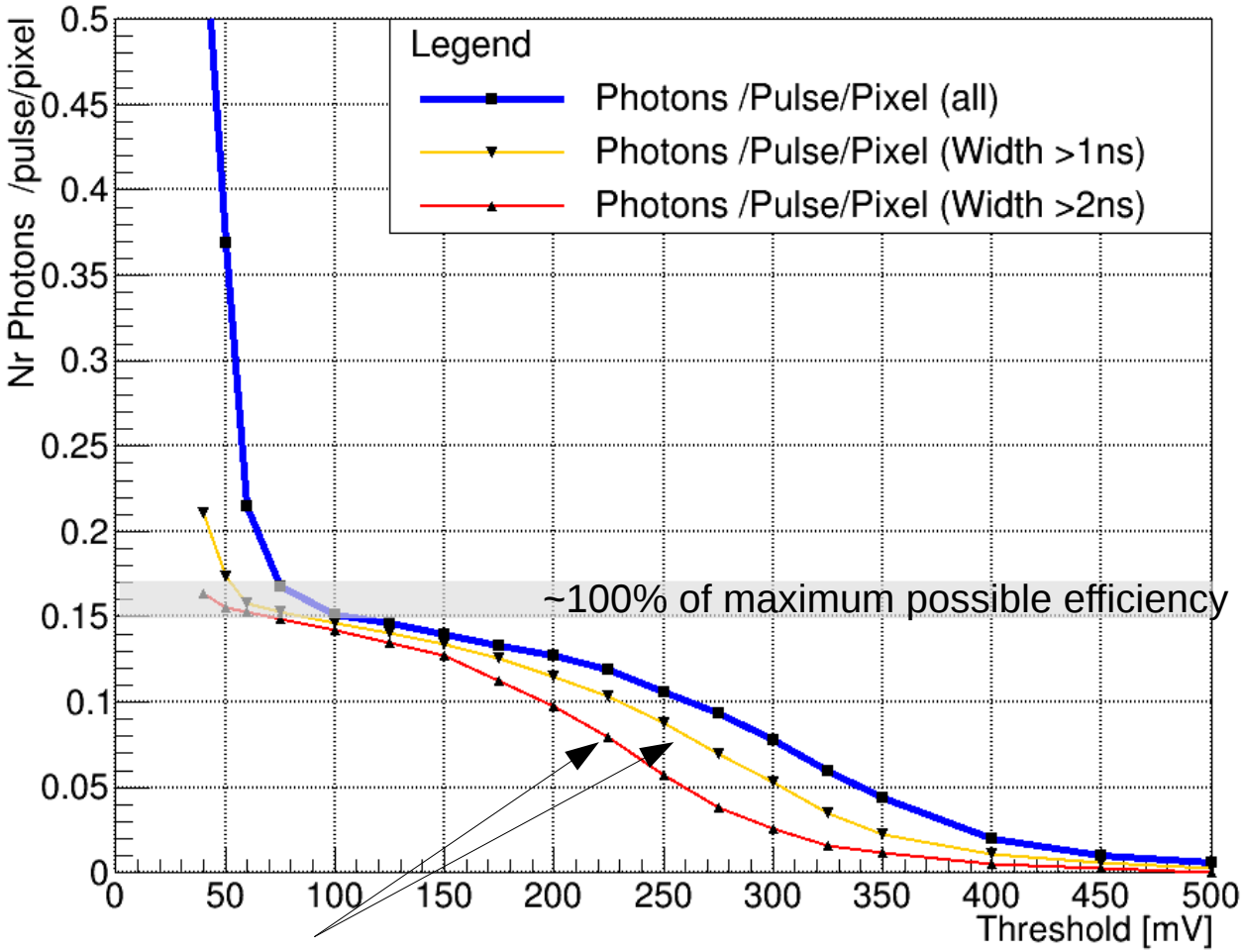
count # photon pulses above thresh
In 10k acquisitions
as function of signal threshold

Result:
Nr detected photons /pulse/pixel

Poisson Distribution



SignalFraction



additional cut on Pulse Width
(>1ns / >2ns)

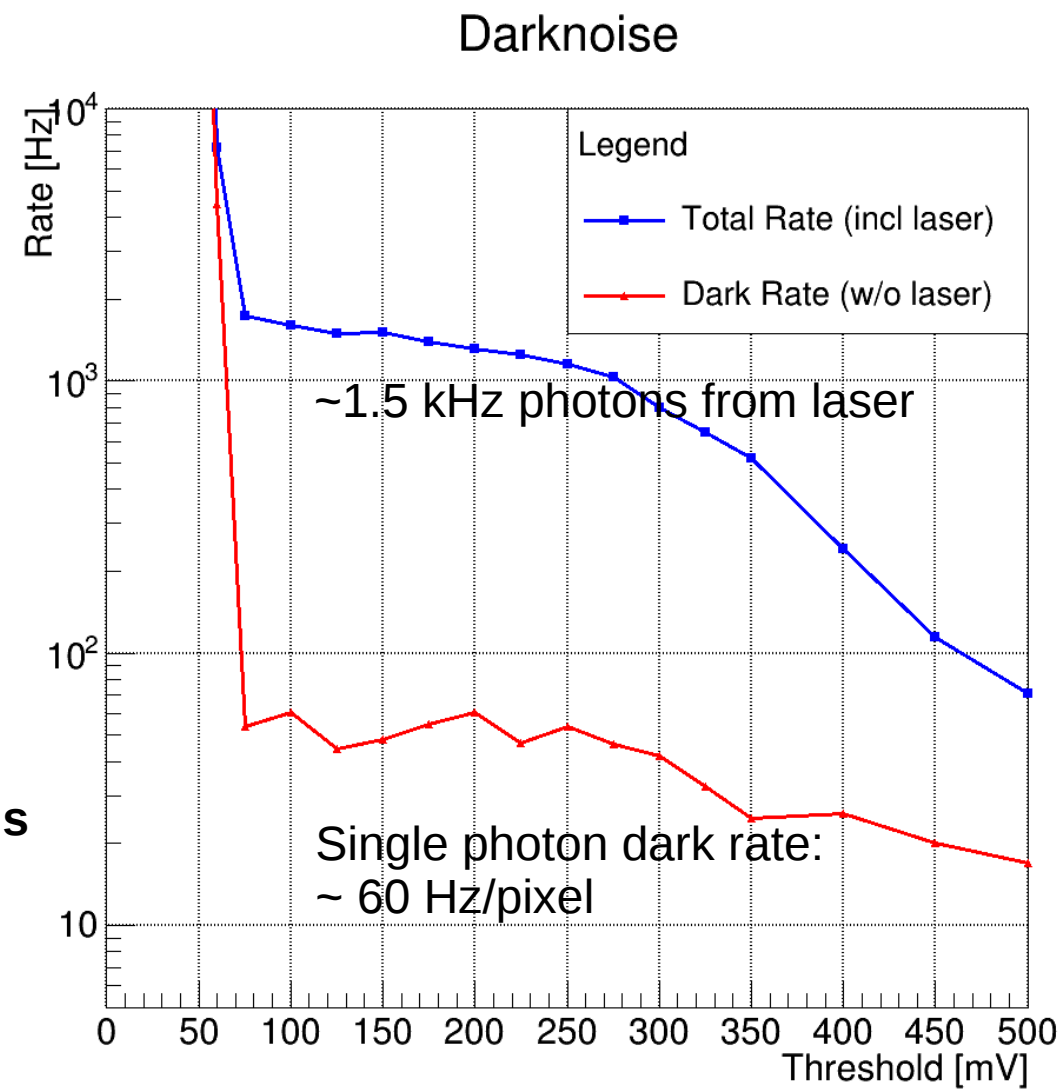
dark noise / electronic noise rate

Opposite strategy:
Laser (unfortunately) on all time:

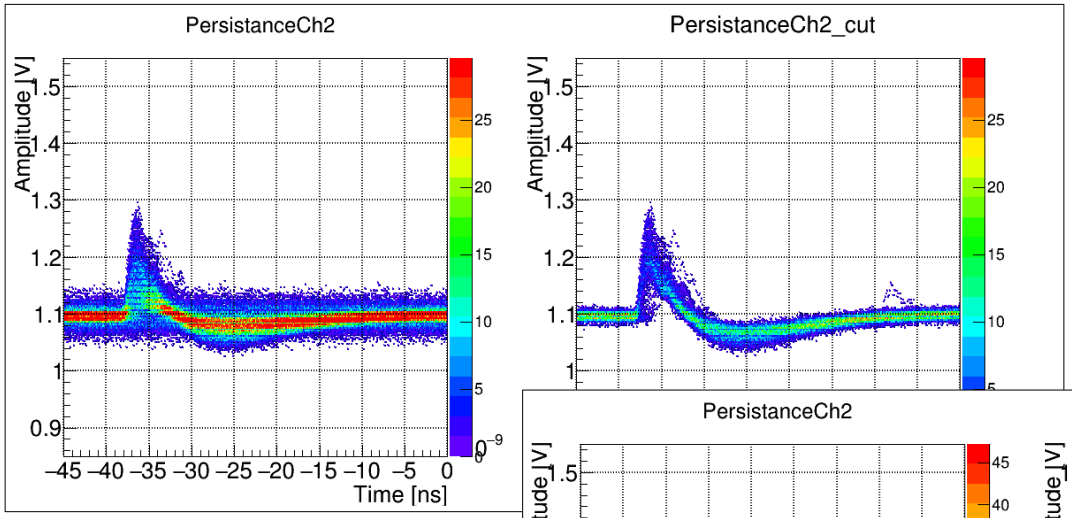
Acquisition trigger ON SIGNAL only,
Threshold 50 mV … 500 mV
10k acquisitions per thresh.
NO trigger request on SYNC signal

Measure time to get 10k acquisitions
→ **Total rate**
(incl. ~1.5 kHz photons from laser)

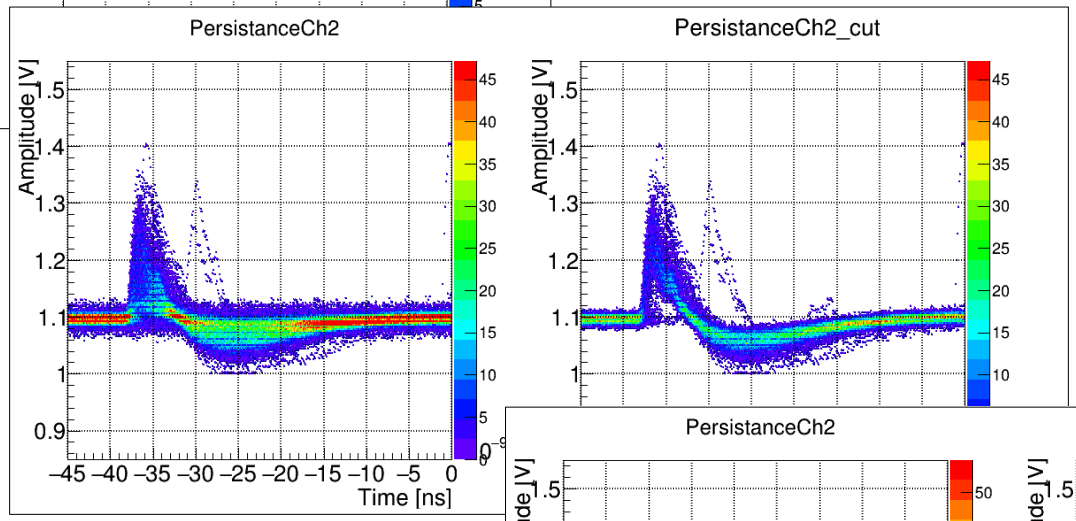
Additional offline cut:
NO SYNC signal correlated to signal
→ **Real dark rate without laser photons**



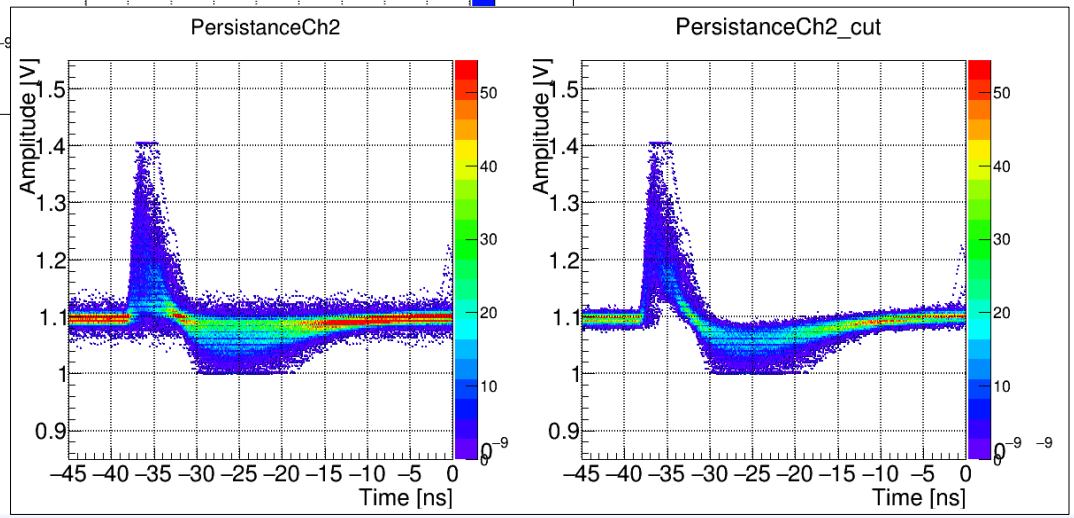
MCP HV scan



1700 V



1800 V

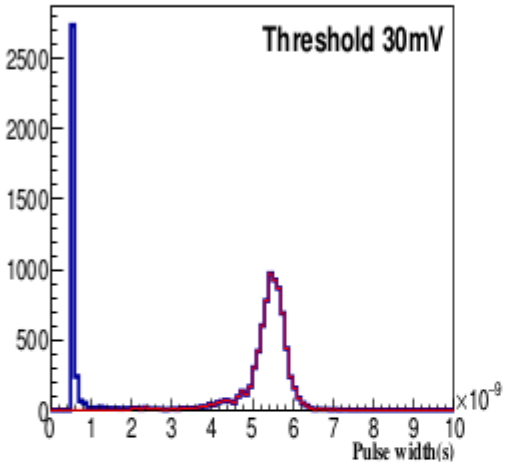


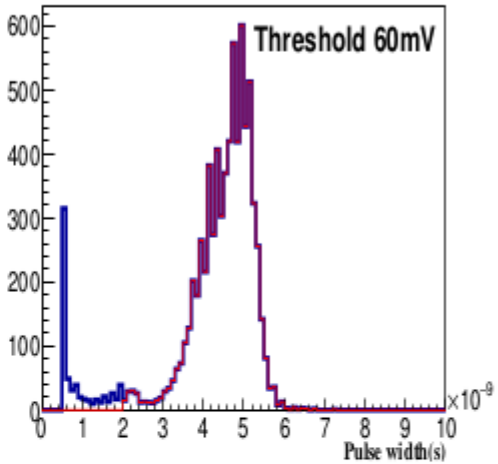
1900 V

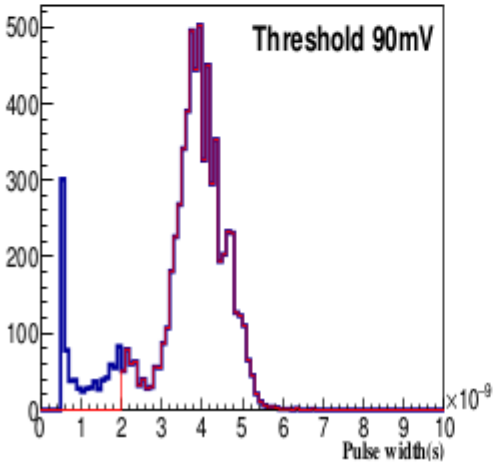
BERGISCHE UNIVERSITÄT WUPPERTAL

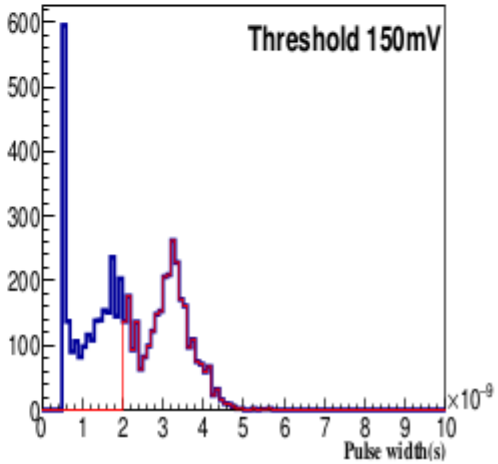
ToT distribution as funct. of threshold MAPMT, scope analysis

ToT(Pulse width)(blue:no Tot cut red:ToT>2ns)







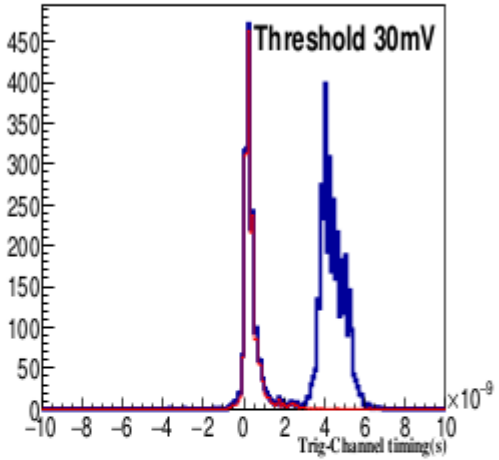


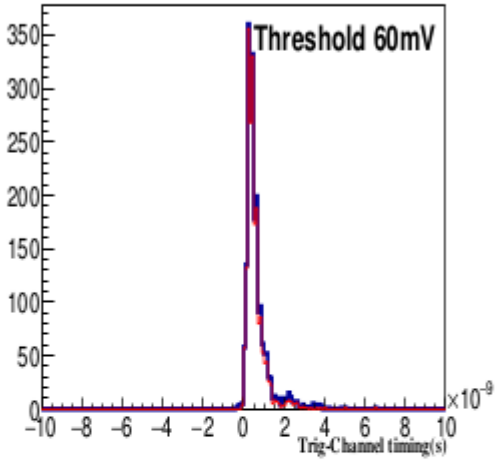
V. Patel, BuW

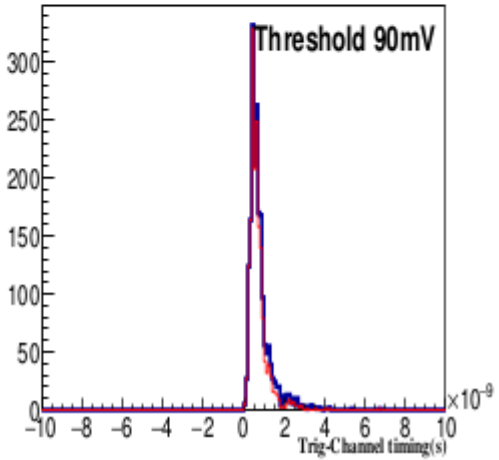
BERGISCHE UNIVERSITÄT WUPPERTAL

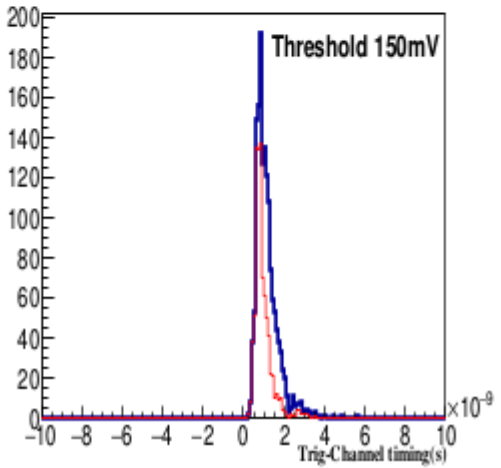
Leading edge timing as funct. of threshold MAPMT, scope analysis

Leading edge timing(blue:no Tot cut red:ToT>2ns)







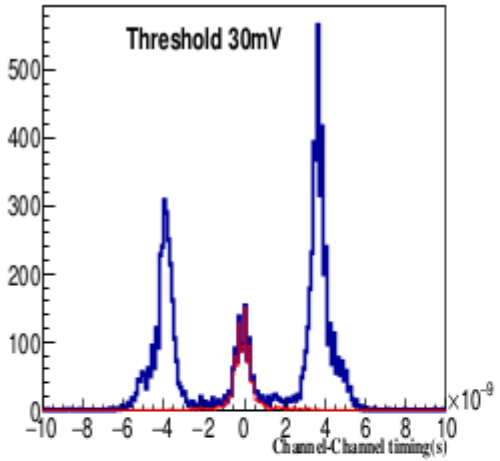


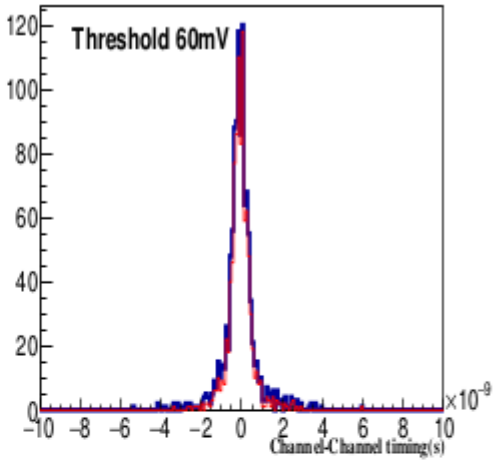
V. Patel, BuW

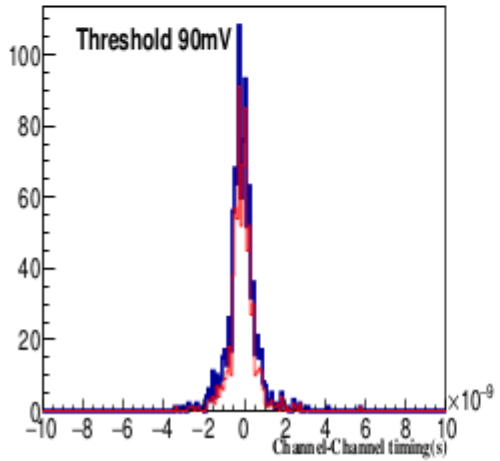
BERGISCHE UNIVERSITÄT WUPPERTAL

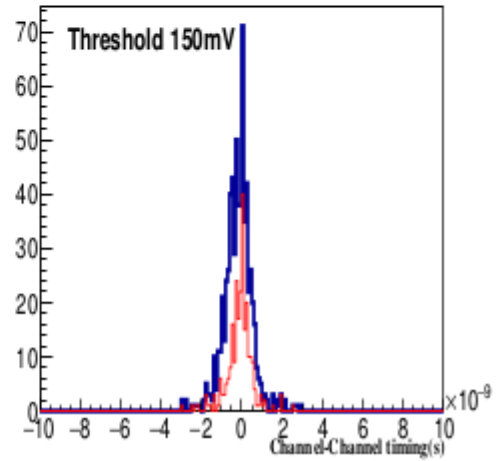
Timediff channel – channel MAPMT, scope analysis

Time-diff channel-channel, blue: no cut, red : ToT>2ns





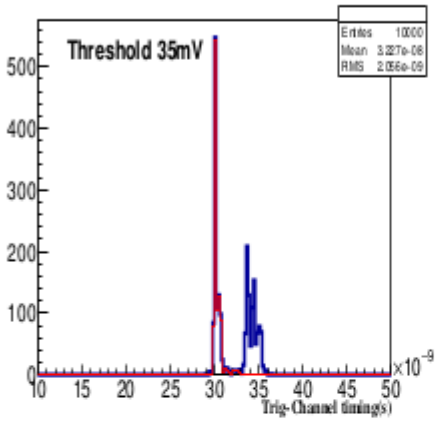


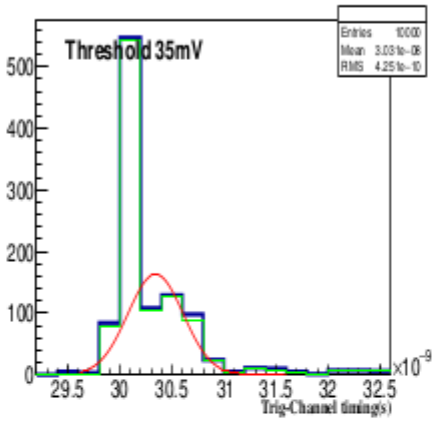


V. Patel, BuW

Timing precision in scope analysis MAPMT

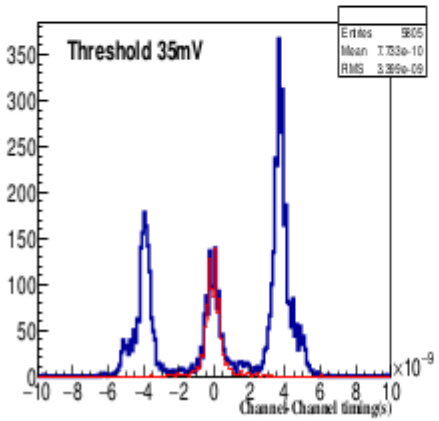
Leading edge timing(blue:no Tot cut red:ToT>2ns)

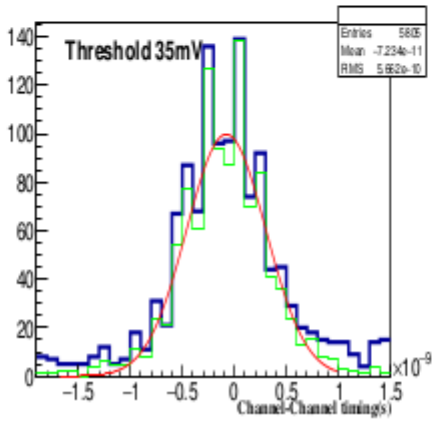




RMS : 420ps
Gauss fit : 300ps

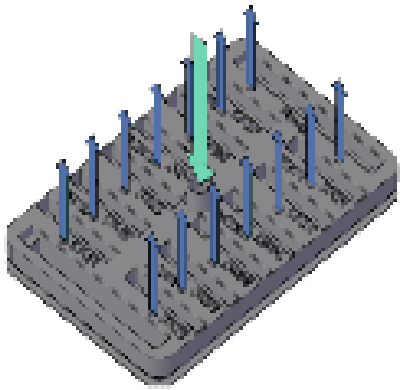
Leading edge timing(blue:no Tot cut red:ToT>2ns)

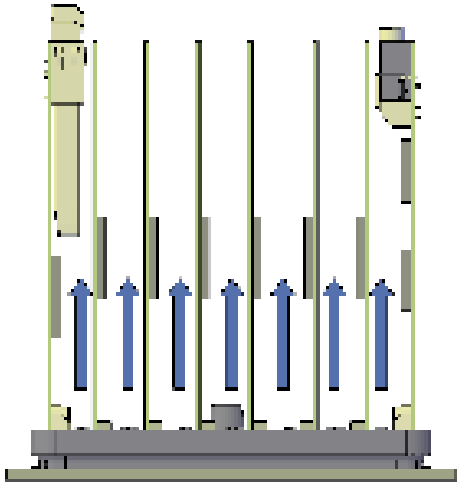




RMS : 500ps
Gauss fit : 360ps

V. Patel, BuW



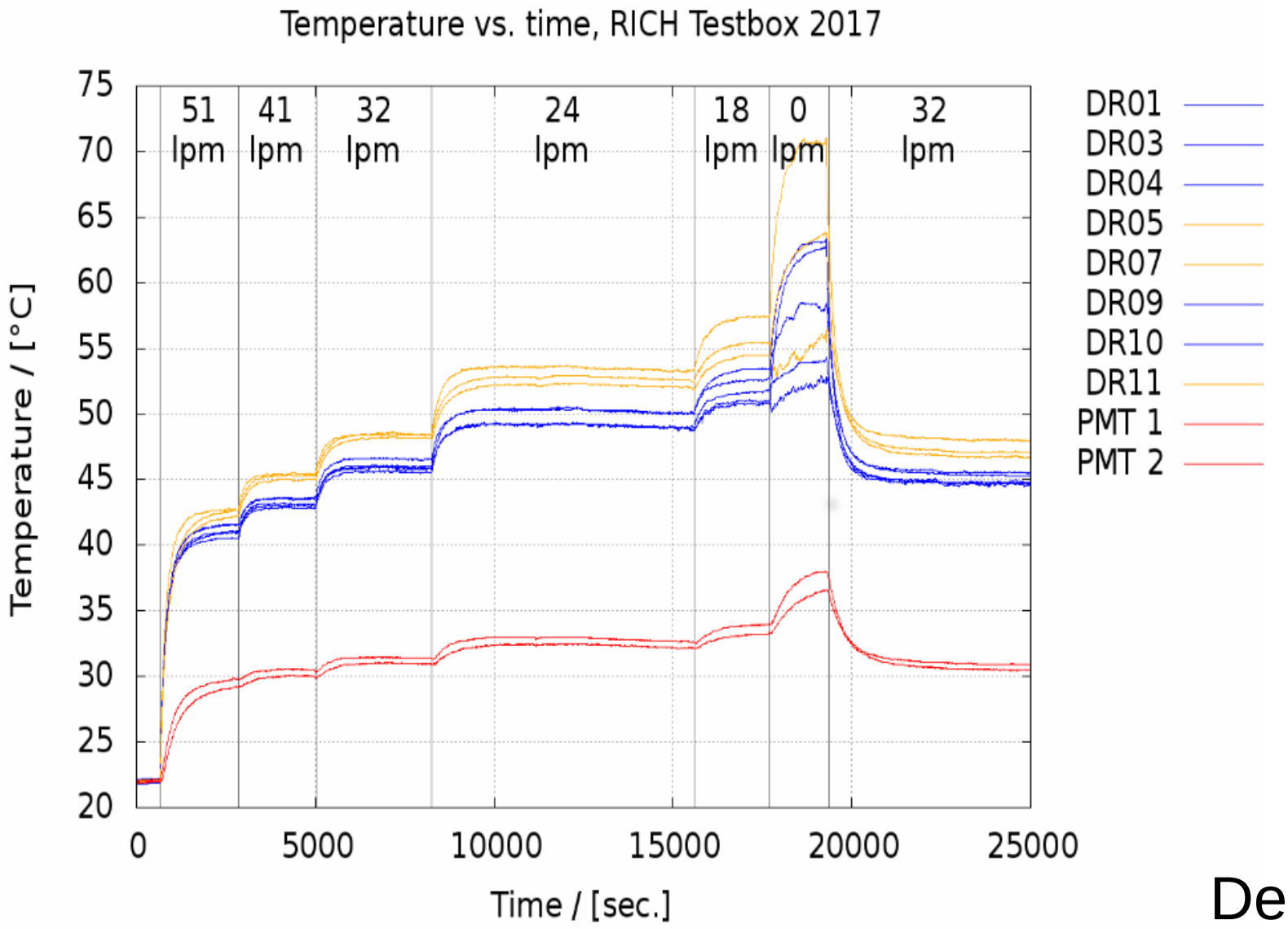


- Dennis Pfeifer

- Mask of plastic with integrated air tubing Central socket for the Air supply, compressed air generator Escape holes for each module
- Serves double purpose:
  (i)Light shield on top of backplane
  (ii)Distribution of cooling air
- Questions:
  - How much compressed air do we nead?
  - How much is available in the cave?

BERGISCHE UNIVERSITÄT WUPPERTAL

Cooling with compressed air via 3d mask on backplane



Dennis Pfeifer