Towards a DAQT TDR

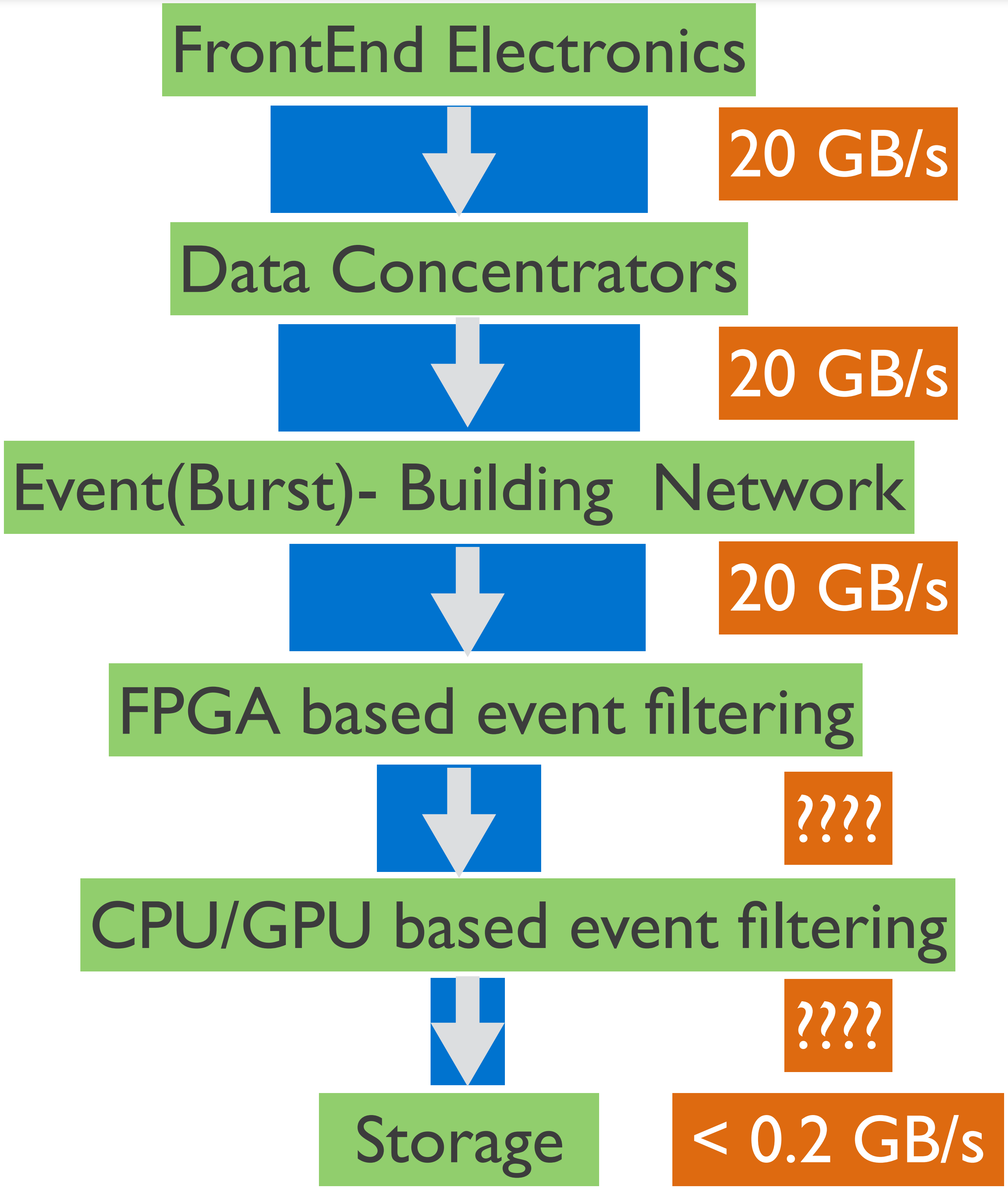
March 2016

Contents of Phase 1 TDR

- **Introduction** : physics objectives, detector configuration
  - Cross sections, luminosities, detector performance (tracking, EMC, PID …)
- **Requirements** (event rates, event size, pile-up situation, storage capacity, event filtering capabilities, partitioning of DAQ, running modes…)
- **System architecture**
  - Building blocks (time synchronisation (SODAnet), data concentrators, data transport, FPGA based Compute Nodes, CPU/GPU farm, …)
  - Data format, interfaces and data flow
  - Event filter: partitioning and performance of algorithms (L1, L2), …
  - Run control system, error detection and recovery, Data Quality Monitoring (DQM)
- **Performance** simulations and measurements with prototype systems
- **Manpower, schedule and cost**

DAQ Architecture

- Assumptions for Phase I
  - up to 10^6 events/s - 20 GB/s
  - separate runs for physics with "large" vs. "small" cross sections
  - negligible overlap between events (needs to be checked by simulations)
  - Final reduction factor for small cross section physics: 100
  - Large cross section physics requires reduced luminosity due to storage limitations



Definition of requirements

- Detector configuration and physics programme of Phase I needs to be defined - **urgent !!**
  - Cross sections, background situation
  - Event rate, event size and required rejection factors, acceptable efficiency loss
    - Need simulation of gas detector performance to explore/define "safe" rate before pile-up destroys rejection capability for event-based approach

Partitioning and Performance of Event Filtering

- **Note: Event filtering does not mean "triggering" !**
  - Our task is **rejection of events** which are not interesting up to the point that we can **store all remaining events** of potential interest
  - The resulting events sample will still contain a majority of events which will later be rejected by offline analysis
- We need to reconstruct the events both with the full off-line algorithms and with fast algorithms based on FPGA hardware. So far only available for STT.
  - Example: STT tracking in FPGA takes 7 us / event vs. much longer but with better resolution with offline algorithm
  - This information is needed to define the partitioning of the event filter

Performance estimates: CPU/GPU Online Farm

- Example: **Belle II High Level Trigger**
- 30 KHz - 2 GB/s
- Execution time for a single hadronic event: 1 s / average execution time /event = 0.3 s
  - 7000 cores to be purchased until end of 2019
  - Cost : 400 K€ + infrastructure
- PANDA resources (green cube): 20000 cores
  - scaling from Belle II HLT: 100 KHz (optimistic !)
    - **Operation at 1 MHz event rate requires rejection factor of 10 in the FPGA layer**

1/7 of
Belle II High level Trigger

Next DAQT Workshop

- April 10/11 (Sporthotel Grünberg, about 80 KM north of Frankfurt)
  - http://www.sporthotel-gruenberg.de
  - Please register as soon as possible - **definitely before end of March**
    - http://indico.uni-giessen.de/indico/conferenceDisplay.py?ovw=True&confId=226
    - **There is only a limited number of rooms available**
    - Will be assigned on a **first come first serve basis**
      - If possible, please share a room with a colleague