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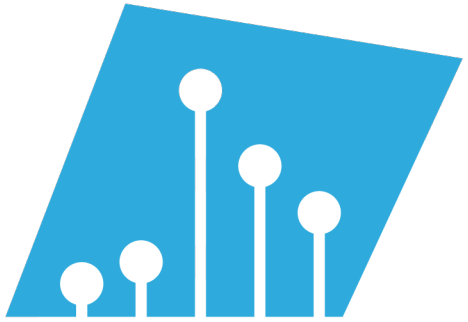

SPADIC

Self triggered Pulse Amplification and Digitization asIC

THE TRD READOUT ASIC 'SPADIC'

P. Fischer & M. Krieger

http://spadic.uni-hd.de

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Original Goals of SPADIC Development (~2006)

TRD readout (electron ID & tracking):

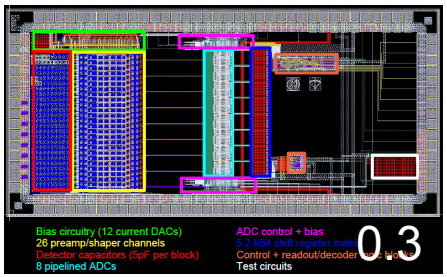
- Event assignment (via time)
- e/π separation via signal shape
  - Shape & time → sample pulse → ADC
  - High rate → eliminate ion tail → (digital) filter
  - High rate → large data volume → high speed IF (CBMNet)

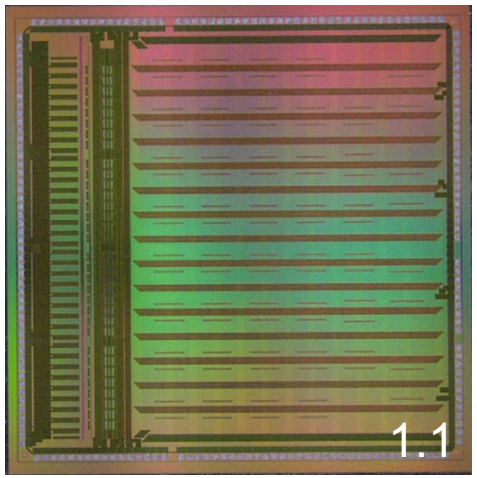
- Concept similar to PASA + ALTRO/TRAP (2 chip solutions)

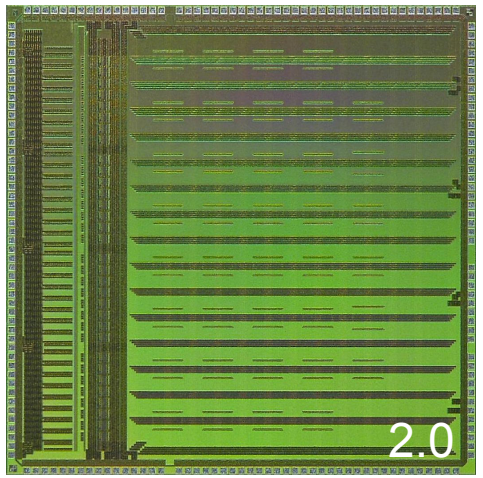
- Aim at a **Single Chip Solution** without external IP
  - Low cost
  - High flexibility to implement what is needed
  - Simple chip mounting (avoid costly Multi-Chip Modules)
  - Compact
  - Get (some) radiation tolerance from DSM technology (UMC018)

History

- 2006: Building blocks (Charge Amplifier, ADC)
- 2009: SPADIC 0.3: Full channels



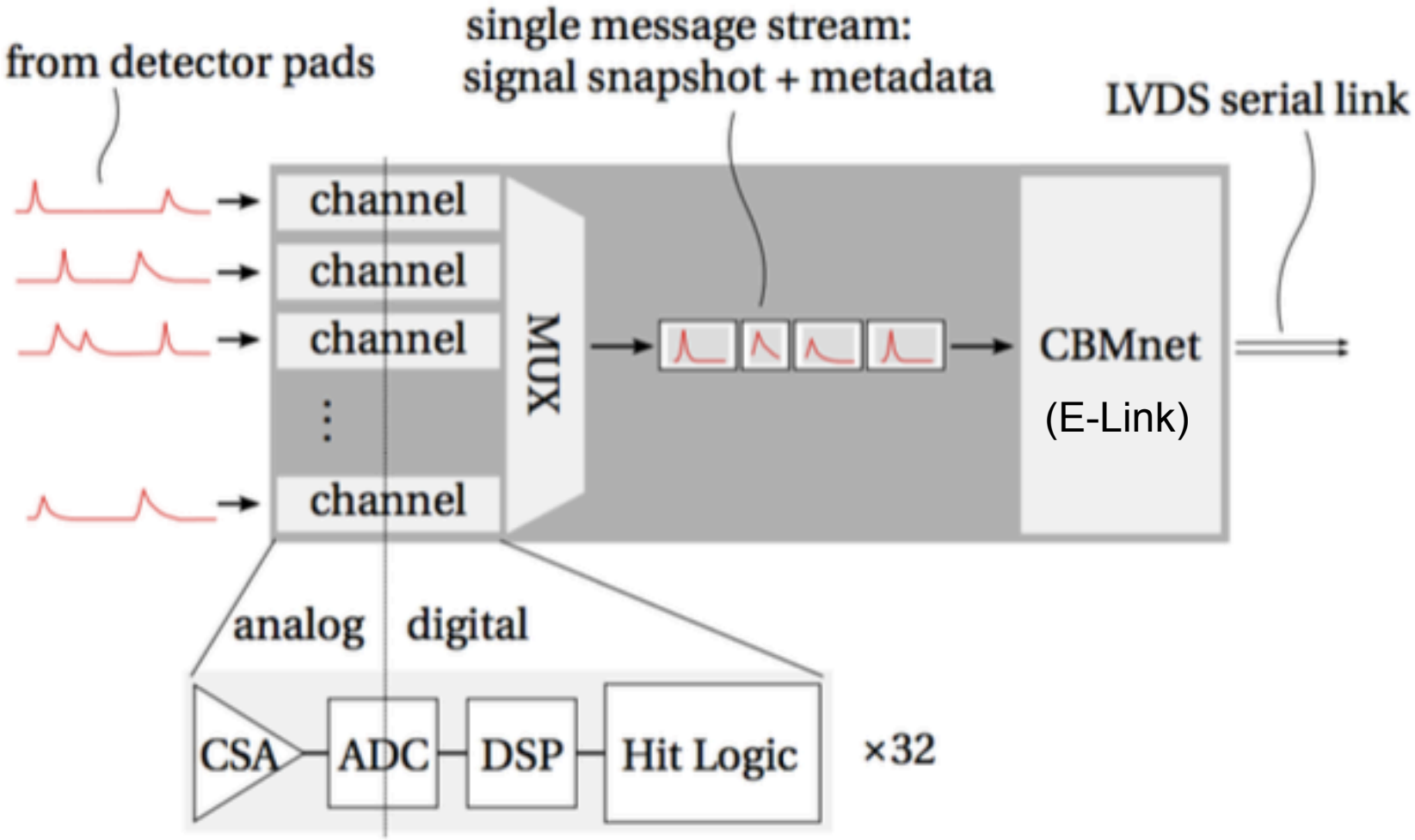




- 2011: SPADIC 1.0: Full 32 channel chip with CBM-Net
- 2015: SPADIC 1.1: Small Bug Fixes (CSA, link, hit detector)
- 2016: SPADIC 2.0: Change in shaping time and sampling, E-Link Interface (from STS-XYTER team)

- Effort: 1 FTE / year (Tim Armbruster, Michael Krieger)

Block Diagram

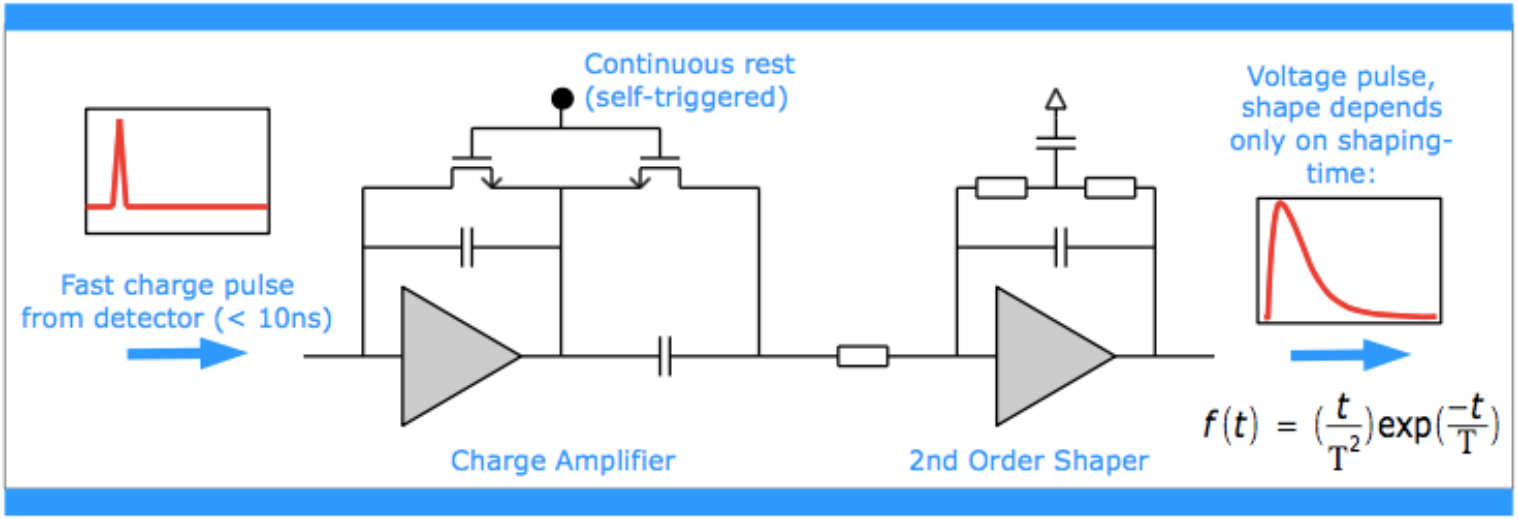


Key Parameters

Chip Size	$5 \times 5\,\mathrm{mm}^2$	
Channels	32	
Total Power	600 mW	
Peaking time of analogue part	80/160 ns	(ENC ~800e @ 90ns, 30 pF)
ADC resolution	9 bit	(EnOB ~ 7.5 Bit)
ADC Sampling frequency	24/16 MHz	
FIR Filter stages (1st order)	4	
Technology	UMC 180nm	
Transistor count	$\approx$ 2.5 M	

- Features
  - Hit Finder with several modes (absolute / differential threshold)
  - Pulse Sampling with arbitrary pulse picking pattern
  - Neighbor Trigger (via LVDS links)
  - Time ordering of hits (per 16 channels)

Charge Amplifier / Shaper

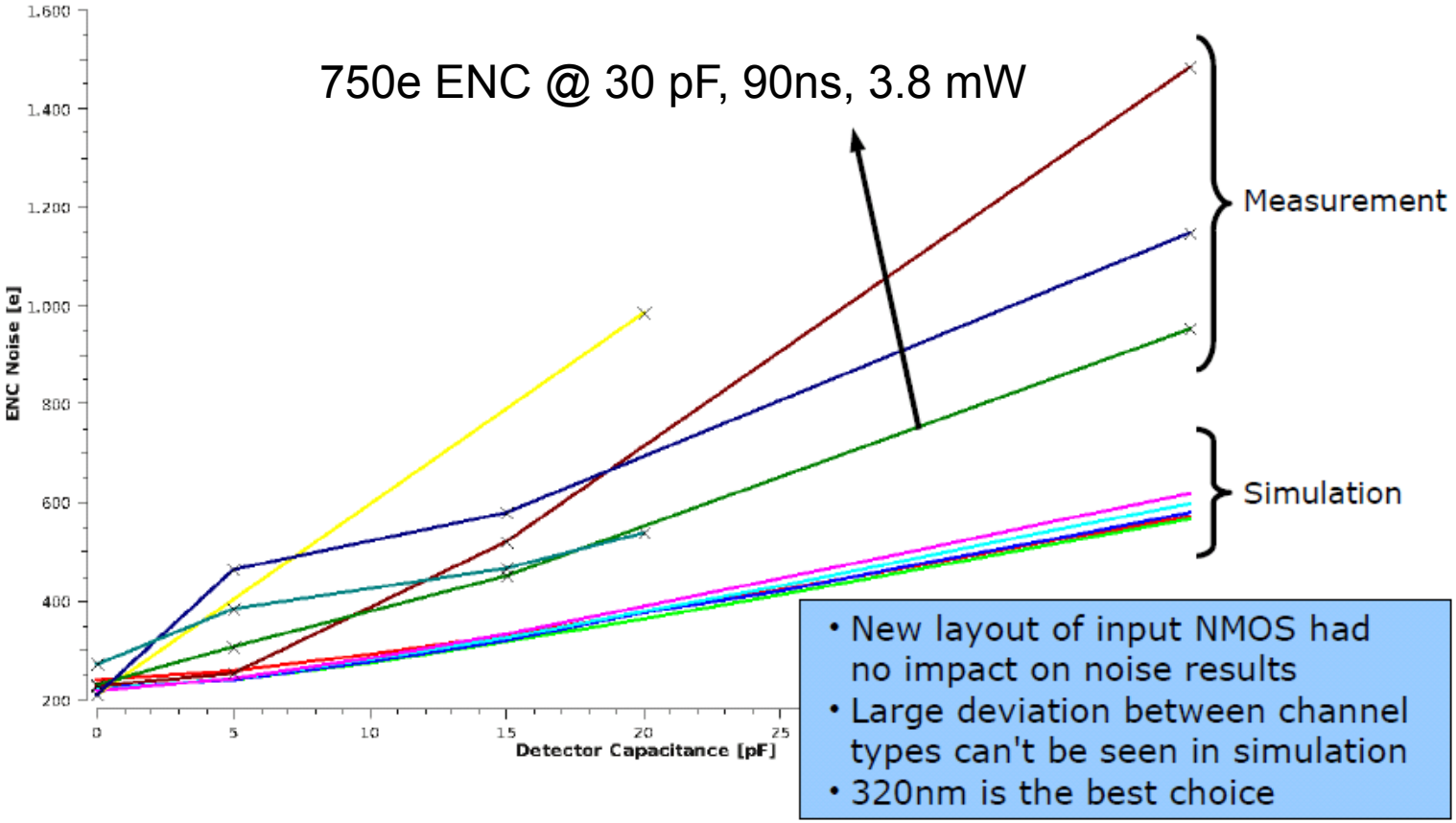


- Positive and negative polarity available, Q_{max} = ±75 fC
- Pole-Zero compensation
- CR-RC Shaping
- P_{CSA} = 3.8 mW (pos.) / 10 mW (neg., not optimized)
- ENC ~ 200 e^- + 20 e^- / pF

- Pulse Monitoring on analogue pad

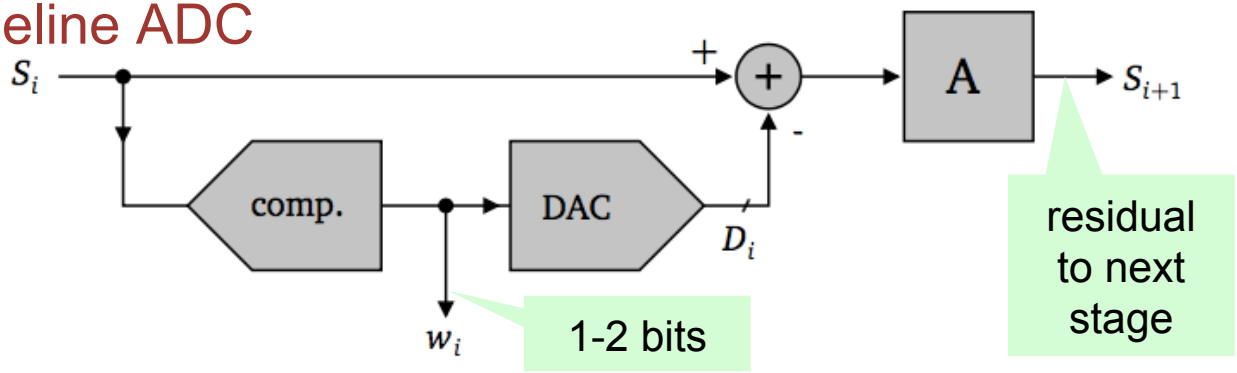
CSA Noise

- Simulated/measured noise for varying transistor length (180-460 nm) do not match (no L-dependence in simulation!)
- Best length of 320 nm determined by test structures

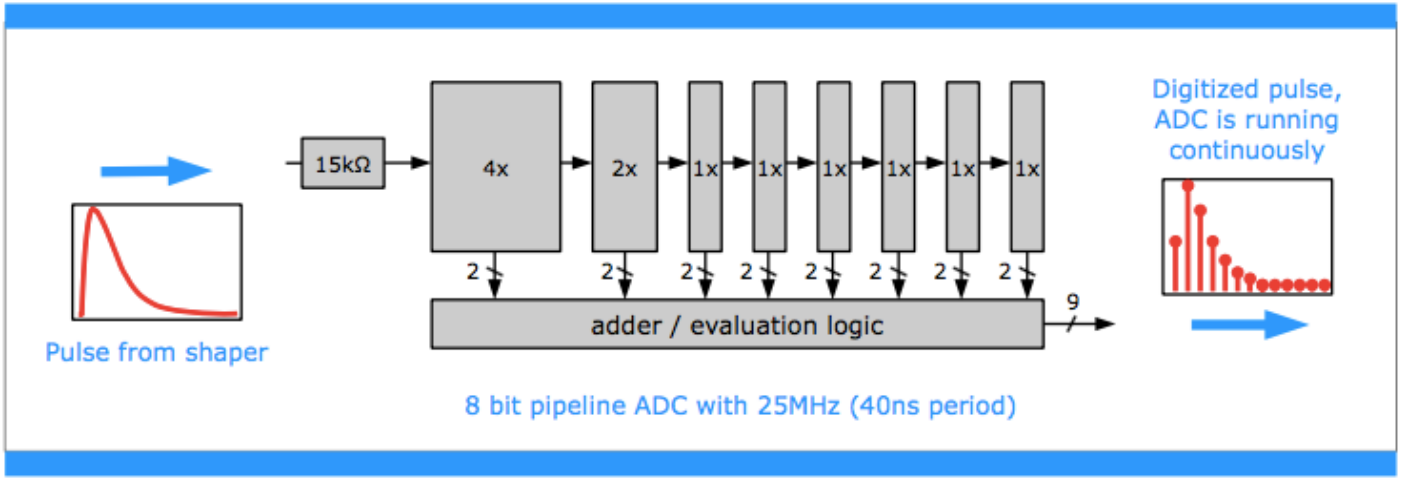


ADC

- Pipeline ADC



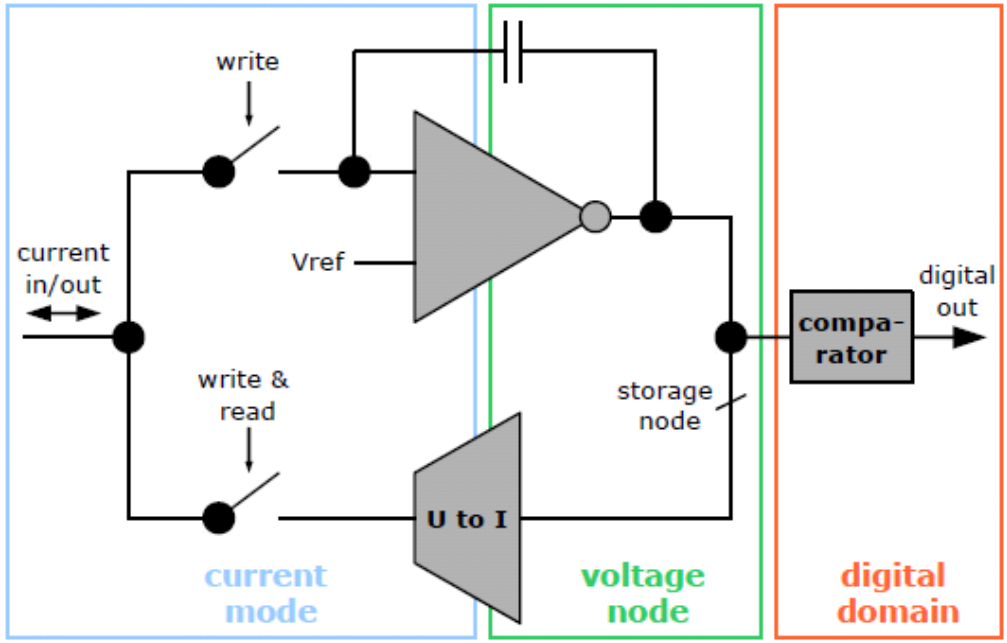
- Scaled Currents for power saving



- 1.5 Bits / stage (error correction)
- 24 MSpS, 9 Bit design

(ADC Current Memory Cell)

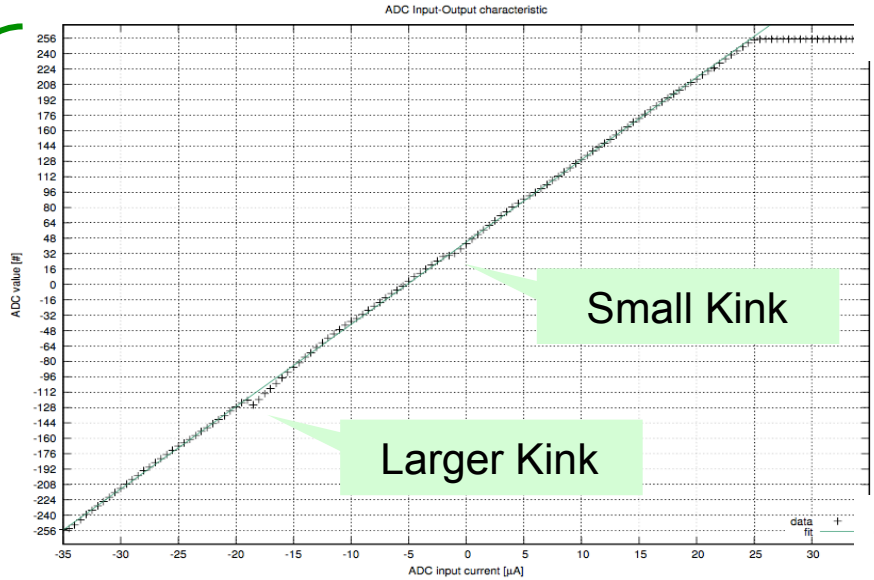
- Current Mode operation
- Novel storage cell:
  - Virtual ground
  - No Early effect
  - Can ‘mirror’ current for comparator

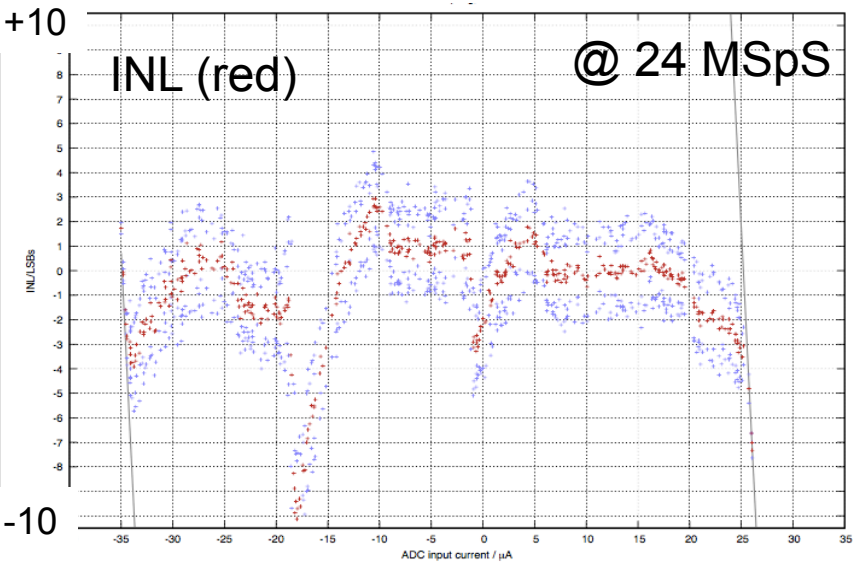


- 'Inherited' from Belle Project (I. Peric), modified by T.A.

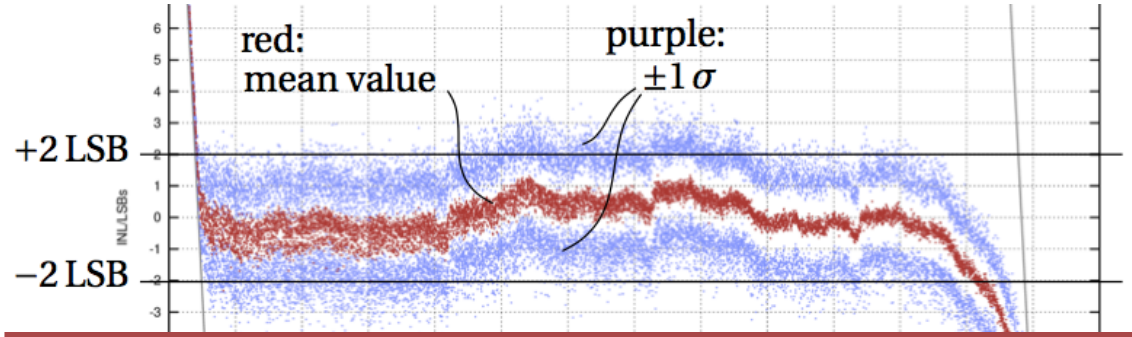
ADC Characteristics

9 Bit



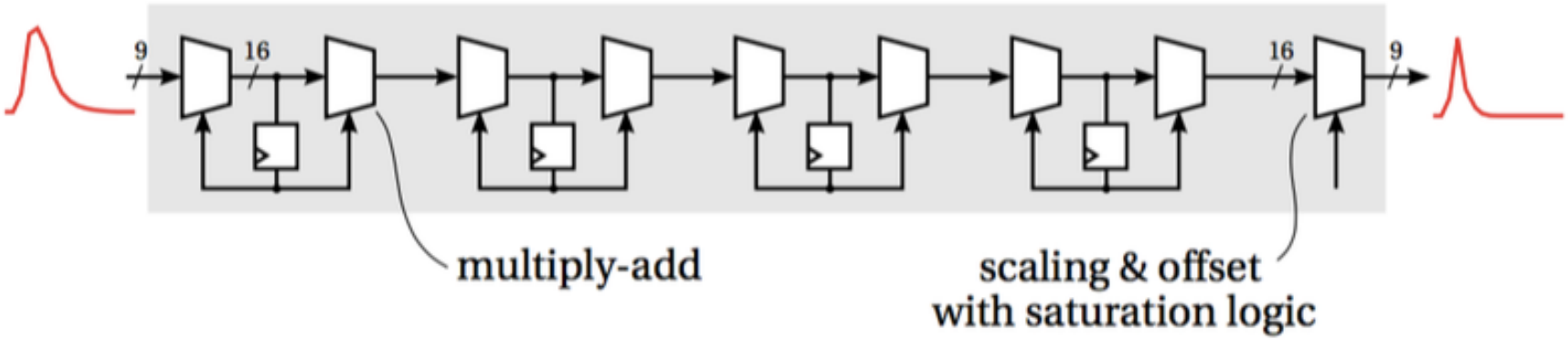


- LSB = 1.8 mV (9 Bit mode), Full scale = 933 mV
- Noise = 0.72 LSB (9 Bit mode)
- After correction, EnOB ~ 7-7.5 Bit (better at lower speed)



@ 20 MSpS

Digital Filter

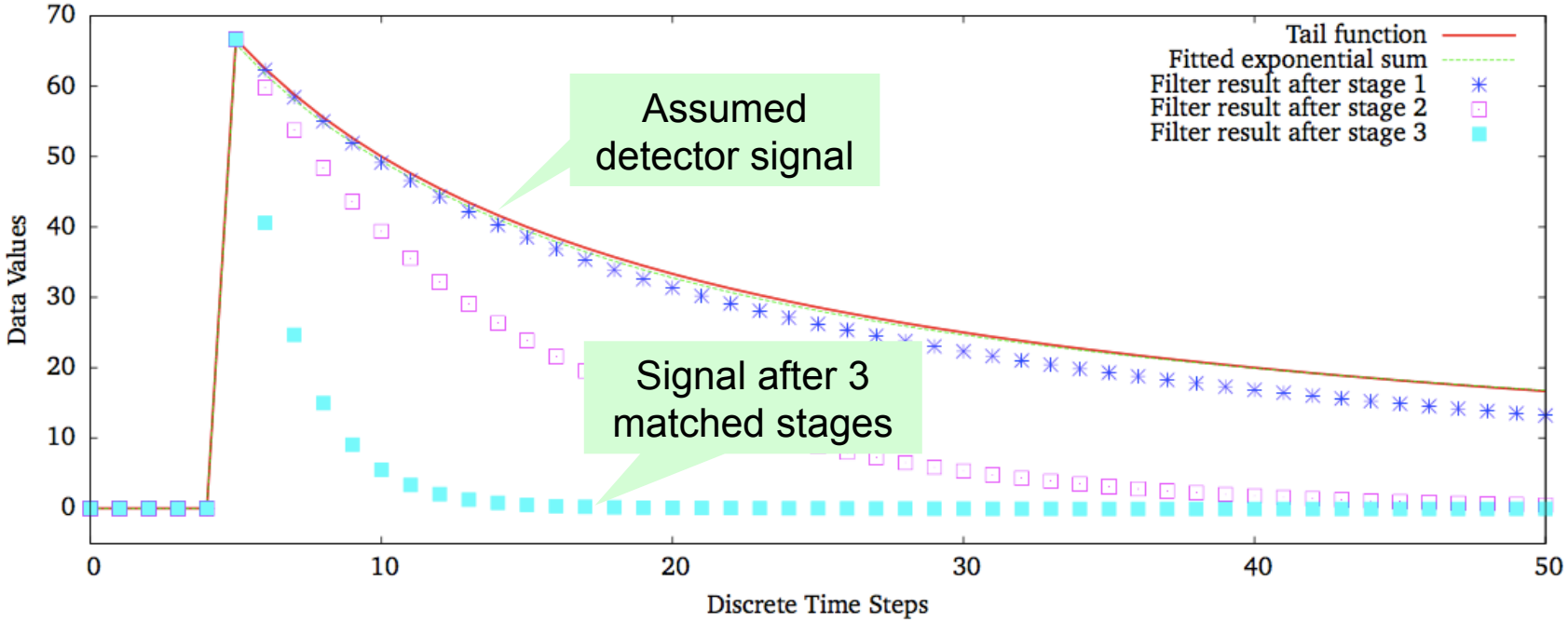


- FIR filter, 4 stages
- Widths of internal processing and coefficients optimized
  - (Diploma M. Krieger)

- Multipliers consume significant digital logic resources

Filter Operation

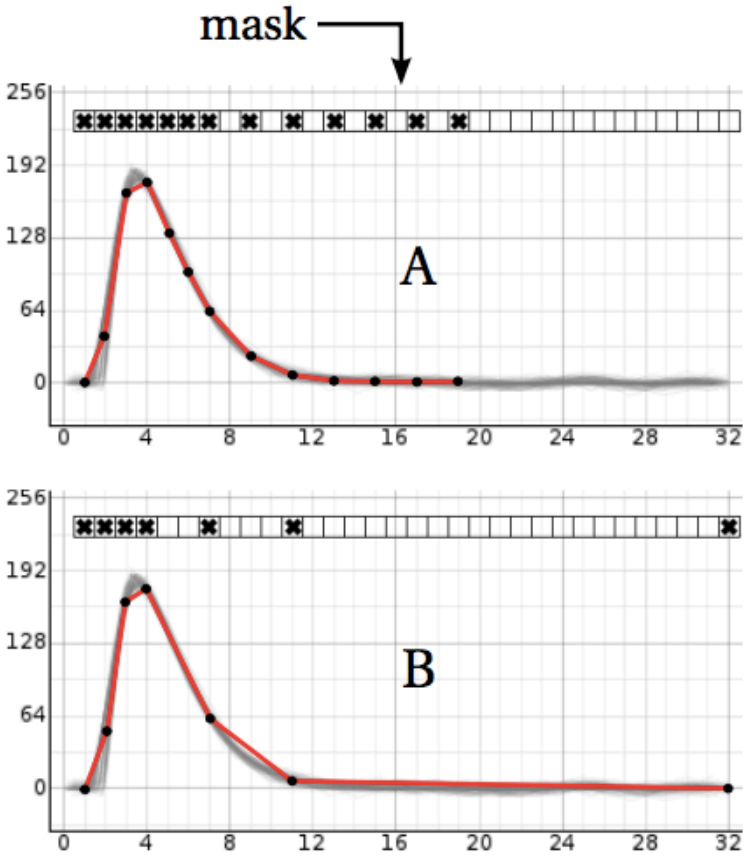
- Can be used to eliminate ion tails
- Can be switched off
- Simulation:



- Note: filter adds noise ('high-pass' function)

Sample Picking

- Mask register allows to pick samples of a pulse to read out
- Pre-samples before pulse are possible (→ get baseline)



message data (hex)

801F
9082
AEEF
5AFF
3FDF
73E1
2840
007E
0F77
47E2
B350

13 samples contained

801F
9E4D
AF0F
52FF
3FCA
404F
4200
B1D0

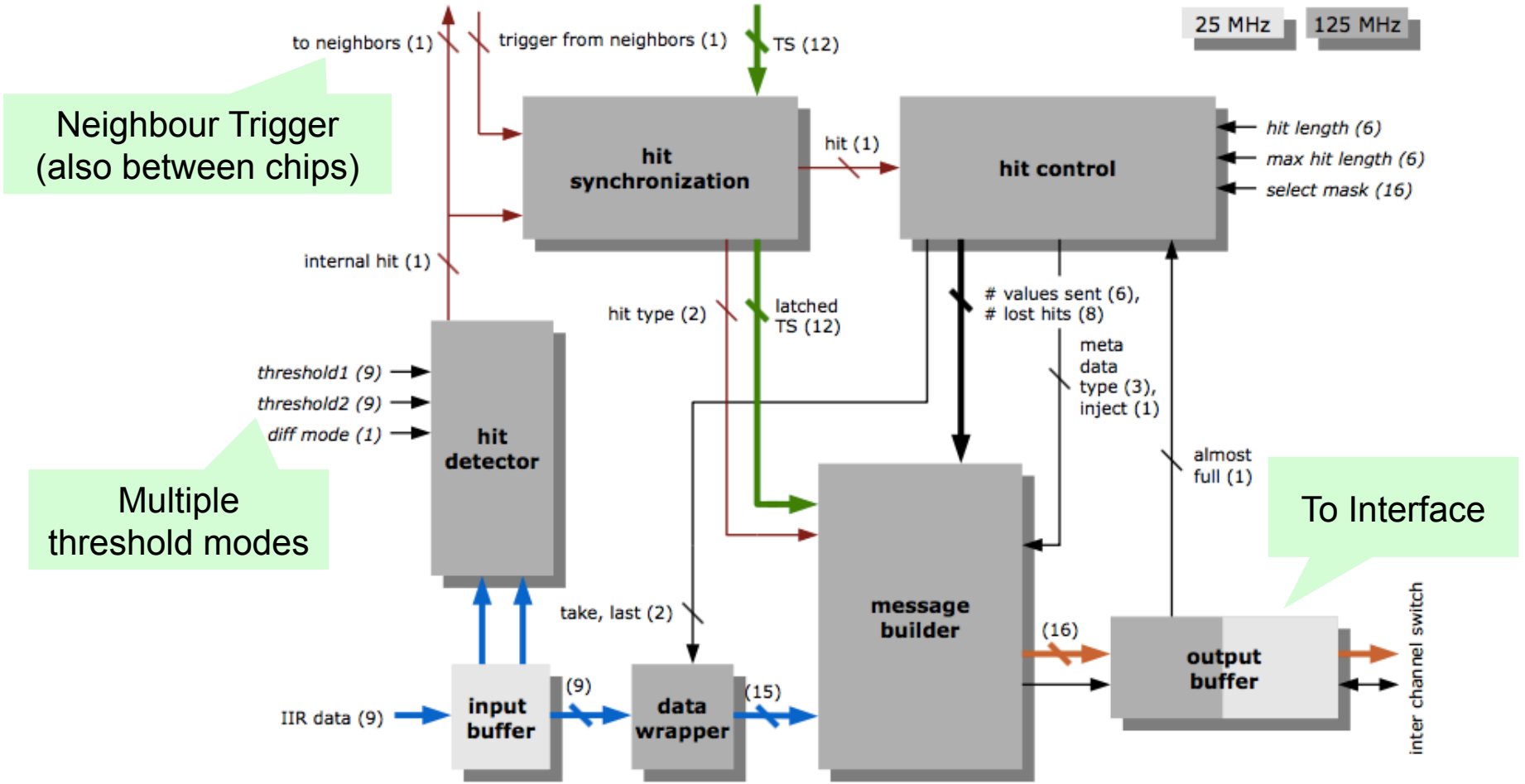
7 samples contained

Number of samples	data words (16 bit)
1	3
2	4
3	4
N (large)	$a + 0.6 \cdot N$

- Trade information vs. data volume:

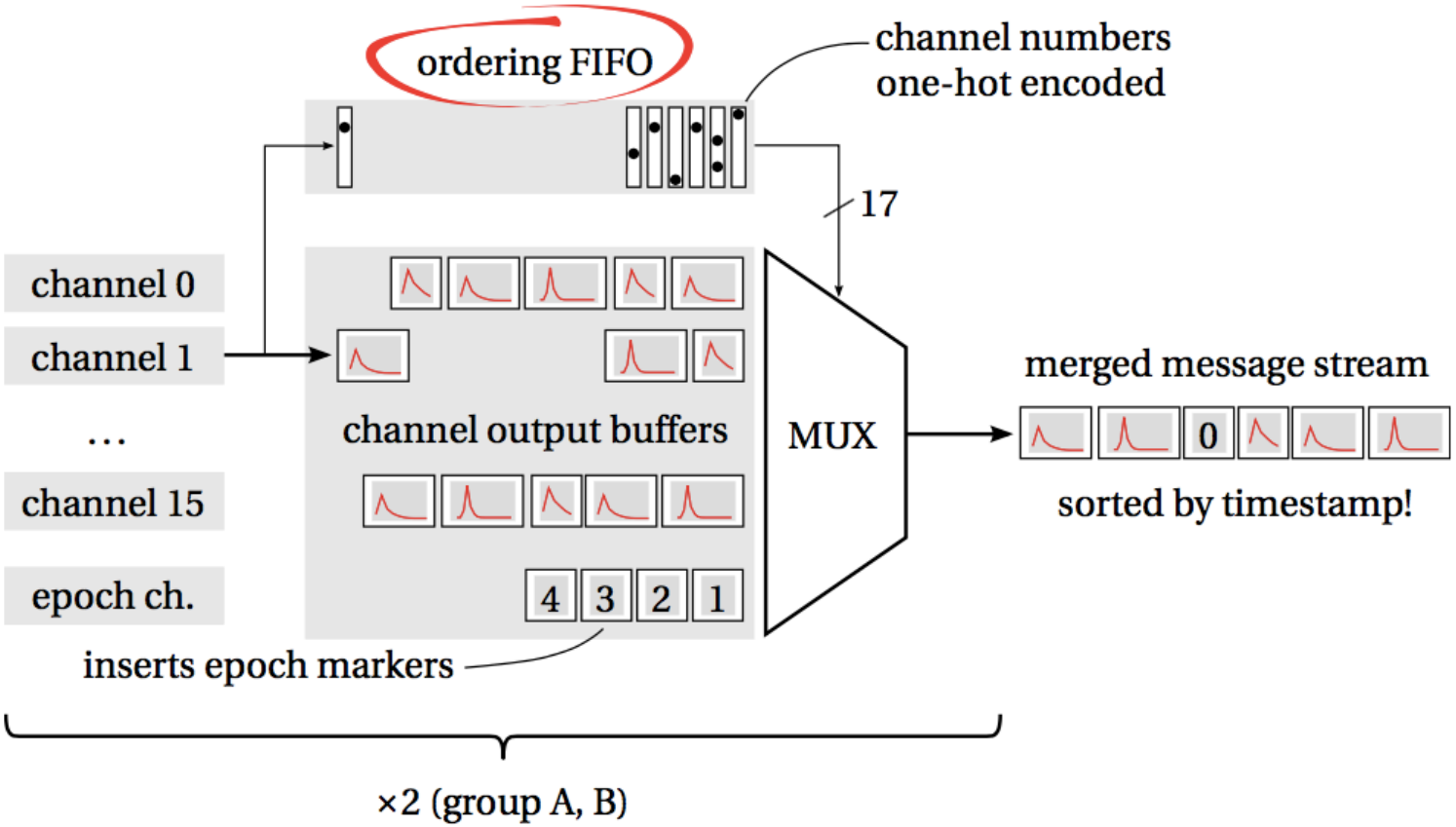
Data Processing

- Quite Complex



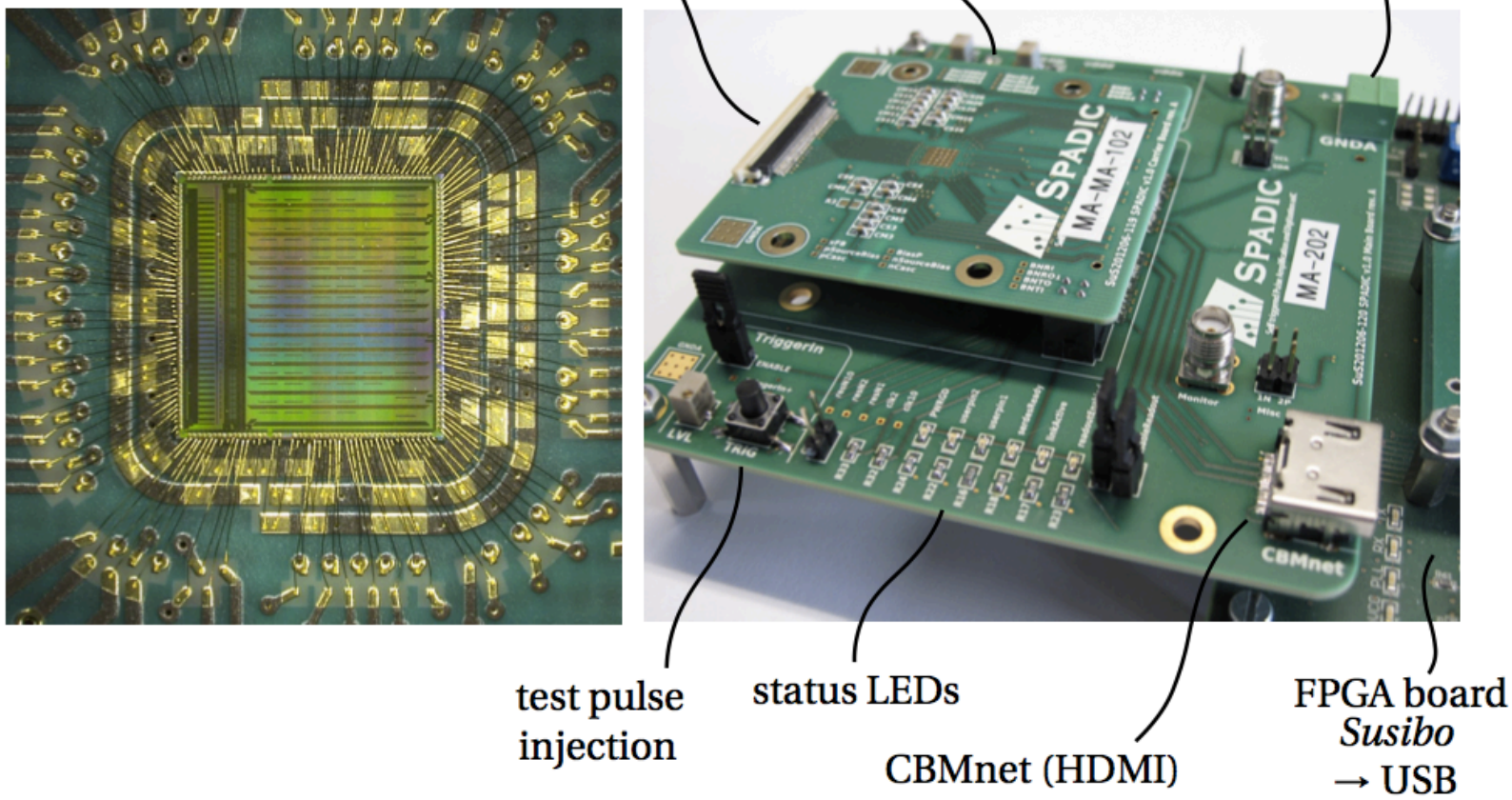
Ordering FIFO

- Sequential data is ordered by time stamps!



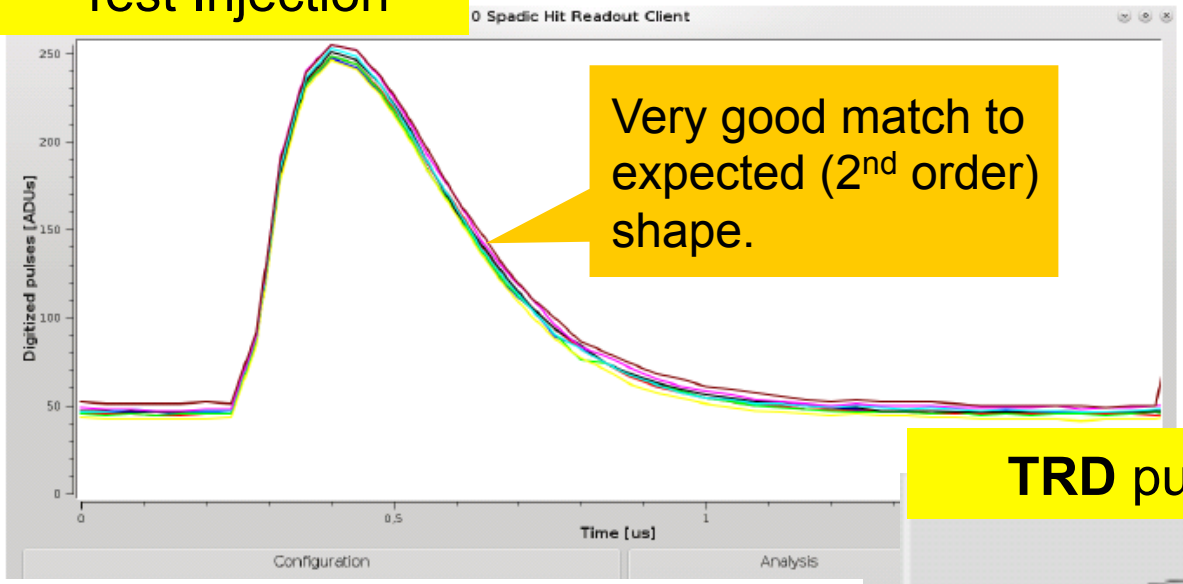
Readout Setup

- Several systems / boards build for various chips
- Measured via USB2.0 readout system ‘SUSIBO’

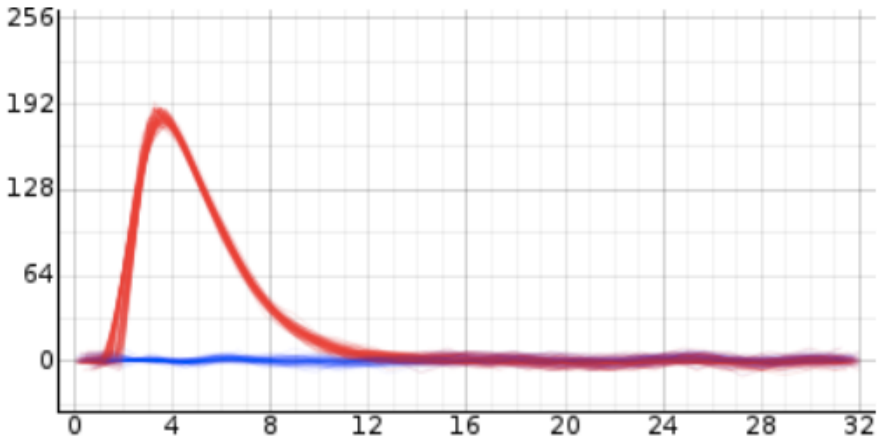


Sampled Pulses

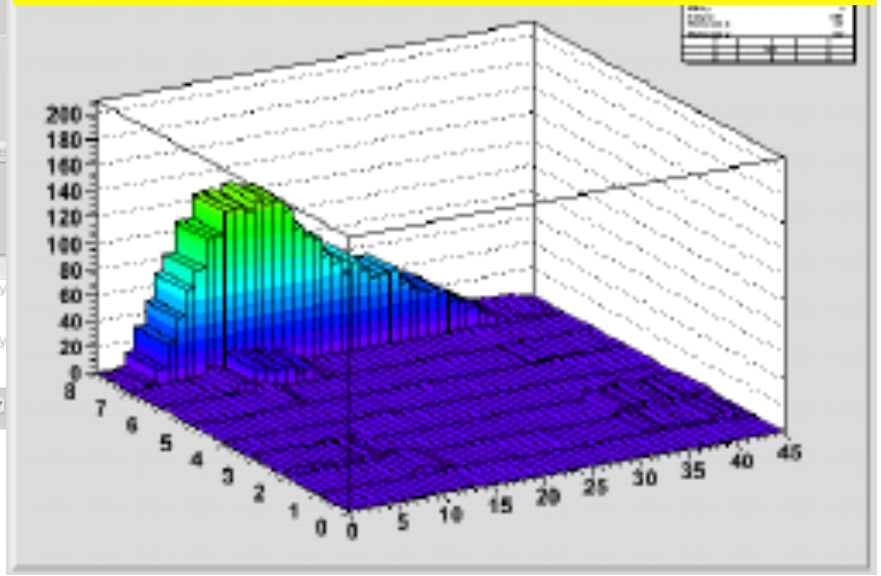
Test Injection



Very good match to expected (2nd order) shape.



TRD pulses @ CERN beam

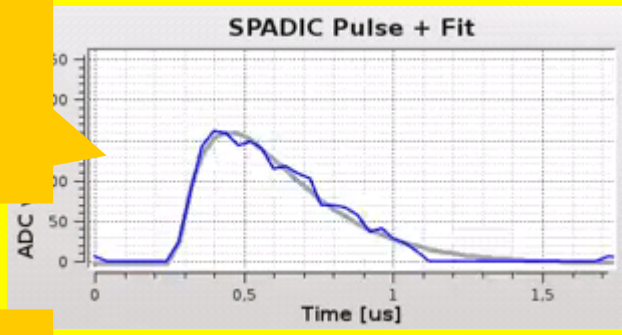


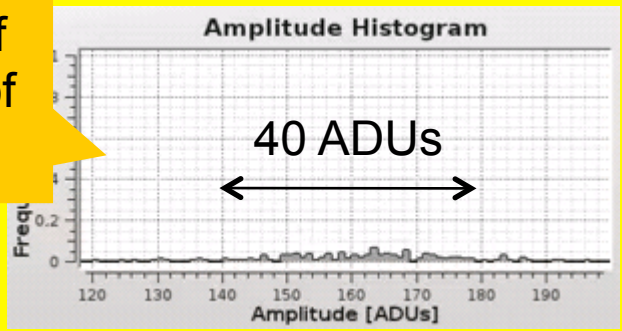
Readout Boards Affect Quality A LOT

- **Same** ASIC, Readout, Detector connected
- Test pulse injections
- www.youtube.com/watch?v=tK7Hm2MSg3Y

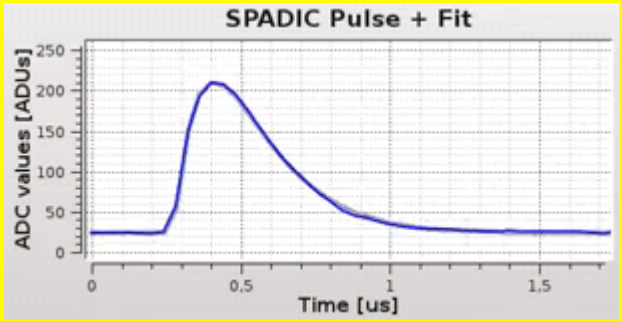
Sampled pulse

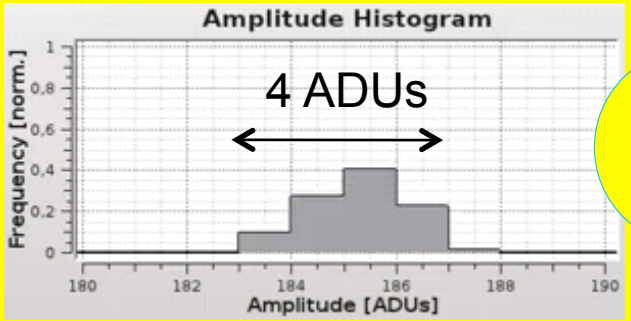
Histogram of Amplitudes of pulse fits





OLD Setup

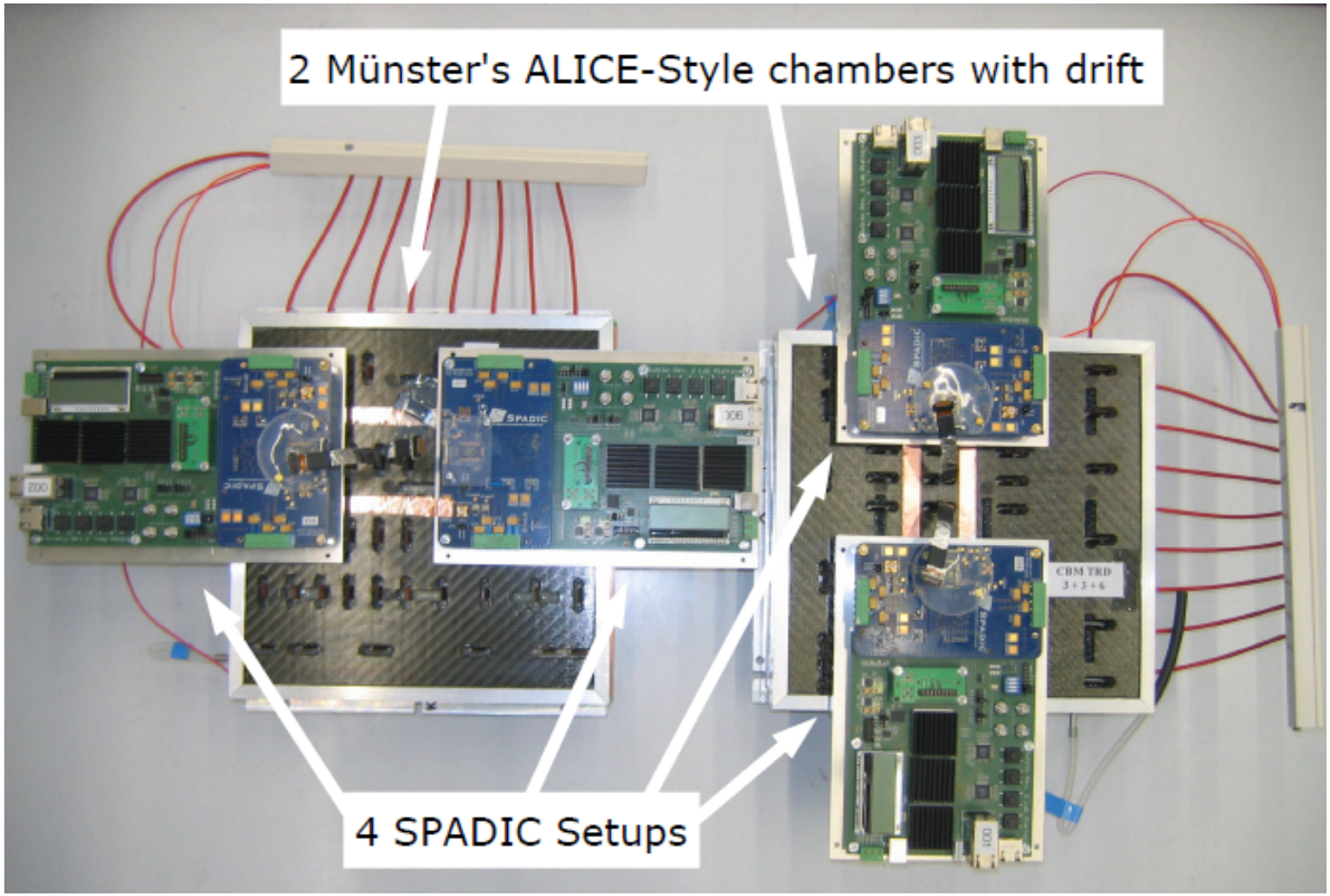




NEW Setup

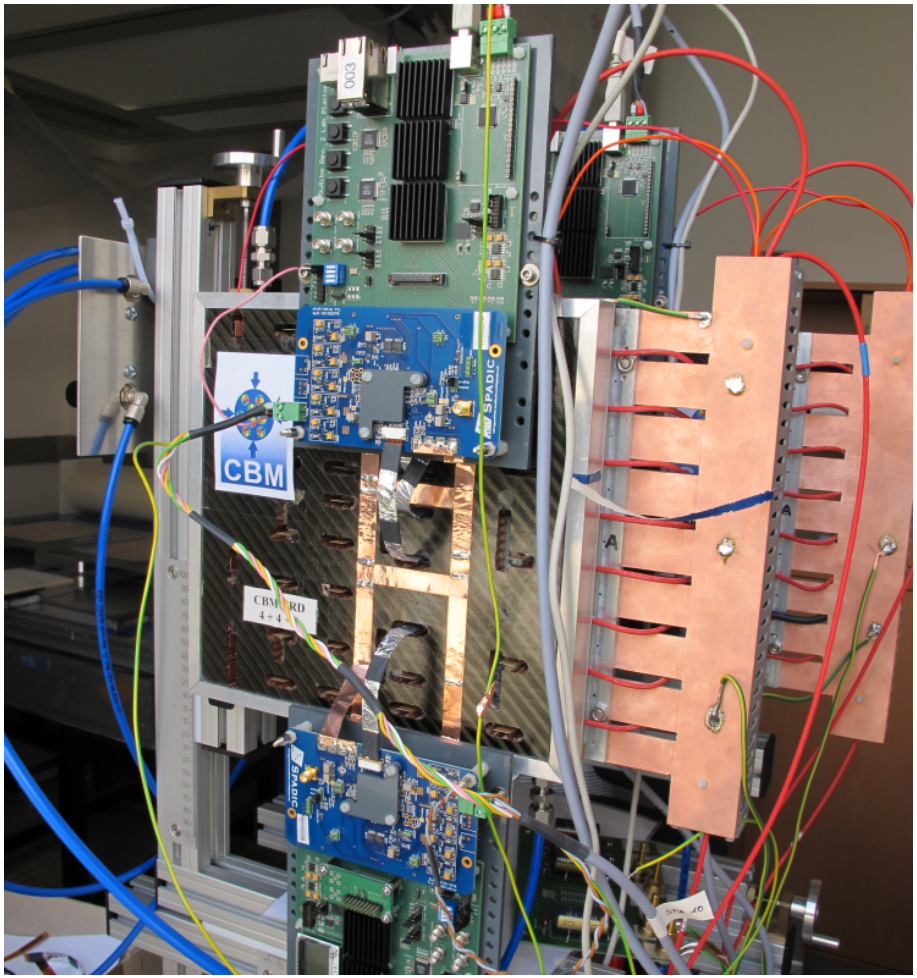
Test Beam Setup

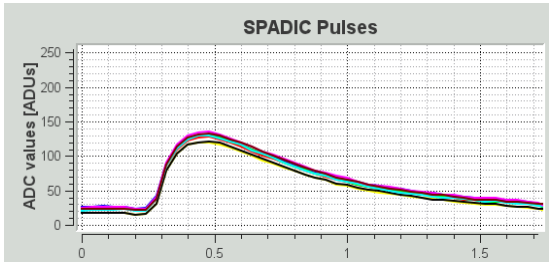
- 4 SPADIC Boards with Interfaces

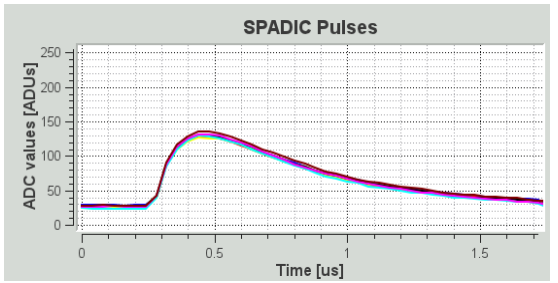


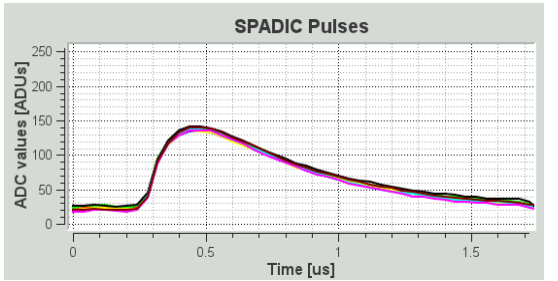
SPADICs on Detectors

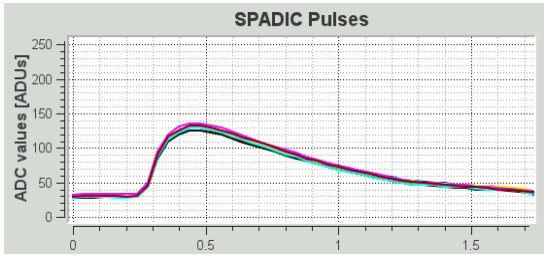
- ‘Münster’ chambers with SPADIC1.0
- Very good noise performance in lab











SPADIC 2.0

- Very close to final chip
- Main motivation: CBMNet → STS-XYTER protocol (E-Link)
- Changes w.r.t. SPADIC 1.0 / 1.1:

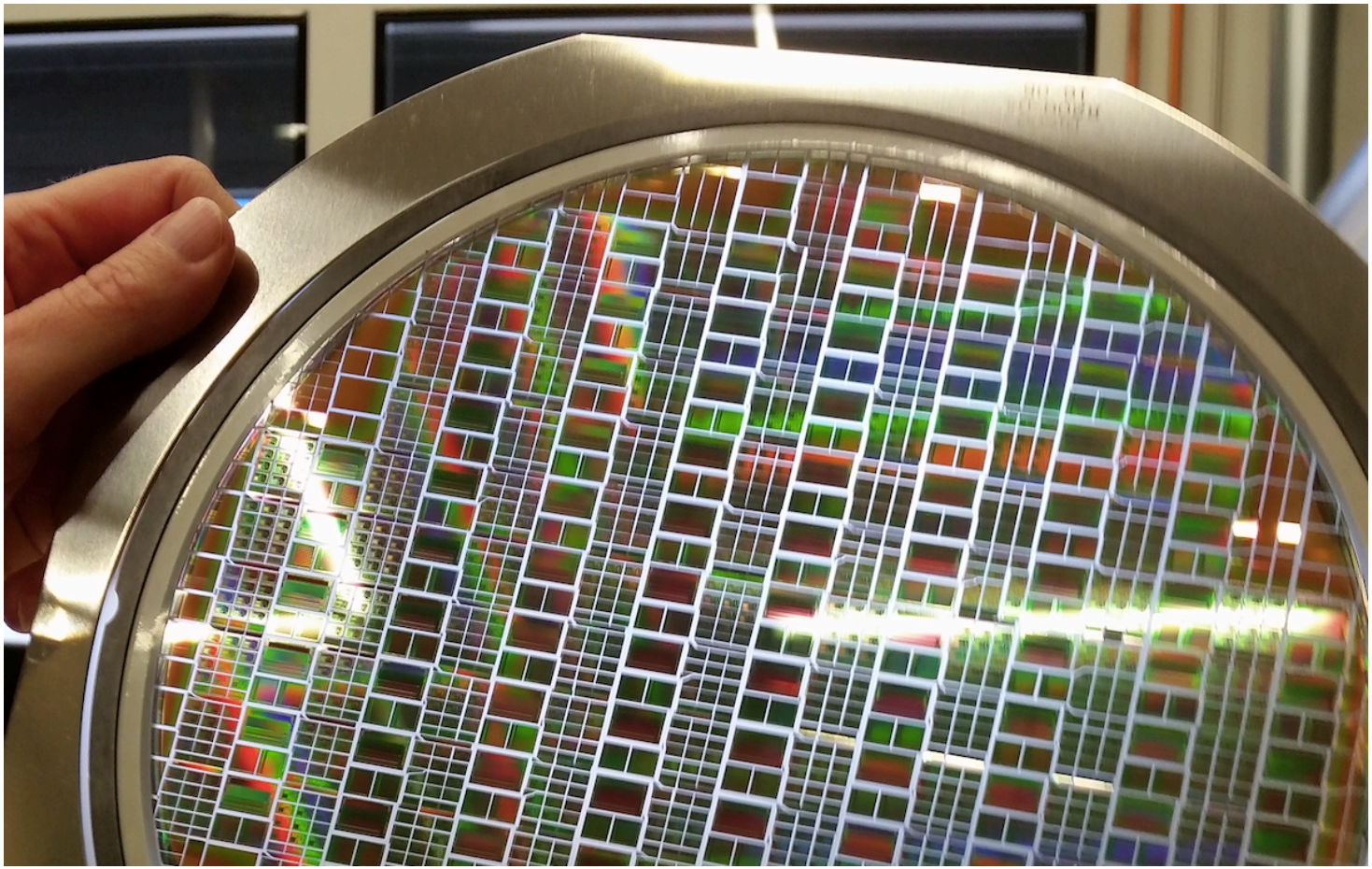
Changes in SPADIC 2.0

CBMnet replaced by STS-XYTER protocol

- **Before:** 25 MHz sampling rate, $\tau = 80$ ns $= 2\ T$
  Now: 16 MHz sampling rate, $\tau = 250$ ns $= 4\ T$
- **Before:** Several SPADIC words in one CBMnet packet
  Now: One SPADIC word in one *uplink frame*
- **Before:** CBMnet packet buffers – DLM needed for synchronization
  Now: No buffering – all *frames* intrinsically deterministic – unified configuration and synchonization interface
- Register size changed from 16 to 15 bits – some registers were split
- No triggering of epoch markers needed anymore
- One more “presample”

SPADIC 2.0 Production

- SPADIC 2.0 was produced as part of a CBM engineering run



SPADIC 2.0 packaging

- SPADIC 1.x were in expensive 'prototype' package
- SPADIC 2.0 is in cheap plastic QFP208 package
  - 2 $ / piece in large quantities
- 200 packaged chips are available

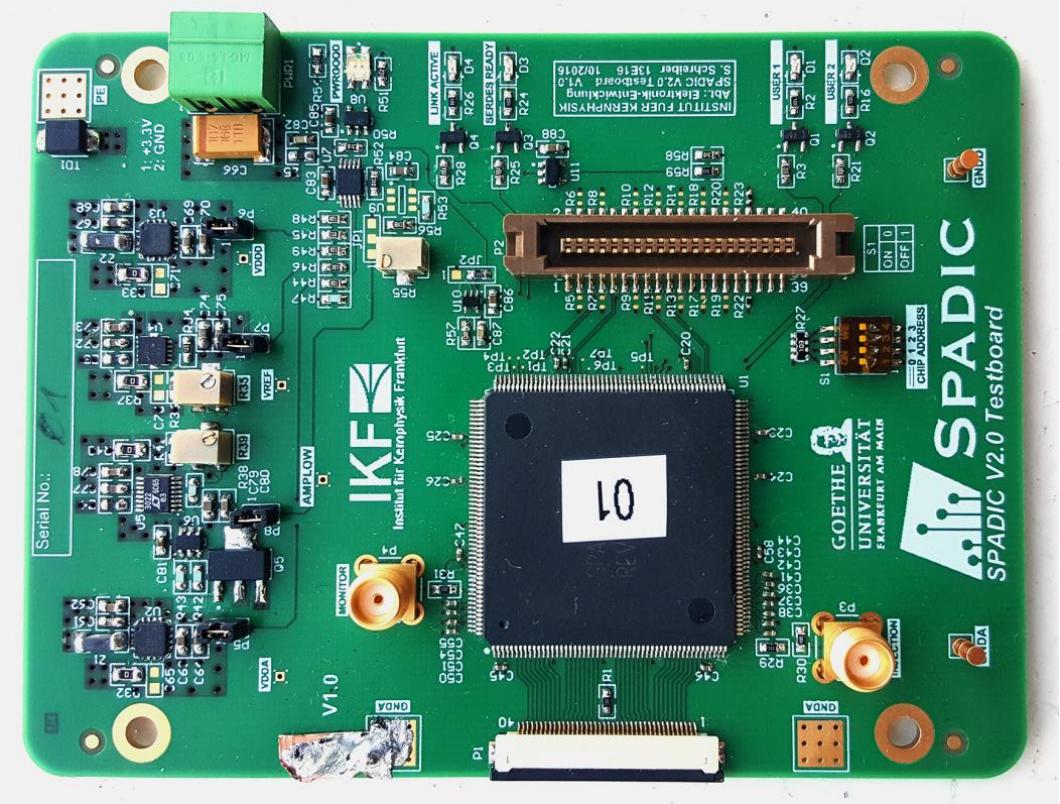
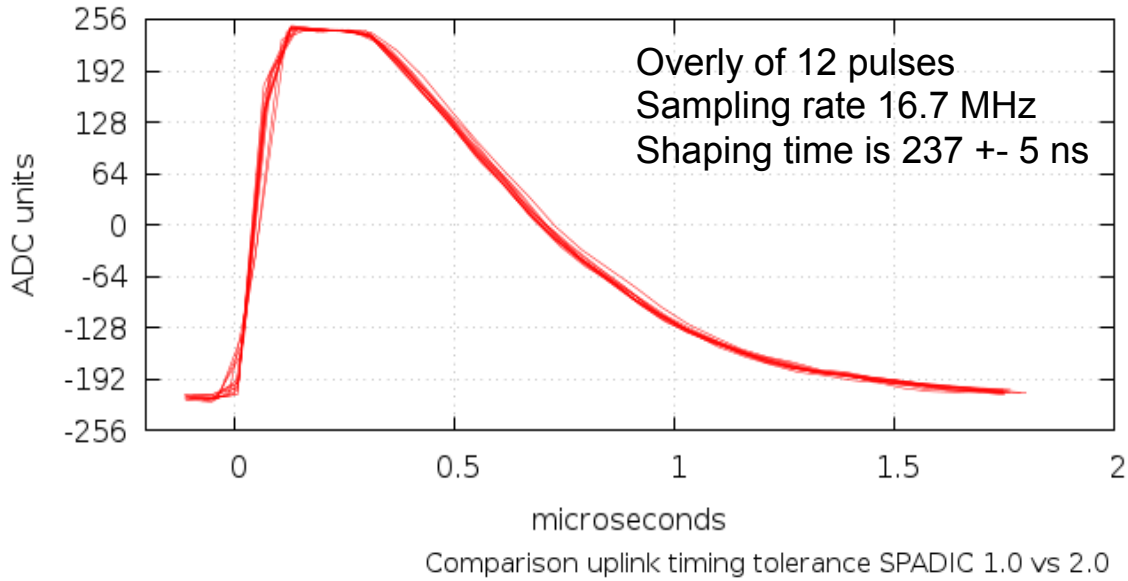


Photo: Cruz Garcia

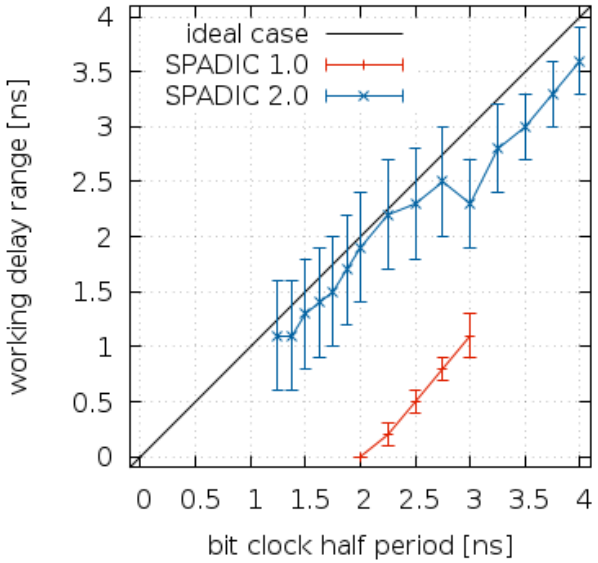
SPADIC 2.0 Works as Expected

- Sampled pulses:



- Timing tolerance of serial interface is largely improved wrt. SPADIC 1.0:

Comparison uplink timing tolerance SPADIC 1.0 vs 2.0



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Next Steps

- Enough SPADIC2.0 available for upcoming detector tests
- Results will tell us if changes are needed
  - e.g. amplifier shaping time, gain

- Planned changes for 'final' SPADIC2.1 are related to data format / volume:

Revision of data format

- Currently, the STS-XYTER protocol is not efficiently used (one 16-bit word in one 23-bit frame – 7 bits per frame wasted)
- Some of the transmitted data is redundant (e.g. group ID mirrors information already known further “up” in the DAQ chain)
- Investigate more clever ways to reduce the amount of data (e.g. combine data from neighboring channels which belong together anyway)

Summary

- The 32 channel SPADIC is available since several years
- It contains Charge Amplifier, ADC, Filter, a flexible hit detection and self-triggered serial readout

- SPADIC has been used for several detector tests successfully

- Latest SPADIC2.0 implements E-Link protocol
- Chip is functioning

- Expected changes for 'hopefully final' SPADIC2.1 are small.