Calibration of a FPGA TDC

M. Heil
Time-over-Threshold measurements

Conversion from an amplitude or charge measurement to a time measurement.

\[ \text{ToT} = t_{le} - t_{te} \]
Working principle of a “normal” TDC

- Time is measured between start and stop signal.
- Each bin has same time duration.
- Time measurement is limited to a certain number of channels.
- Calibration with a time calibrator.

![Diagram of TDC principle]
Working principle of a FPGA TDC

- Time measurement split in coarse (clock cycle) and fine (channel) time.

![Diagram showing coarse and fine time measurements]
Working principle of a FPGA TDC

- Time measurement split in coarse (clock cycle) and fine (channel) time.
- LVDS Signal is sampled via delays of carry chain of FPGA.
- Signal level is recorded in logic modules (flip flops)

Delays are not constant !!!
Every channel has a different bin size.

Results are stored in a buffer and can be read out later by a read-out trigger.
Calibration of times

LosMapped.fTimeCoarse

- Counts
- Channels
- Entries: 8720656
- Mean: 4094
- Std Dev: 2365

LosMapped.fTimeFine

- Counts
- Channels
- Entries: 8720656
- Mean: 498.9
- Std Dev: 213.8
Calibration of times

\[ \text{fineTime}(\text{bin}) = \frac{\sum_{i=0}^{\text{bin}} \text{counts}(i)}{\sum_{i=0}^{\text{max}} \text{counts}(i)} \times \text{clockTime} \]

\[ t_{\text{ns}} = \text{clockCycle} \times \text{clockTime} - \text{fineTime} \]

Calibration done channel by channel as look-up table
Overflow of coarse counter

- The coarse counter of Tamex2 (Ptof) is reset at 8191. Time differences for which one coarse counter is reset have peculiar times. This has to be corrected.
  
  e.g.:
  
  ```
  while(tt-tl<0){
      tt=tt+2048*clockTime;
  }
  ```

- The coarse counter of VFTX2 (LOS) is reset at 2047. Time differences between LOS and Ptof have to be corrected for this.
Time-of-flight measurements in Cave C

- All times are measured relative to one common clock signal.
Pictures of setup and FPGA TDCs
Advantages of FPGA TDC

- Long time differences can be measured accurately by dividing the time into a coarse and fine measurement.
- FPGA TDC measures time differences with a precision of up to $\sigma_t \sim 7$ ps.
- It can be calibrated with physics data. No time calibrator necessary.
- All events within a large trigger window of $\pm 10$ $\mu$s can be stored and read out later by a read-out trigger.
- It can handle multi-hits.
- All detectors measure relative to same clock signal.